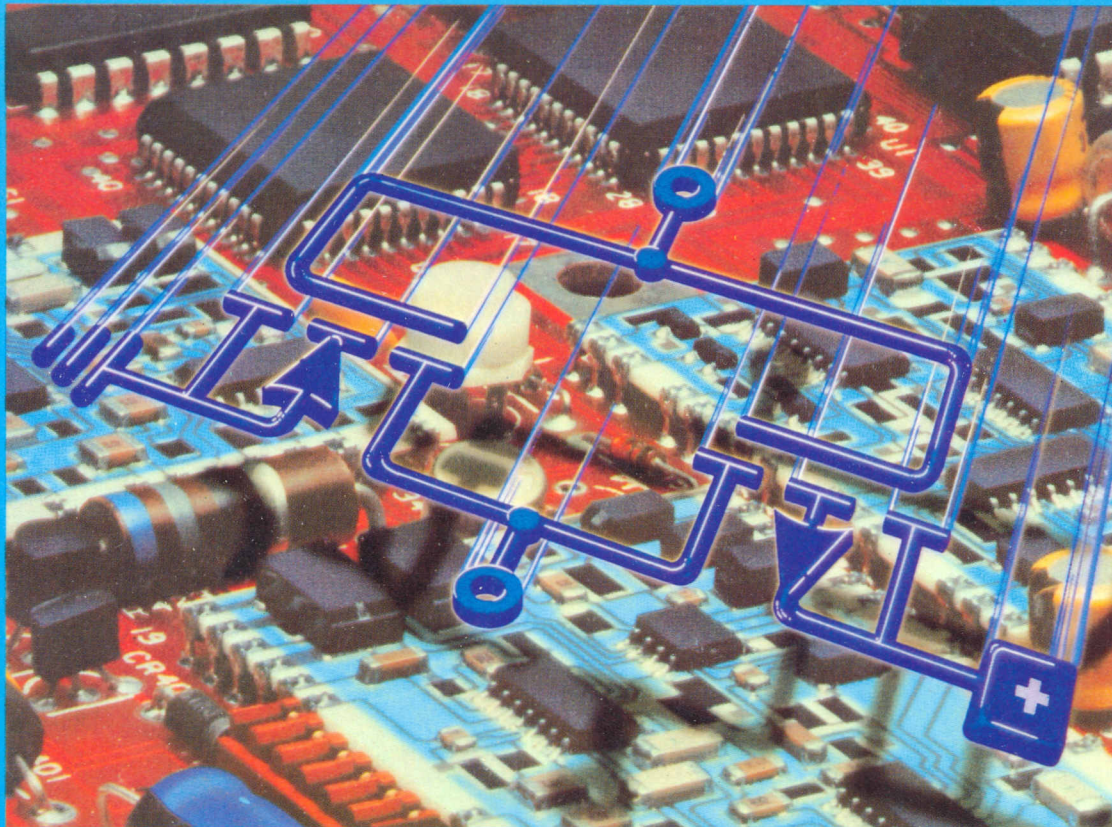


**MOTOROLA Semiconductors****ADVANCED SEMICONDUCTOR DEVICES (PTY) LTD.****P.O. BOX 2944
JOHANNESBURG 2000
TEL. 802-5820**

HIGH-SPEED CMOS LOGIC DATA

Alphanumeric Index **1**

Function Selector Guide **2**

The "Better" Program **3**

Design Considerations **4**

Data Sheets **5**

Reliability **6**

Package Dimensions **7**

Q quantum electronics
Box 391262
Bramley
2018

DATA CLASSIFICATION

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

This heading on a data sheet indicates that the device is in sampling, pre-production, or first production stages. The disclaimer at the bottom of the first page reads: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your local Motorola Semiconductor Sales Office.



MOTOROLA

HIGH-SPEED CMOS LOGIC DATA

Prepared by
Technical Information Center

This book presents technical data for the broad line of High-Speed Logic integrated circuits. Complete specifications are provided in the form of data sheets. In addition, a comprehensive Function Selector Guide and a Design Considerations chapter have been included to familiarize the user with these logic circuits.

Motorola reserves the right to make changes to any product herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product described herein; neither does it convey any license under its patent rights nor the rights of others.

© Motorola Inc. 1984

©MOTOROLA INC.,
"All Rights Reserved"
Second Revision 1984 - B002C
Reprinted 1986 - DLE130C
Third Revision 1987 - DLE129R3
Printed in Great Britain by Eyre & Spottiswoode Ltd. 10,000, 6/87

MOTOROLA HIGH-SPEED CMOS LOGIC DATA

HIGH-SPEED CMOS LOGIC DATA

Prepared by
Technical Information Center

This book presents technical data for the broad line of High-Speed Logic integrated circuits. Complete specifications are provided in the form of data sheets. In addition, a comprehensive Function Selector Guide and a Design Considerations chapter have been included to familiarize the user with these logic circuits. Motorola reserves the right to make changes to any product herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product described herein; neither does it convey any license under its patent rights nor the rights of others.

9-Wide and Nine-Wide are trademarks of Motorola Inc.

MOTOROLA INC.
All Rights Reserved
Second Edition 1984 - 80200
Printed in USA - 018130C
Third Edition 1987 - 018130S
Printed in Great Britain by Eves & Spottiswoode Ltd. 10,000, 087

MOTOROLA HIGH-SPEED CMOS LOGIC DATA

Alphanumeric Index

1

Page Number	Function	Device Number MCM/MC3A
5-2	Quad 2-input NAND Gate	HC00
5-5	Quad 2-input NOR Gate	HC02
5-8	Quad 2-input NAND Gate with Open-Drain Outputs	HC03
5-12	Hex Inverter	HC04
5-15	Hex Inverter with LSTTL-Compatible Inputs	HC104
5-18	Hex Unbuffered Inverter	HC04A
5-22	Hex Inverter with Open-Drain Outputs	HC05
5-25	Hex Inverter with Open-Drain Outputs and LSTTL-Compatible Inputs	HC105
5-28	Quad 2-input AND Gate	HC08
5-31	Triple 3-input NAND Gate	HC10
5-34	Triple 3-input AND Gate	HC11
5-37	Hex Schmitt-Trigger Inverter	HC14
5-41	Dual 4-input NAND Gate	HC20
5-44	Triple 3-input NOR Gate	HC27
5-47	8-input NAND Gate	HC30
5-50	Quad 2-input OR Gate	HC32
5-53	Hex Noninverting Buffer	HC34
5-56	Hex Noninverting Buffer with LSTTL-Compatible Inputs	HC134
5-59	Hex Noninverting Buffer with Open-Drain Outputs	HC35
5-62	Hex Noninverting Buffer with Open-Drain Outputs and LSTTL-Compatible Inputs	HC135
5-65	1-of-10 Decoder	HC42
5-68	2-Wide, 2-input/2-Wide, 3-input AND-NOR Gates	HC51
5-72	2-Wide, 2-input/2-Wide, 3-input AND-OR Gates	HC58
5-75	Dual J-K Flip-Flop with Reset	HC73
5-78	Dual D Flip-Flop with Set and Reset	HC74
5-82	Dual 2-Bit Transparent Latch	HC75
5-87	Dual J-K Flip-Flop with Set and Reset	HC76
5-91	4-Bit Magnitude Comparator	HC85
5-97	Quad 2-input Exclusive OR Gate	HC86
5-100	Dual J-K Flip-Flop with Reset	HC107
5-104	Dual J-K Flip-Flop with Set and Reset	HC108
5-108	Dual J-K Flip-Flop with Set and Reset	HC112
5-112	Dual J-K Flip-Flop with Set	HC113
5-116	Quad 3-State Noninverting Buffer	HC125
5-119	Quad 3-State Noninverting Buffer	HC126
5-120	Quad 2-input NAND Gate with Schmitt-Trigger Inputs	HC132
5-124	13-input NAND Gate	HC133
5-127	1-of-8 Decoder/Multiplexer with Address Latch	HC137
5-132	1-of-8 Decoder/Multiplexer	HC138
5-136	Dual 1-of-4 Decoder/Multiplexer	HC139
5-140	Decimal-to-BCD Encoder	HC147
5-144	8-input Data Selector/Multiplexer	HC157
5-148	Dual 4-input Data Selector/Multiplexer	HC158
5-153	1-of-16 Decoder/Multiplexer	HC159
5-158	Quad 2-input Noninverting Data Selector/Multiplexer	HC157

ALPHANUMERIC INDEX

1

Device Number MC54/MC74	Function	Page Number
HC00	Quad 2-Input NAND Gate	5-2
HC02	Quad 2-Input NOR Gate	5-5
HC03	Quad 2-Input NAND Gate with Open-Drain Outputs	5-8
HC04	Hex Inverter	5-12
HCT04	Hex Inverter with LSTTL-Compatible Inputs	5-15
HCU04	Hex Unbuffered Inverter	5-18
HC05	Hex Inverter with Open-Drain Outputs	5-22
HCT05	Hex Inverter with Open-Drain Outputs and LSTTL-Compatible Inputs	5-25
HC08	Quad 2-Input AND Gate	5-28
HC10	Triple 3-Input NAND Gate	5-31
HC11	Triple 3-Input AND Gate	5-34
HC14	Hex Schmitt-Trigger Inverter	5-37
HC20	Dual 4-Input NAND Gate	5-41
HC27	Triple 3-Input NOR Gate	5-44
HC30	8-Input NAND Gate	5-47
HC32	Quad 2-Input OR Gate	5-50
HC34	Hex Noninverting Buffer	5-53
HCT34	Hex Noninverting Buffer with LSTTL-Compatible Inputs	5-56
HC35	Hex Noninverting Buffer with Open-Drain Outputs	5-59
HCT35	Hex Noninverting Buffer with Open-Drain Outputs and LSTTL-Compatible Inputs	5-62
HC42	1-of-10 Decoder	5-65
HC51	2-Wide, 2-Input/2-Wide, 3-Input AND-NOR Gates	5-69
HC58	2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates	5-72
HC73	Dual J-K Flip-Flop with Reset	5-75
HC74	Dual D Flip-Flop with Set and Reset	5-79
HC75	Dual 2-Bit Transparent Latch	5-83
HC76	Dual J-K Flip-Flop with Set and Reset	5-87
HC85	4-Bit Magnitude Comparator	5-91
HC86	Quad 2-Input Exclusive OR Gate	5-97
HC107	Dual J-K Flip-Flop with Reset	5-100
HC109	Dual J-K Flip-Flop with Set and Reset	5-104
HC112	Dual J-K Flip-Flop with Set and Reset	5-108
HC113	Dual J-K Flip-Flop with Set	5-112
HC125	Quad 3-State Noninverting Buffer	5-116
HC126	Quad 3-State Noninverting Buffer	5-116
HC132	Quad 2-Input NAND Gate with Schmitt-Trigger Inputs	5-120
HC133	13-Input NAND Gate	5-124
HC137	1-of-8 Decoder/Demultiplexer with Address Latch	5-127
HC138	1-of-8 Decoder/Demultiplexer	5-132
HC139	Dual 1-of-4 Decoder/Demultiplexer	5-136
HC147	Decimal-to-BCD Encoder	5-140
HC151	8-Input Data Selector/Multiplexer	5-144
HC153	Dual 4-Input Data Selector/Multiplexer	5-149
HC154	1-of-16 Decoder/Demultiplexer	5-153
HC157	Quad 2-Input Noninverting Data Selector/Multiplexer	5-158

ALPHANUMERIC INDEX

1

Device Number	Function	Page Number
MC54/MC74		
HC158	Quad 2-Input Inverting Data Selector/Multiplexer	5-158
HC160	Presetable BCD Counter with Asynchronous Reset	5-163
HC161	Presetable 4-Bit Binary Counter with Asynchronous Reset	5-163
HC162	Presetable BCD Counter with Synchronous Reset	5-163
HC163	Presetable 4-Bit Binary Counter with Synchronous Reset	5-163
HC164	8-Bit Serial-Input/Parallel-Output Shift Register	5-177
HC165	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register	5-182
HC173	Quad 3-State D Flip-Flop with Common Clock and Reset	5-188
HC174	Hex D Flip-Flop with Common Clock and Reset	5-193
HC175	Quad D Flip-Flop with Common Clock and Reset	5-197
HC194	4-Bit Bidirectional Universal Shift Register	5-202
HC195	4-Bit Universal Shift Register	5-208
HC237	1-of-8 Decoder/Demultiplexer with Address Latch	5-214
HC240	Octal 3-State Inverting Buffer/Line Driver/Line Receiver	5-219
HCT240	Octal 3-State Inverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	5-223
HC241	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	5-227
HCT241	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	5-231
HC242	Quad 3-State Inverting Bus Transceiver	5-235
HC243	Quad 3-State Noninverting Bus Transceiver	5-235
HC244	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	5-240
HCT244	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	5-244
HC245	Octal 3-State Noninverting Bus Transceiver	5-248
HCT245	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	5-252
HC251	8-Input Data Selector/Multiplexer with 3-State Outputs	5-256
HC253	Dual 4-Input Data Selector/Multiplexer with 3-State Outputs	5-261
HC257	Quad 2-Input Data Selector/Multiplexer with 3-State Outputs	5-265
HC259	8-Bit Addressable Latch/1-of-8 Decoder	5-270
HC266	Quad 2-Input Exclusive NOR Gate with Open-Drain Outputs	5-275
HC273	Octal D Flip-Flop with Common Clock and Reset	5-279
HC280	9-Bit Odd/Even Parity Generator/Checker	5-284
HC283	4-Bit Binary Full Adder with Fast Carry	5-289
HC299	8-Bit Bidirectional Universal Shift Register with Parallel I/O	5-293
HC354	8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs	5-300
HC356	8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs	5-306
HC365	Hex 3-State Noninverting Buffer with Common Enables	5-312
HC366	Hex 3-State Inverting Buffer with Common Enables	5-316
HC367	Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections	5-320
HC368	Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections	5-324
HC373	Octal 3-State Noninverting Transparent Latch	5-328
HCT373	Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs	5-332

HC374	Octal 3-State Noninverting D Flip-Flop	5-336
HCT374	Octal 3-State Noninverting D Flip-Flop with LSTTL-Compatible Inputs	5-340
HC386	Quad 2-Input Exclusive OR Gate	5-344
HC390	Dual 4-Stage Binary Ripple Counter with $\div 2$ and $\div 5$ Sections	5-347
HC393	Dual 4-Stage Binary Ripple Counter	5-353
HC533	Octal 3-State Inverting Transparent Latch	5-358
HCT533	Octal 3-State Inverting Transparent Latch with LSTTL-Compatible Inputs	5-362
HC534	Octal 3-State Inverting D Flip-Flop	5-366
HCT534	Octal 3-State Inverting D Flip-Flop with LSTTL-Compatible Inputs	5-370
HC540	Octal 3-State Inverting Buffer/Line Driver/Line Receiver	5-374
HCT540	Octal 3-State Inverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	5-378
HC541	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	5-382
HCT541	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	5-386
HC563	Octal 3-State Inverting Transparent Latch	5-390
HC564	Octal 3-State Inverting D Flip-Flop	5-395
HC573	Octal 3-State Noninverting Transparent Latch	5-400
HC574	Octal 3-State Noninverting D Flip-Flop	5-405
HC589	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with 3-State Output	5-410
HC595	8-Bit Serial-Input/Serial- or Parallel-Output Shift Register with Latched 3-State Outputs	5-418
HC597	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with Input Latch	5-425
HC620	Octal 3-State Inverting Bus Transceiver	5-432
HCT620	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs	5-436
HC623	Octal 3-State Noninverting Bus Transceiver	5-440
HCT623	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	5-444
HC640	Octal 3-State Inverting Bus Transceiver	5-448
HCT640	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs	5-452
HC643	Octal 3-State Inverting and Noninverting Bus Transceiver	5-456
HCT643	Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs	5-460
HC646	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	5-464
HC648	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	5-464
HC651	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	5-475
HC652	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	5-475
HC688	8-Bit Equality Comparator	5-486
HC793	Octal 3-State Noninverting Transparent Latch with Readback	5-490
HC4002	Dual 4-Input NOR Gate	5-495
HC4016	Quad Analog Switch/Multiplexer/Demultiplexer	5-498
HC4017	Decade Counter	5-507
HC4020	14-Stage Binary Ripple Counter	5-515
HC4024	7-Stage Binary Ripple Counter	5-520
HC4040	12-Stage Binary Ripple Counter	5-525

ALPHANUMERIC INDEX

1

Device Number MC54/MC74	Function	Page Number
HC4049	Hex Inverting Buffer/Logic-Level Down Converter	5-530
HC4050	Hex Noninverting Buffer/Logic-Level Down Converter	5-530
HC4051	8-Channel Analog Multiplexer/Demultiplexer	5-534
HC4052	Dual 4-Channel Analog Multiplexer/Demultiplexer	5-534
HC4053	Triple 2-Channel Analog Multiplexer/Demultiplexer	5-534
HC4060	14-Stage Binary Ripple Counter with Oscillator	5-546
HC4066	Quad Analog Switch/Multiplexer/Demultiplexer	5-554
HC4075	Triple 3-Input OR Gate	5-563
HC4078	8-Input NOR/OR Gate	5-566
HC4316	Quad Analog Switch/Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies	5-570
HC4351	8-Channel Analog Multiplexer/Demultiplexer with Address Latch	5-579
HC4352	Dual 4-Channel Analog Multiplexer/Demultiplexer with Address Latch	5-579
HC4353	Triple 2-Channel Analog Multiplexer/Demultiplexer with Address Latch	5-579
HC4511	BCD-to-Seven-Segment Latch/Decoder/Display Driver	5-591
HC4514	1-of-16 Decoder/Demultiplexer with Address Latch	5-598
HC4538	Dual Precision Monostable Multivibrator (Retriggerable, Resettable)	5-605
HC4543	BCD-to-Seven-Segment Latch/Decoder/Display Driver for LCDs	5-615
HC7266	Quad 2-Input Exclusive NOR Gate	5-622
HC7793	Octal 3-State Noninverting Transparent Latch with Readback	5-626
HC9000	Programmable Timer	5-631
HC9014	Nine-Wide Schmitt-Trigger Inverter	5-645
HC9015	Nine-Wide Schmitt-Trigger Noninverting Buffer	5-645
HC9034	Nine-Wide Inverter	5-649
HCT9034	Nine-Wide Inverter with LSTTL-Compatible Inputs	5-652
HC9035	Nine-Wide Noninverting Buffer	5-649
HCT9035	Nine-Wide Noninverting Buffer with LSTTL-Compatible Inputs	5-652
HC9114	Nine-Wide Schmitt-Trigger Inverter with Open-Drain Outputs	5-655
HC9115	Nine-Wide Schmitt-Trigger Noninverting Buffer with Open-Drain Outputs	5-655
HC9134	Nine-Wide Inverter with Open-Drain Outputs	5-659
HC9135	Nine-Wide Noninverting Buffer with Open-Drain Outputs	5-659

Device Number	Function	Page Number
HC9135	Nine-Wide Noninverting Buffer with Open-Drain Outputs	5-550
HC9134	Nine-Wide Inverter with Open-Drain Outputs	5-550
HC9135	Nine-Wide Noninverting Buffer with Open-Drain Outputs	5-550
HC9136	Nine-Wide Schmitt-Trigger Noninverting Buffer with Open-Drain Outputs	5-550
HC9137	Nine-Wide Schmitt-Trigger Inverter with Open-Drain Outputs	5-550
HC9138	Nine-Wide Noninverting Buffer with LSTTL-Compatible Inputs	5-550
HC9139	Nine-Wide Inverter with LSTTL-Compatible Inputs	5-550
HC9140	Nine-Wide Inverter	5-549
HC9141	Nine-Wide Schmitt-Trigger Inverter	5-548
HC9142	Programmable Timer	5-531
HC7393	Octal 3-State Noninverting Transparent Latch with Readback	5-528
HC7394	Quad 3-Input Exclusive NOR Gate	5-523
HC643	BCD-to-Seven-Segment Latch/Decoder/Display Driver for LCDs	5-515
HC638	Dual Precision Monostable Multivibrator (Retriggable, Resettable)	5-505
HC614	1-of-16 Decoder/Demultiplexer with Address Latch	5-500
HC611	BCD-to-Seven-Segment Latch/Decoder/Display Driver	5-501
HC603	Triple 3-Channel Analog Multiplexer/Demultiplexer with Address Latch	5-570
HC602	Dual 4-Channel Analog Multiplexer/Demultiplexer with Address Latch	5-570
HC601	3-Channel Analog Multiplexer/Demultiplexer with Address Latch	5-570
HC600	Digital Power Supplies	5-570
HC4318	Quad Analog Switch/Multiplexer/Demultiplexer with Separate Analog and 8-Input NOR/OR Gate	5-568
HC4375	Triple 3-Input OR Gate	5-563
HC4086	Quad Analog Switch/Multiplexer/Demultiplexer	5-554
HC4080	14-Stage Binary Ripple Counter with Oscillator	5-548
HC4083	Triple 3-Channel Analog Multiplexer/Demultiplexer	5-534
HC4082	Dual 4-Channel Analog Multiplexer/Demultiplexer	5-534
HC4081	3-Channel Analog Multiplexer/Demultiplexer	5-534
HC4080	Hex Noninverting Buffer/Logic-Level Down Converter	5-530
HC4049	Hex Inverting Buffer/Logic-Level Down Converter	5-530

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC04	Hex Inverter	LS04	*4069	LS/CMOS	14
HCT04	Hex Inverter with LSTTL-Compatible Inputs	LS04	*4069	LS/CMOS	14
HCU04	Hex Unbuffered Inverter	LS04	4069	LS/CMOS	14
HC05	Hex Inverter with Open-Drain Outputs	LS05		LS	14
HCT05	Hex Inverter with Open-Drain Outputs and LSTTL-Compatible Inputs	LS05		LS	14
HC14	Hex Schmitt-Trigger Inverter	LS14	4584	LS/CMOS	14
HC34	Hex Noninverting Buffer	LS34		LS	14
HCT34	Hex Noninverting Buffer with LSTTL-Compatible Inputs	LS34		LS	14
HC35	Hex Noninverting Buffer with Open-Drain Outputs	LS35		LS	14
HCT35	Hex Noninverting Buffer with Open-Drain Outputs and LSTTL-Compatible Inputs	LS35		LS	14
HC125	Quad 3-State Noninverting Buffer	LS125,LS125A		LS	14
HC126	Quad 3-State Noninverting Buffer	LS126,LS126A		LS	14
HC240	Octal 3-State Inverting Buffer/Line Driver/Line Receiver	LS240		LS	20
HCT240	Octal 3-State Inverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS240		LS	20
HC241	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	LS241		LS	20
HCT241	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS241		LS	20
HC242	Quad 3-State Inverting Bus Transceiver	LS242		LS	14
HC243	Quad 3-State Noninverting Bus Transceiver	LS243		LS	14
HC244	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	LS244		LS	20
HCT244	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS244		LS	20
HC245	Octal 3-State Noninverting Bus Transceiver	LS245		LS	20
HCT245	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS245		LS	20
HC365	Hex 3-State Noninverting Buffer with Common Enables	LS365,LS365A		LS	16
HC366	Hex 3-State Inverting Buffer with Common Enables	LS366,LS366A		LS	16
HC367	Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections	LS367,LS367A	4503	LS/CMOS	16
HC368	Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections	LS368,LS368A		LS	16
HC540	Octal 3-State Inverting Buffer/Line Driver/Line Receiver	LS540		LS	20
HCT540	Octal 3-State Inverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS540		LS	20
HC541	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver	LS541		LS	20
HCT541	Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs	LS541		LS	20
HC620	Octal 3-State Inverting Bus Transceiver	LS620		LS	20
HCT620	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs	LS620		LS	20
HC623	Octal 3-State Noninverting Bus Transceiver	LS623		LS	20
HCT623	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS623		LS	20
HC640	Octal 3-State Inverting Bus Transceiver	LS640		LS	20
HCT640	Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs	LS640		LS	20
HC643	Octal 3-State Inverting and Noninverting Bus Transceiver	LS643		LS	20
HCT643	Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS643		LS	20
HC4049	Hex Inverting Buffer/Logic-Level Down Converter		4049	CMOS	16
HC4050	Hex Noninverting Buffer/Logic-Level Down Converter		4050	CMOS	16

BUFFERS/INVERTERS (Continued)

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
★ HC9014	Nine-Wide Schmitt-Trigger Inverter				20
★ HC9015	Nine-Wide Schmitt-Trigger Noninverting Buffer				20
★ HC9034	Nine-Wide Inverter				20
★ HCT9034	Nine-Wide Inverter with LSTTL-Compatible Inputs				20
★ HC9035	Nine-Wide Noninverting Buffer				20
★ HCT9035	Nine-Wide Noninverting Buffer with LSTTL-Compatible Inputs				20
★ HC9114	Nine-Wide Schmitt-Trigger Inverter with Open-Drain Outputs				20
★ HC9115	Nine-Wide Schmitt-Trigger Noninverting Buffer with Open-Drain Outputs				20
★ HC9134	Nine-Wide Inverter with Open-Drain Outputs				20
★ HC9135	Nine-Wide Noninverting Buffer with Open-Drain Outputs				20

* Suggested alternative

★ Exclusive High-Speed CMOS design

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HC HCT 04	HC HCU 04	HC HCT 05	HC HCT 14	HC HCT 34	HC HCT 35	HC HCT 125	HC HCT 126	HC HCT 240	HC HCT 241	HC HCT 242	HC HCT 243	HC HCT 244
# Pins	14	14	14	14	14	14	14	14	20	20	14	24	20
Quad Device													
Hex Device	•	•	•	•	•	•	•						
Octal Device									•	•			•
Nine-Wide Device													
Noninverting Outputs	•	•	•	•		•	•	•	•	•		•	•
Inverting Outputs	•	•	•	•		•	•	•	•	•		•	•
Single Stage (unbuffered)		•											
Schmitt Trigger				•									
3-State Outputs							•	•	•	•			•
Open-Drain Outputs			•			•							
Common Output Enables									•	•	•	•	•
Active-Low Output Enables							•		•	•	•	•	•
Active-High Output Enables								•		•	•	•	•
Separate 4-Bit Sections									•	•			•
Separate 2-Bit and 4-Bit Sections													
Transceiver												•	•
Direction Control													
Logic-Level Down Converter													

BUFFERS/INVERTERS (Continued)

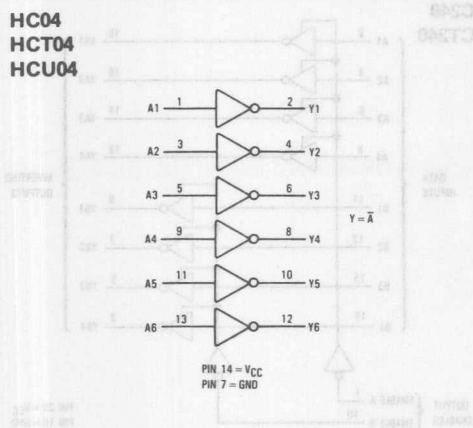
Device Number	Function	Functional Equivalent LSTTL Device	Functional Equivalent CMOS Device	Pin Compatibility	Number of Pins						
HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.											
Device	HC HCT 245	HC 365	HC 366	HC 367	HC 368	HC HCT 540	HC HCT 541	HC HCT 620	HC HCT 623	HC HCT 640	HC HCT 643
# Pins	20	16	16	16	16	20	20	20	20	20	20
Quad Device											
Hex Device		•		•	•	•	•	•	•	•	•
Octal Device	•					•	•	•	•	•	•
Nine-Wide Device											
Noninverting Outputs	•	•		•	•	•	•	•	•	•	•
Inverting Outputs			•		•	•	•	•		•	•
Single Stage (unbuffered)											
Schmitt Trigger											
3-State Outputs	•	•	•	•	•	•	•	•	•	•	•
Open-Drain Outputs											
Common Output Enables	•	•				•	•	•			
Active-Low Output Enables	•	•	•	•	•	•	•	•		•	•
Active-High Output Enables											
Separate 4-Bit Sections											
Separate 2-Bit and 4-Bit Sections				•	•						
Transceiver	•							•	•	•	•
Direction Control	•									•	•
Logic-Level Down Converter											

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

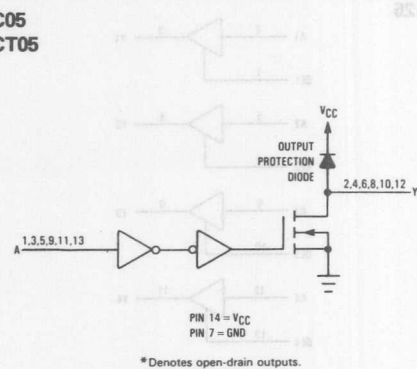
Device	HC 4049	HC 4050	HC 9014	HC 9015	HC HCT 9034	HC HCT 9035	HC 9114	HC 9115	HC 9134	HC 9135
# Pins	16	16	20	20	20	20	20	20	20	20
Quad Device										
Hex Device	•	•								
Octal Device										
Nine-Wide Device			•	•	•	•	•	•	•	•
Noninverting Outputs		•		•	•	•		•	•	•
Inverting Outputs	•		•		•		•		•	•
Single Stage (unbuffered)										
Schmitt Trigger			•	•			•	•		
3-State Outputs										
Open-Drain Outputs							•	•	•	•
Common Output Enables										
Active-Low Output Enables										
Active-High Output Enables										
Separate 4-Bit Sections										
Separate 2-Bit and 4-Bit Sections										
Transceiver										
Direction Control										
Logic-Level Down Converter	•	•								

BUFFERS/INVERTERS (Continued)

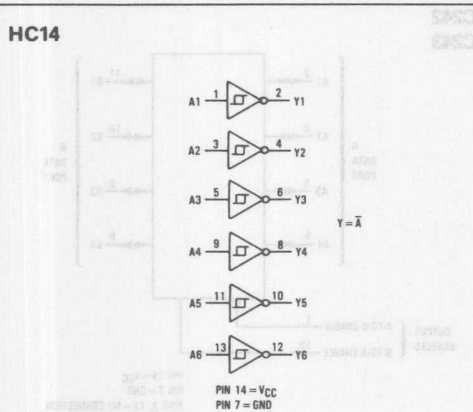
**HC04
HCT04
HCU04**



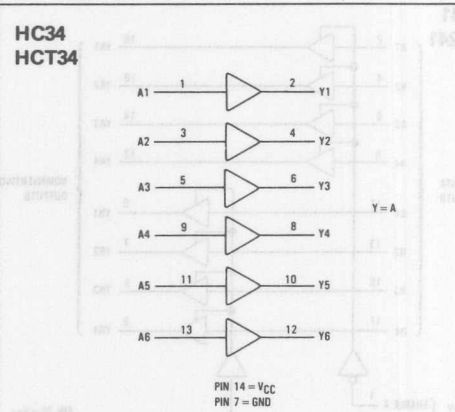
**HC05
HCT05**



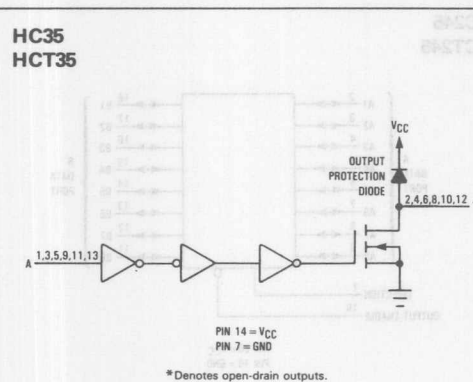
HC14



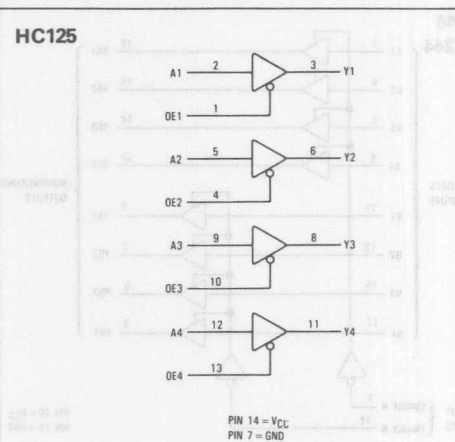
**HC34
HCT34**

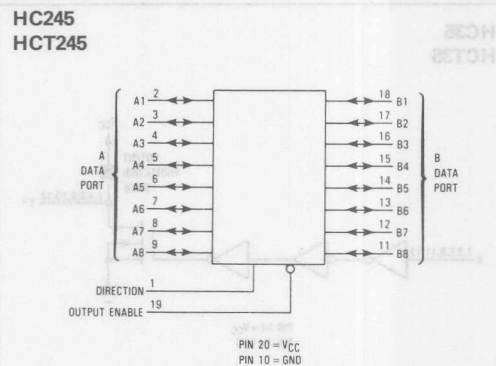
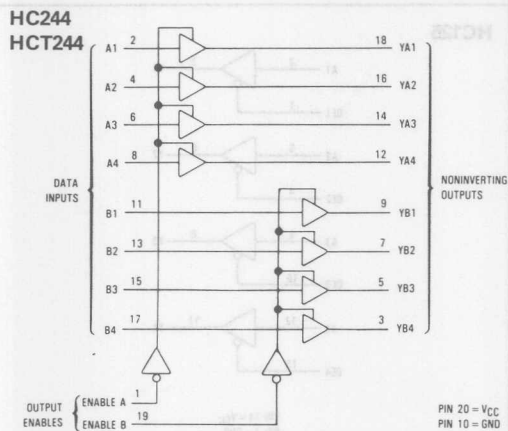
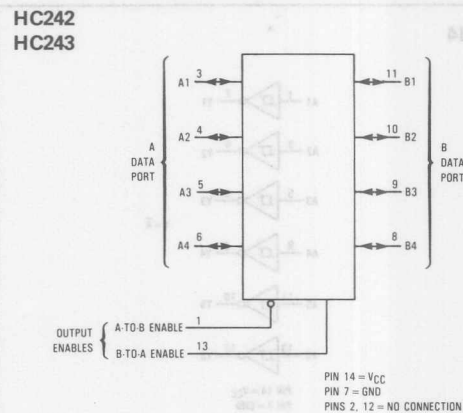
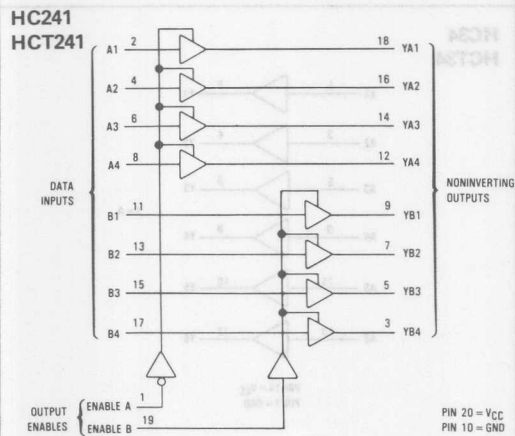
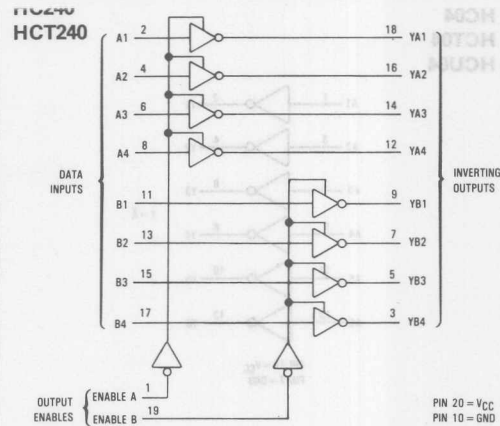
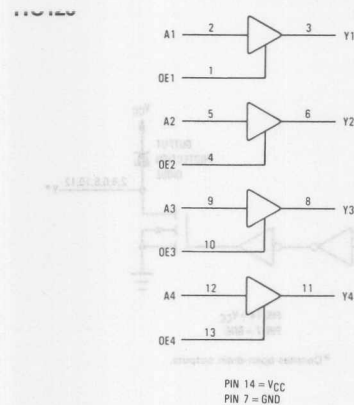


**HC35
HCT35**



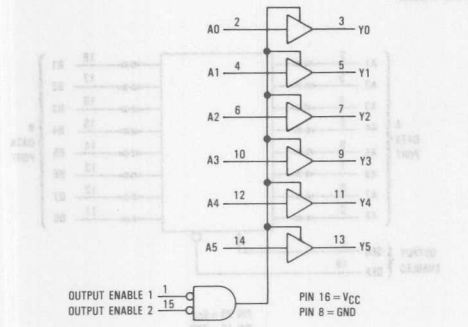
HC125



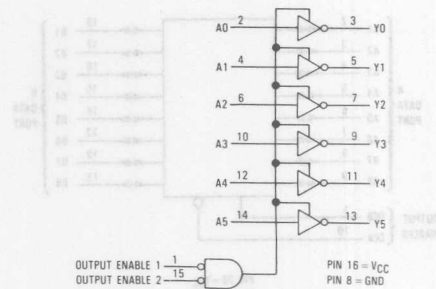


BUFFERS/INVERTERS (Continued)

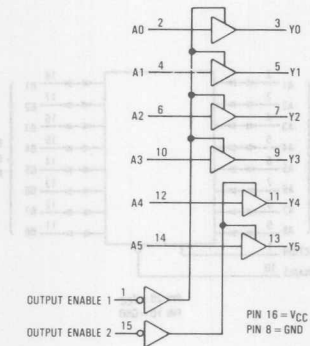
HC365



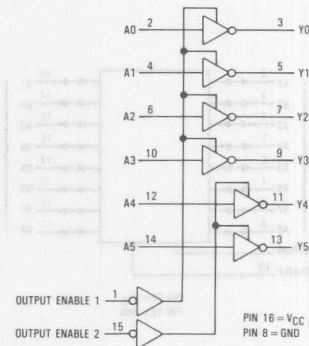
HC366



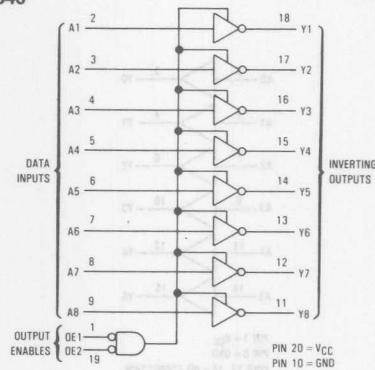
HC367



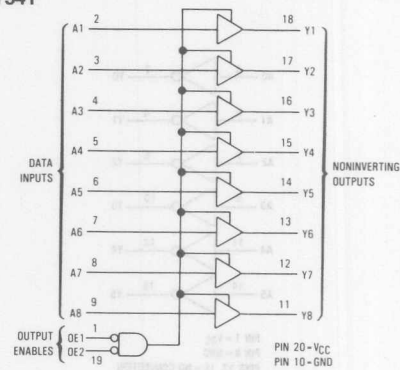
HC368



**HC540
HCT540**



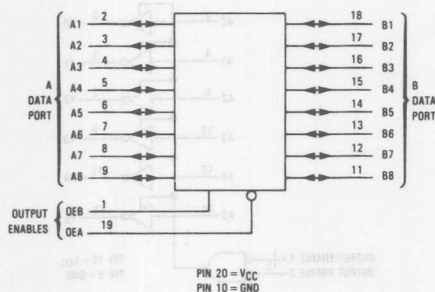
**HC541
HCT541**



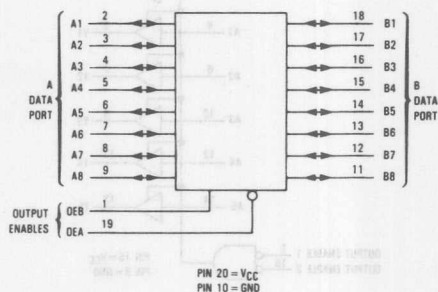
BUFFERS/INVERTERS (Continued)

2

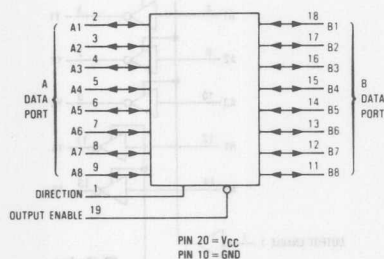
**HC620
HCT620**



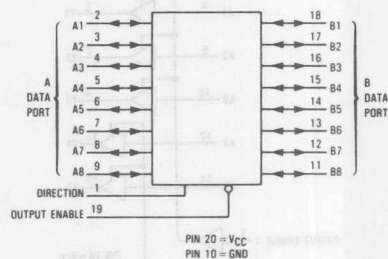
**HC623
HCT623**



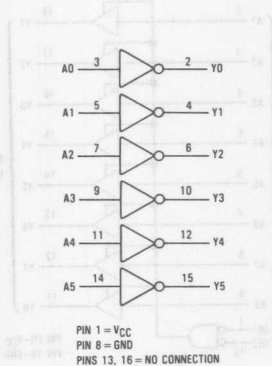
**HC640
HCT640**



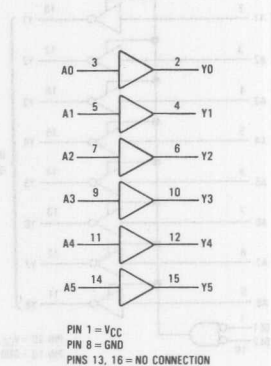
**HC643
HCT643**



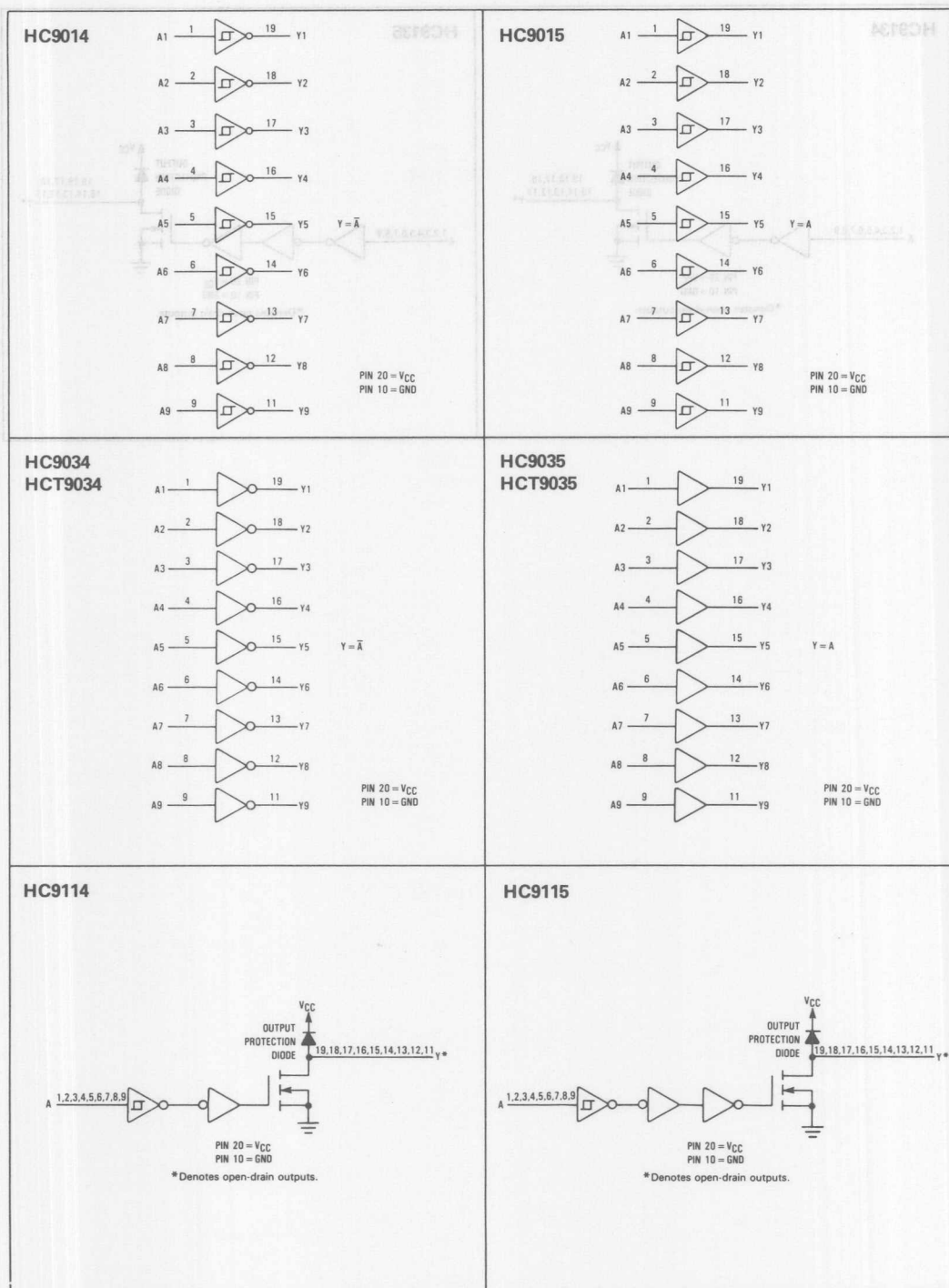
HC4049

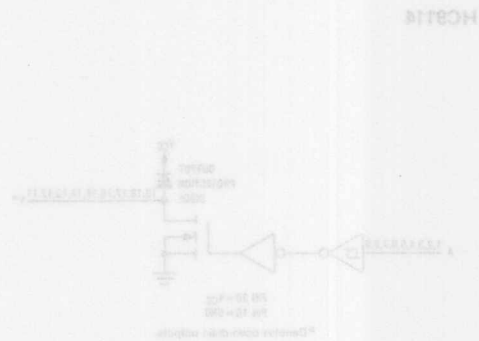
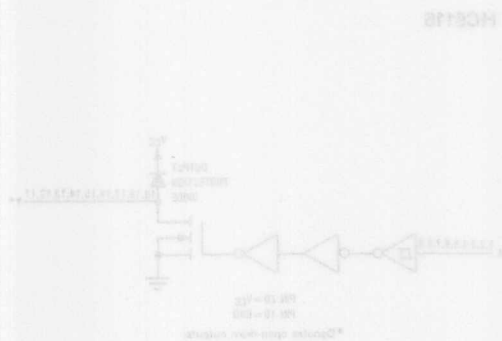
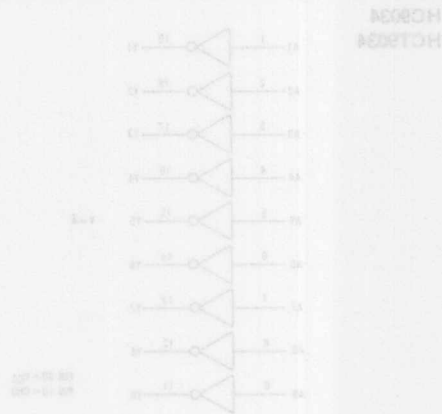
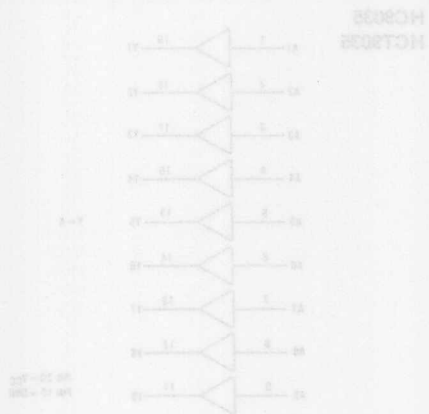
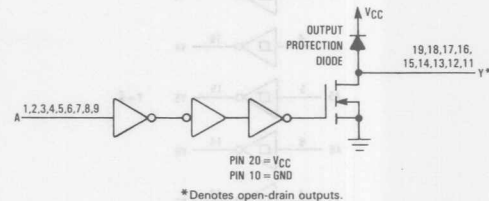
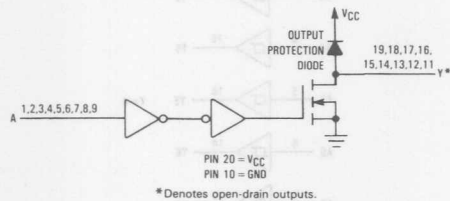


HC4050



BUFFERS/INVERTERS (Continued)





GATES

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC00	Quad 2-Input NAND Gate	LS00	4011	LS	14
HC02	Quad 2-Input NOR Gate	LS02	4001	LS	14
HC03	Quad 2-Input NAND Gate with Open-Drain Outputs	LS03	*4011	LS	14
HC08	Quad 2-Input AND Gate	LS08	4081	LS	14
HC10	Triple 3-Input NAND Gate	LS10	4023	LS	14
HC11	Triple 3-Input AND Gate	LS11	4073	LS	14
HC20	Dual 4-Input NAND Gate	LS20	4012	LS	14
HC27	Triple 3-Input NOR Gate	LS27	4025	LS	14
HC30	8-Input NAND Gate	LS30	4068	LS	14
HC32	Quad 2-Input OR Gate	LS32	4071	LS	14
HC51	2-Wide, 2-Input/2-Wide, 3-Input AND-NOR Gates	LS51	*4506	LS	14
*HC58	2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates		*4506		14
HC86	Quad 2-Input Exclusive OR Gate	LS86	4070	LS	14
HC132	Quad 2-Input NAND Gate with Schmitt-Trigger Inputs	LS132	4093	LS	14
HC133	13-Input NAND Gate	LS133		LS	16
HC266	Quad 2-Input Exclusive NOR Gate with Open-Drain Outputs	LS266	*4077	LS/CMOS	14
HC386	Quad 2-Input Exclusive OR Gate	LS386	4070	LS/CMOS	14
HC4002	Dual 4-Input NOR Gate	*LS25	4002	CMOS	14
HC4075	Triple 3-Input OR Gate		4075	CMOS	14
HC4078	8-Input NOR/OR Gate		4078	CMOS	14
*HC7266	Quad 2-Input Exclusive NOR Gate	*LS266	4077	LS/CMOS	14

*Suggested alternative

*Exclusive High-Speed CMOS design

GATES (Continued)

HC Devices Have CMOS-Compatible Inputs.

Device	HC 00	HC 02	HC 03	HC 08	HC 10	HC 11	HC 20	HC 27	HC 30	HC 32
# Pins	14	14	14	14	14	14	14	14	14	14
Single Device										
Dual Device										
Triple Device										
Quad Device										
NAND										
NOR										
AND										
OR										
Exclusive OR										
Exclusive NOR										
AND-NOR										
AND-OR										
2-Input										
3-Input										
4-Input										
8-Input										
13-Input										
Schmitt-Trigger Inputs										
Open-Drain Outputs										

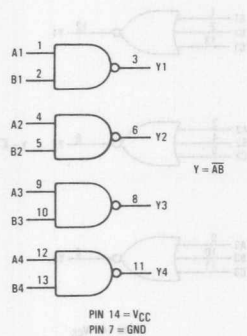
HC Devices Have CMOS-Compatible Inputs.

Device	HC 51	HC 58	HC 86	HC 132	HC 133	HC 266	HC 386	HC 4002	HC 4075	HC 4078	HC 7266
# Pins	14	14	14	14	16	14	14	14	14	14	14
Single Device											
Dual Device											
Triple Device											
Quad Device											
NAND											
NOR											
AND											
OR											
Exclusive OR											
Exclusive NOR											
AND-NOR											
AND-OR											
2-Input											
3-Input											
4-Input											
8-Input											
13-Input											
Schmitt-Trigger Inputs											
Open-Drain Outputs											

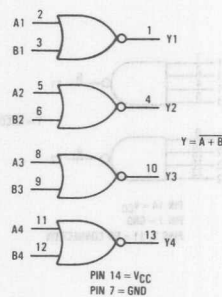
These devices are identical in function and are different in pinout only: HC86 and HC386

GATES (Continued)

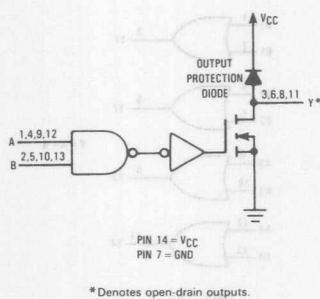
HC00



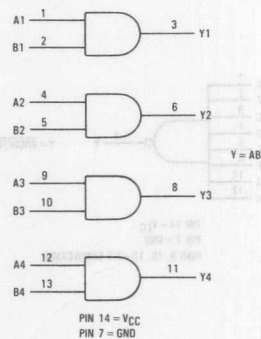
HC02



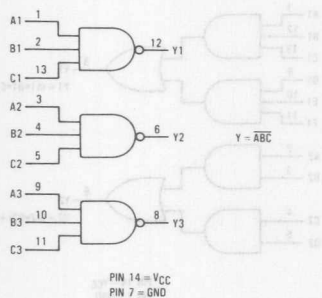
HC03



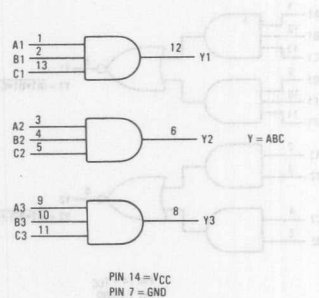
HC08

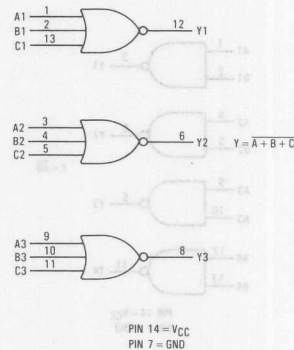
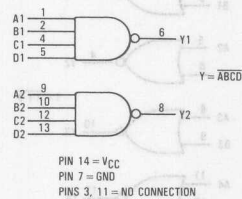


HC10

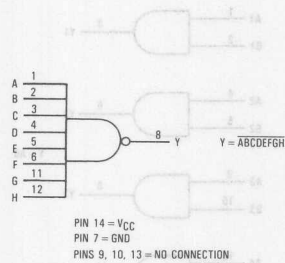


HC11

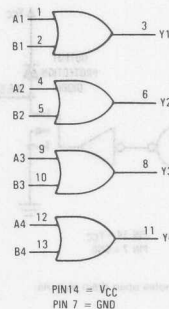




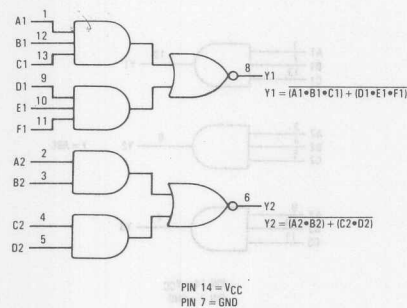
HC30



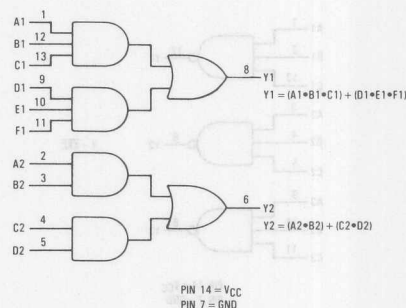
HC32



HC51

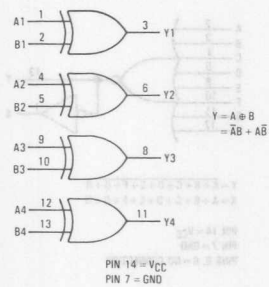


HC58

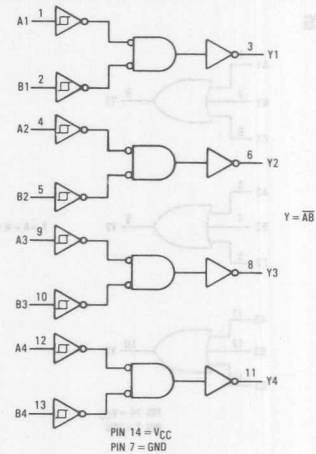


(b) GATES (Continued)

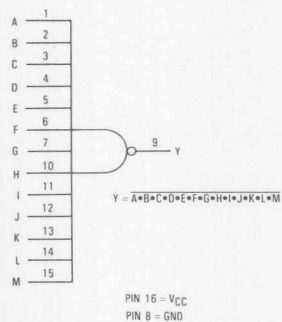
HC86



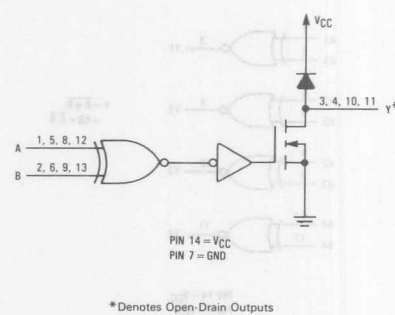
HC132



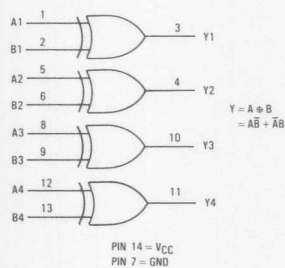
HC133



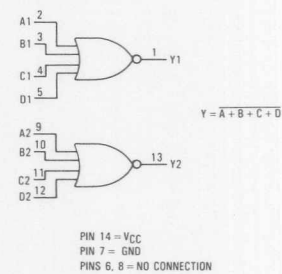
HC266



HC386



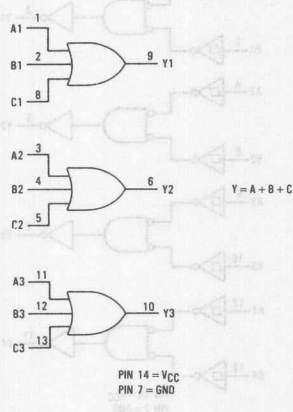
HC4002



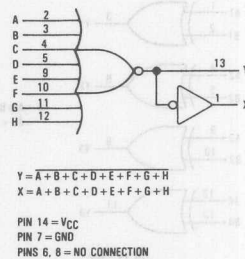
(b) GATES (Continued)

2

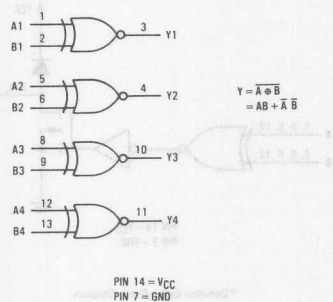
HC4075



HC4078



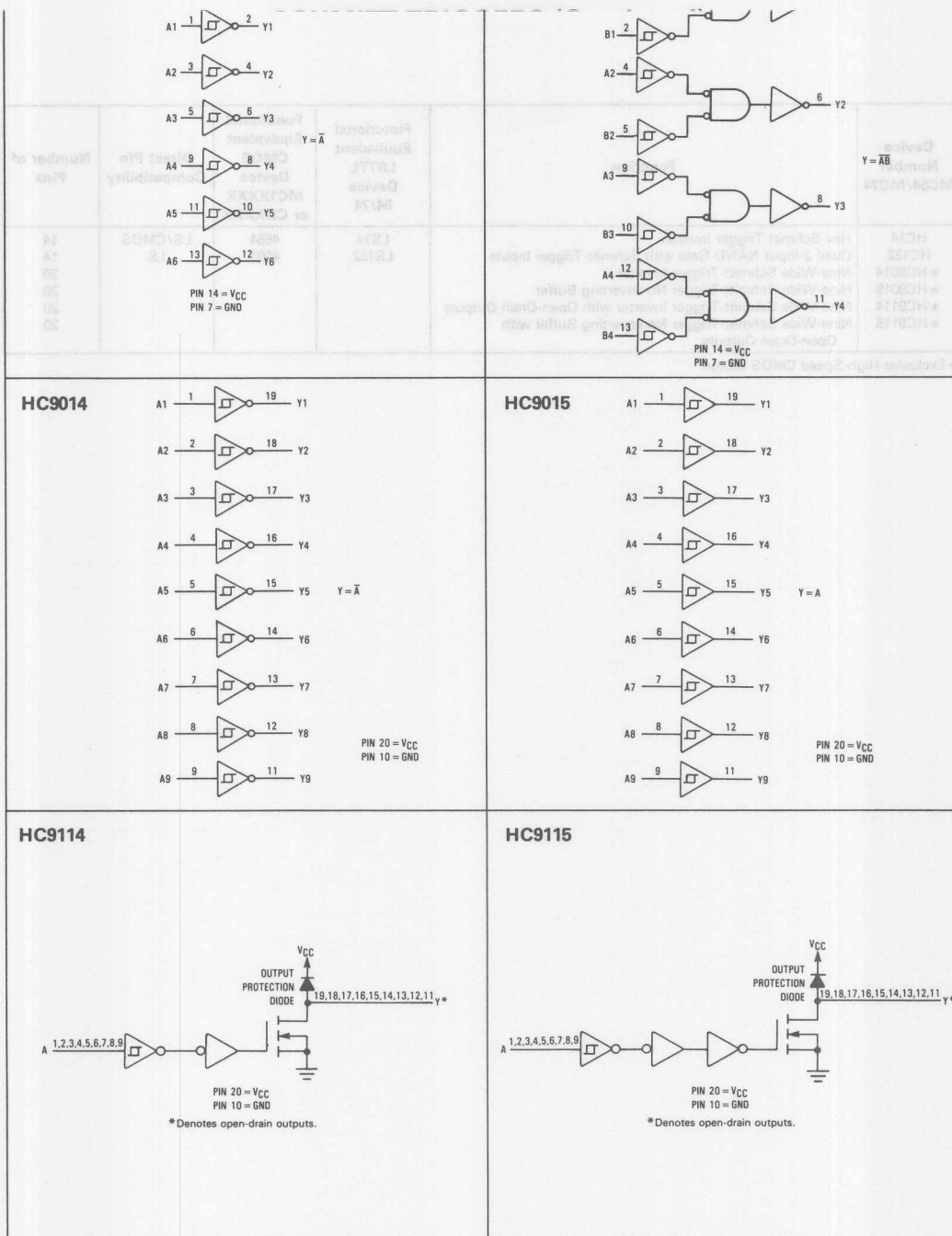
HC7266



SCHMITT TRIGGERS

		Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
Device Number MC54/MC74						
HC14	Hex Schmitt-Trigger Inverter		LS14	4584	LS/CMOS	14
HC132	Quad 2-Input NAND Gate with Schmitt-Trigger Inputs		LS132	4093	LS	14
★ HC9014	Nine-Wide Schmitt-Trigger Inverter					20
★ HC9015	Nine-Wide Schmitt-Trigger Noninverting Buffer					20
★ HC9114	Nine-Wide Schmitt-Trigger Inverter with Open-Drain Outputs					20
★ HC9115	Nine-Wide Schmitt-Trigger Noninverting Buffer with Open-Drain Outputs					20

★ Exclusive High-Speed CMOS design



BUS TRANSCEIVERS

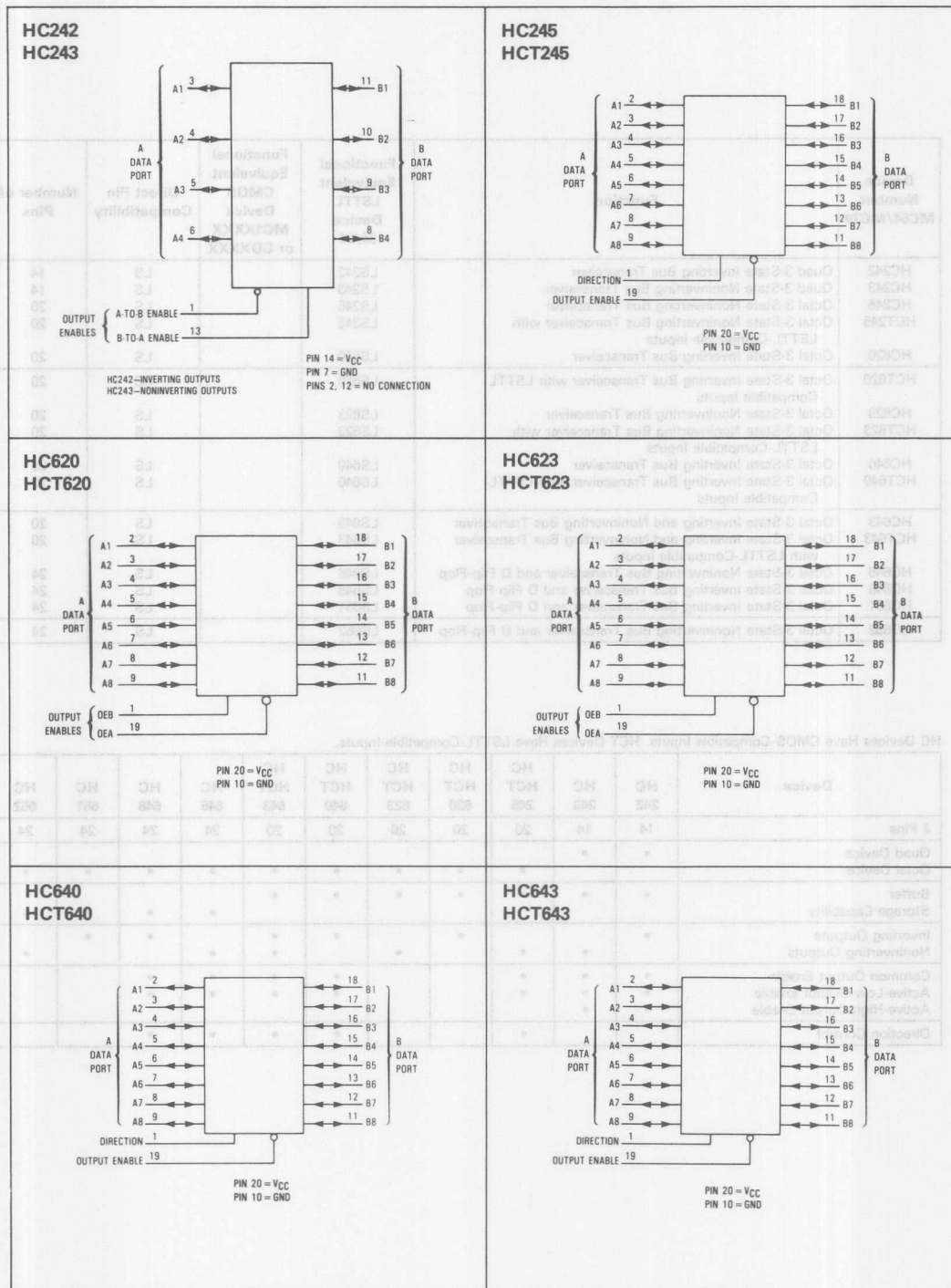
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC242	Quad 3-State Inverting Bus Transceiver	LS242		LS	14
HC243	Quad 3-State Noninverting Bus Transceiver	LS243		LS	14
HC245	Octal 3-State Noninverting Bus Transceiver	LS245		LS	20
HCT245	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS245		LS	20
HC620	Octal 3-State Inverting Bus Transceiver	LS620		LS	20
HCT620	Octal 3-State Inverting Bus Transceiver with LSTTL- Compatible Inputs	LS620		LS	20
HC623	Octal 3-State Noninverting Bus Transceiver	LS623		LS	20
HCT623	Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS623		LS	20
HC640	Octal 3-State Inverting Bus Transceiver	LS640		LS	20
HCT640	Octal 3-State Inverting Bus Transceiver with LSTTL- Compatible Inputs	LS640		LS	20
HC643	Octal 3-State Inverting and Noninverting Bus Transceiver	LS643		LS	20
HCT643	Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs	LS643		LS	20
HC646	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS646		LS	24
HC648	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	LS648		LS	24
HC651	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	LS651		LS	24
HC652	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS652		LS	24

HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

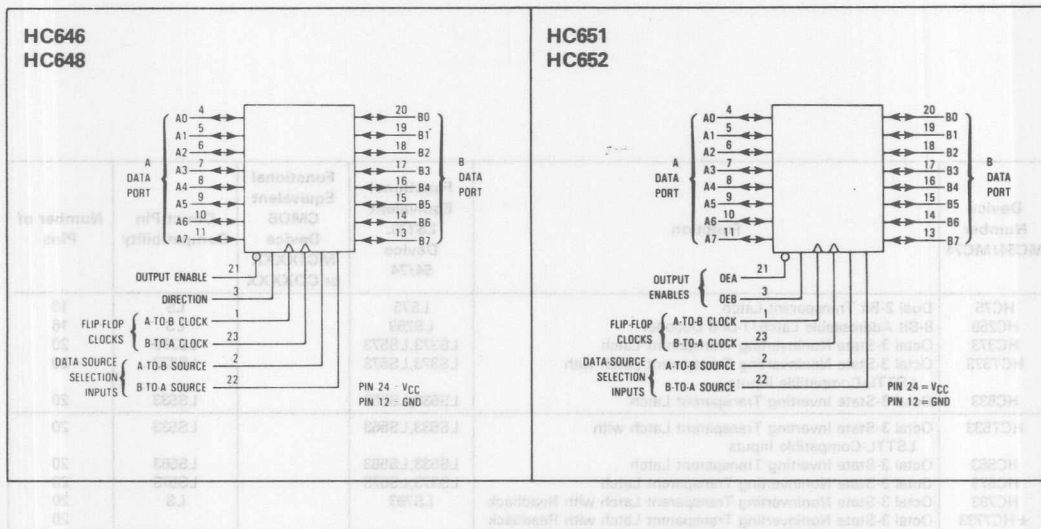
Device	HC 242	HC 243	HC HCT 245	HC HCT 620	HC HCT 623	HC HCT 640	HC HCT 643	HC 646	HC 648	HC 651	HC 652
# Pins	14	14	20	20	20	20	20	24	24	24	24
Quad Device	•	•									
Octal Device			•	•	•	•	•	•	•	•	•
Buffer	•	•	•	•	•	•	•	•	•	•	•
Storage Capability											
Inverting Outputs	•	•	•	•	•	•	•	•	•	•	•
Noninverting Outputs					•						•
Common Output Enable	•	•	•			•	•	•	•		
Active-Low Output Enable	•	•	•			•	•	•	•		
Active-High Output Enable	•	•									
Direction Control			•			•	•	•	•		

BUS TRANSCEIVERS (Continued)

2



BUS TRANSCEIVERS (Continued)



2

Device	HC 74	HC 74B	HC 74C	HC 74D	HC 74E	HC 74F	HC 74G	HC 74H	HC 74J	HC 74K	HC 74L	HC 74M	HC 74N	HC 74P	HC 74Q	HC 74R	HC 74S	HC 74T	HC 74U	HC 74V	HC 74W	HC 74X	HC 74Y	HC 74Z
Number of Bits Controlled by Each Input	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
Number of Bits Controlled by Each Output	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
Number of Bits Controlled by Each Input/Output	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
Number of Bits Controlled by Each Input/Output (Total)	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
Number of Bits Controlled by Each Input/Output (Total) (Continued)	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC75	Dual 2-Bit Transparent Latch	LS75		LS	16
HC259	8-Bit Addressable Latch/1-of-8 Decoder	LS259		LS	16
HC373	Octal 3-State Noninverting Transparent Latch	LS373,LS573		LS373	20
HCT373	Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs	LS373,LS573		LS373	20
HC533	Octal 3-State Inverting Transparent Latch	LS533,LS563		LS533	20
HCT533	Octal 3-State Inverting Transparent Latch with LSTTL-Compatible Inputs	LS533,LS563		LS533	20
HC563	Octal 3-State Inverting Transparent Latch	LS533,LS563		LS563	20
HC573	Octal 3-State Noninverting Transparent Latch	LS373,LS573		LS573	20
HC793	Octal 3-State Noninverting Transparent Latch with Readback	LS793		LS	20
★HC7793	Octal 3-State Noninverting Transparent Latch with Readback				20

★ Exclusive High-Speed CMOS design

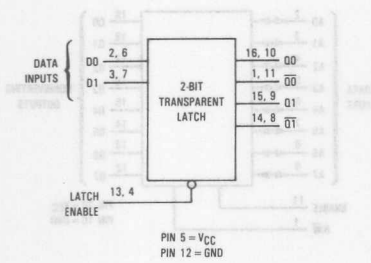
HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HC 75	HC 259	HC HCT 373	HC HCT 533	HC 563	HC 573	HC 793	HC 7793
# Pins	16	16	20	20	20	20	20	20
Single Device	•	•	•	•	•	•	•	•
Dual Device	•	•	•	•	•	•	•	•
Octal Device	•	•	•	•	•	•	•	•
Number of Bits Controlled by Latch Enable: 2 8	•	•	•	•	•	•	•	•
Transparent Addressable Readback Capability	•	•	•	•	•	•	•	•
Noninverting Outputs	•	•	•	•	•	•	•	•
Inverting Outputs	•	•	•	•	•	•	•	•
Common Latch Enable, Active-Low	•	•	•	•	•	•	•	•
3-State Outputs	•	•	•	•	•	•	•	•
Common Output Enable, Active-Low	•	•	•	•	•	•	•	•

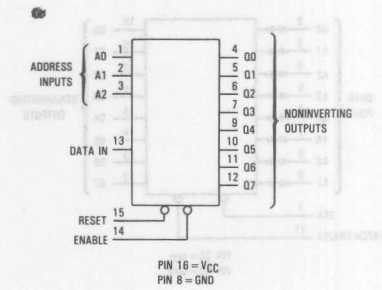
These devices are identical in function and are different in pinout only: HC/HCT373 and HC573
HC/HCT533 and HC563

LATCHES (Continued)

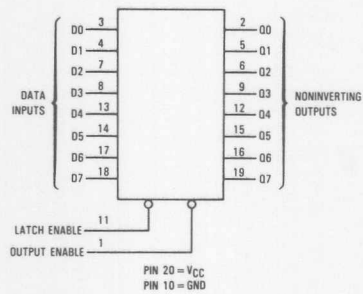
HC75



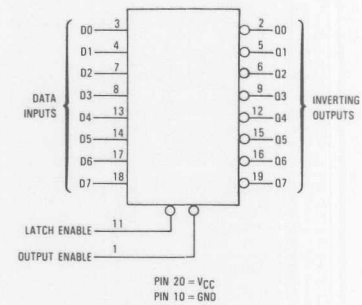
HC259



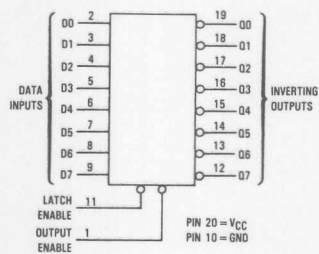
HC373
HCT373



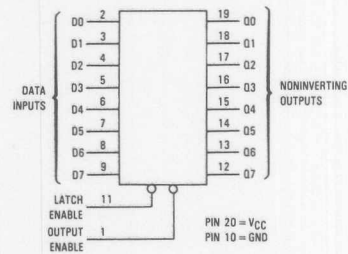
HC533
HCT533



HC563

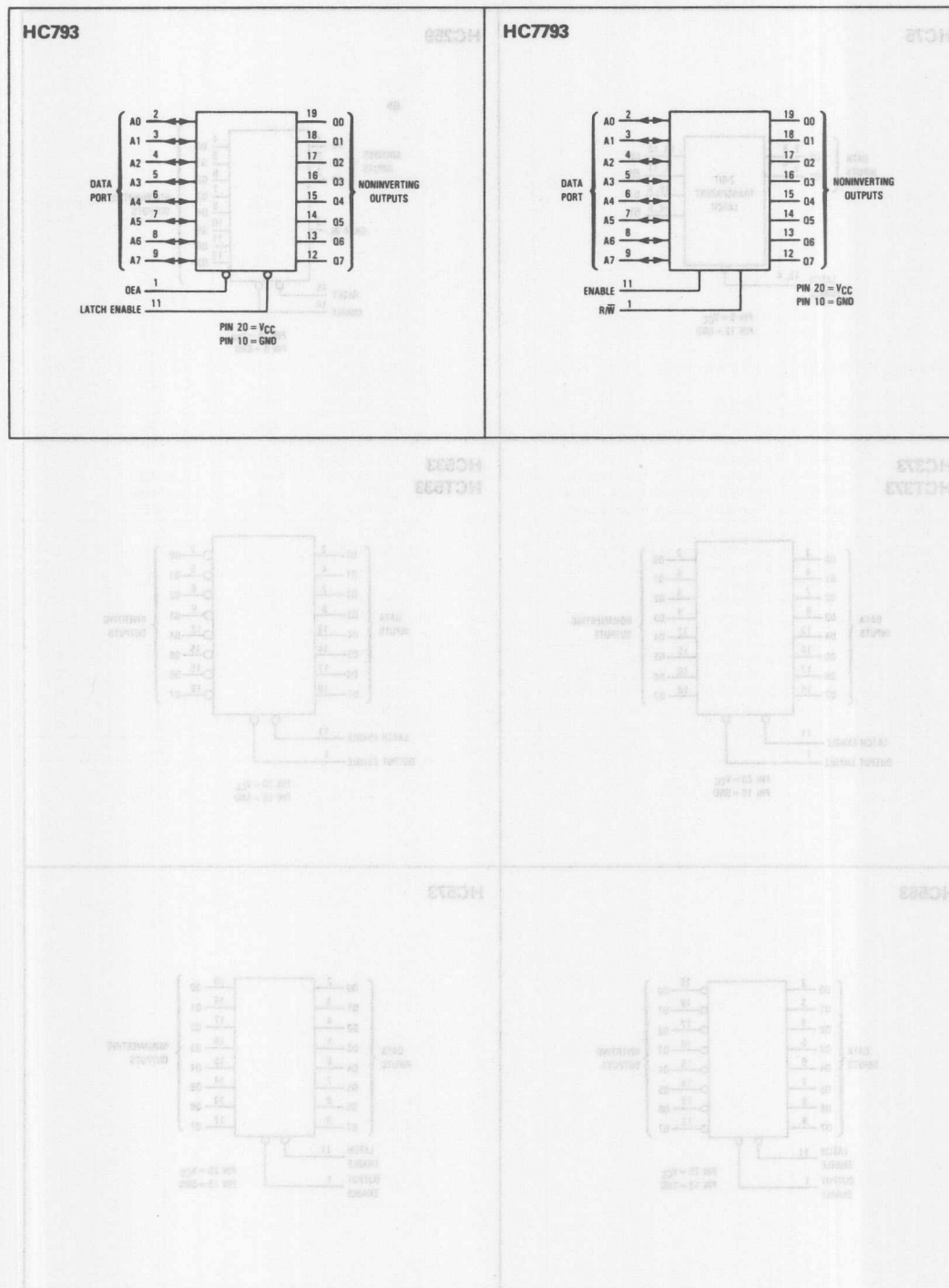


HC573



LATCHES (Continued)

2



FLIP-FLOPS

Device Number	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
MC54/MC74					
HC73	Dual J-K Flip-Flop with Reset	LS73,LS73A, LS107,LS107A	*4027	LS73, LS73A	14
HC74	Dual D Flip-Flop with Set and Reset	LS74,LS74A	*4013	LS	14
HC76	Dual J-K Flip-Flop with Set and Reset	LS76,LS76A, LS112,LS112A	*4027	LS76, LS76A	16
HC107	Dual J-K Flip-Flop with Reset	LS73,LS73A, LS107,LS107A	*4027	LS107, LS107A	14
HC109	Dual J-K Flip-Flop with Set and Reset	LS109,LS109A	*4027	LS	16
HC112	Dual J-K Flip-Flop with Set and Reset	LS76,LS76A, LS112,LS112A	*4027	LS112, LS112A	16
HC113	Dual J-K Flip-Flop with Set	LS113,LS113A	*4027	LS	14
HC173	Quad 3-State D Flip-Flop with Common Clock and Reset	LS173,LS173A	4076	LS/CMOS	16
HC174	Hex D Flip-Flop with Common Clock and Reset	LS174	4174	LS/CMOS	16
HC175	Quad D Flip-Flop with Common Clock and Reset	LS175	4175	LS/CMOS	16
HC273	Octal D Flip-Flop with Common Clock and Reset	LS273		LS	20
HC374	Octal 3-State Noninverting D Flip-Flop	LS374,LS574		LS374	20
HCT374	Octal 3-State Noninverting D Flip-Flop with LSTTL-Compatible Inputs	LS374,LS574		LS374	20
HC534	Octal 3-State Inverting D Flip-Flop	LS534,LS564		LS534	20
HCT534	Octal 3-State Inverting D Flip-Flop with LSTTL-Compatible Inputs	LS534,LS564		LS534	20
HC564	Octal 3-State Inverting D Flip-Flop	LS534,LS564		LS564	20
HC574	Octal 3-State Noninverting D Flip-Flop	LS374,LS574		LS574	20
HC646	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS646		LS	24
HC648	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	LS648		LS	24
HC651	Octal 3-State Inverting Bus Transceiver and D Flip-Flop	LS651		LS	24
HC652	Octal 3-State Noninverting Bus Transceiver and D Flip-Flop	LS652		LS	24

*Suggested alternative

Device	HC 73	HC 74	HC 76	HC 107	HC 109	HC 112	HC 113	HC 173	HC 174	HC 175
# Pins	14	14	16	14	16	16	14	16	16	16
Type	J-K	D	J-K	J-K	J-K	J-K	J-K	D	D	D
Dual Device	•	•	•	•	•	•	•	•	•	•
Quad Device										
Hex Device									•	•
Octal Device										
Common Clock										
Negative-Transition Clocking	•		•	•	•	•	•	•	•	•
Positive-Transition Clocking		•			•			•	•	•
Common, Active-Low Data Enables										
Noninverting Outputs	•	•	•	•	•	•	•	•	•	•
Inverting Outputs	•	•	•	•	•	•	•	•	•	•
3-State Outputs								•		
Common, Active-Low Output Enables								•		
Common Reset									•	•
Active-Low Reset	•	•	•	•	•	•	•	•	•	•
Active-High Reset										
Active-Low Set		•	•		•	•	•			
Transceiver										
Direction Control										

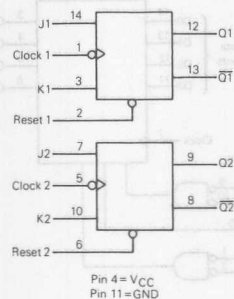
HC Devices Have CMOS-Compatible Inputs. HCT Devices Have LSTTL-Compatible Inputs.

Device	HC 273	HC HCT 374	HC HCT 534	HC 564	HC 574	HC 646	HC 648	HC 651	HC 652
# Pins	20	20	20	20	20	24	24	24	24
Type	D	D	D	D	D	D	D	D	D
Dual Device									
Quad Device									
Hex Device	•	•	•	•	•	•	•	•	•
Octal Device									
Common Clock	•	•	•	•	•	•	•	•	•
Negative-Transition Clocking	•	•	•	•	•	•	•	•	•
Positive-Transition Clocking									
Common, Active-Low Data Enables									
Noninverting Outputs	•	•	•	•	•	•	•	•	•
Inverting Outputs			•	•	•	•	•	•	•
3-State Outputs		•	•	•	•	•	•	•	•
Common, Active-Low Output Enables		•	•	•	•	•	•	•	•
Common Reset	•								
Active-Low Reset	•								
Active-High Reset									
Active-Low Set									
Transceiver						•	•	•	•
Direction Control						•	•	•	•

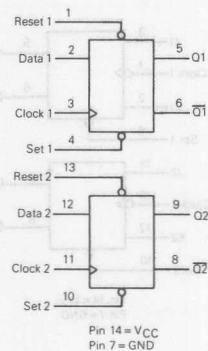
These devices are identical in function and are different in pinout only: HC73 and HC107
 HC76 and HC112
 HC374 and HC574
 HC534 and HC564

FLIP-FLOPS (Continued)

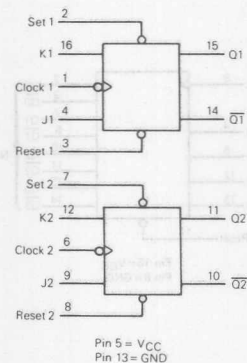
HC73



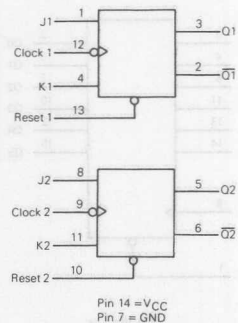
HC74



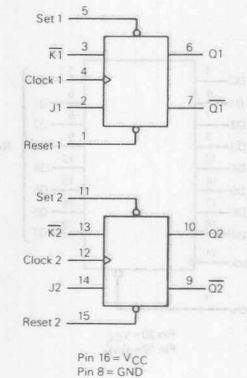
HC76



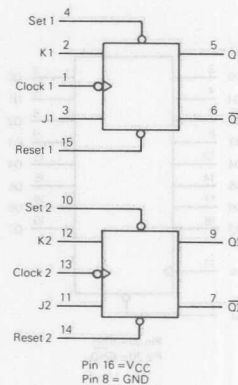
HC107



HC109



HC112

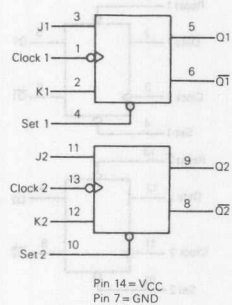


2

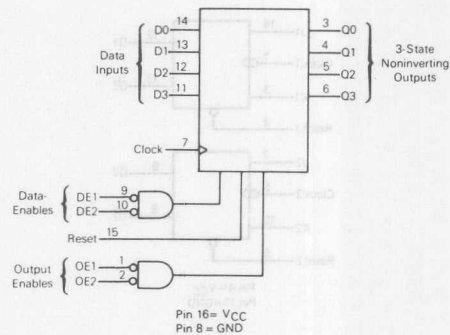
FLIP-FLOPS (Continued)

2

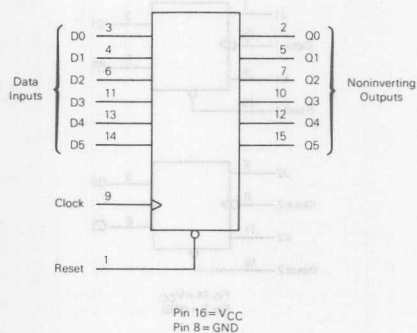
HC113



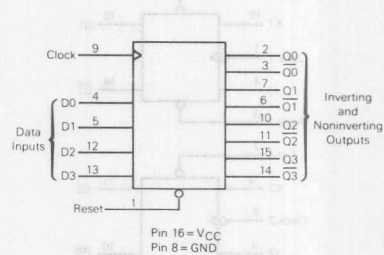
HC173



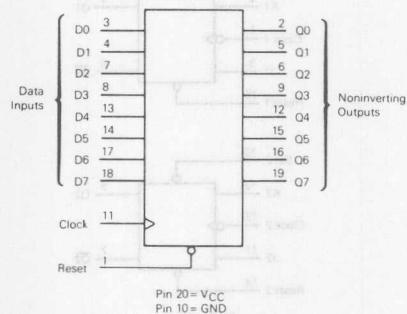
HC174



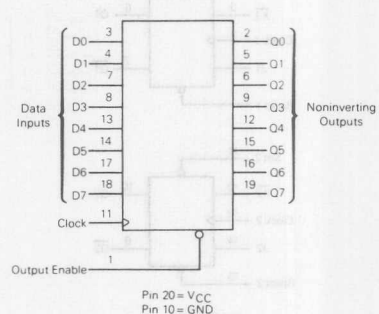
HC175



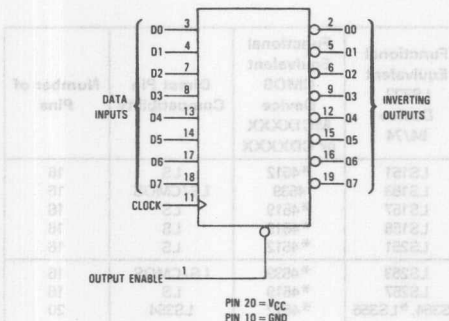
HC273



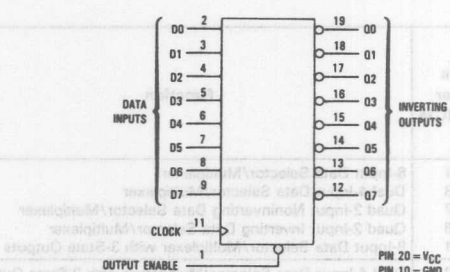
HC374
HCT374



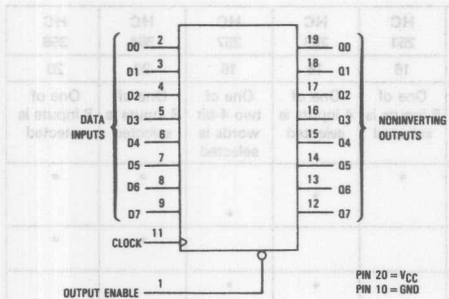
**HC534
HCT534**



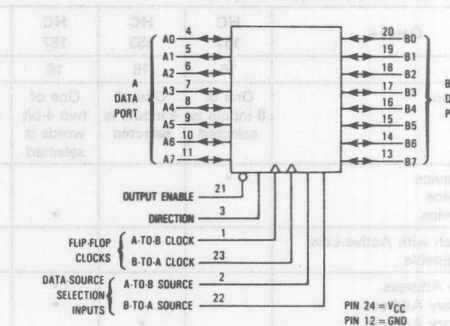
HC564



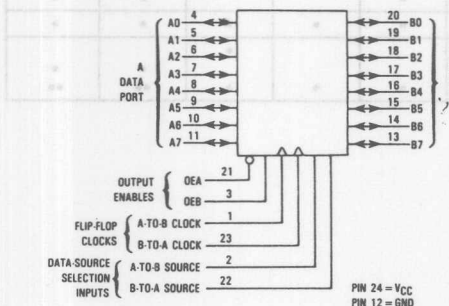
HC574



**HC646
HC648**



**HC651
HC652**



Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC151	8-Input Data Selector/Multiplexer	LS151	*4512	LS	16
HC153	Dual 4-Input Data Selector/Multiplexer	LS153	4539	LS/CMOS	16
HC157	Quad 2-Input Noninverting Data Selector/Multiplexer	LS157	*4519	LS	16
HC158	Quad 2-Input Inverting Data Selector/Multiplexer	LS158	*4519	LS	16
HC251	8-Input Data Selector/Multiplexer with 3-State Outputs	LS251	*4512	LS	16
HC253	Dual 4-Input Data Selector/Multiplexer with 3-State Outputs	LS253	*4539	LS/CMOS	16
HC257	Quad 2-Input Data Selector/Multiplexer with 3-State Outputs	LS257	*4519	LS	16
HC354	8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs	LS354,*LS356	*4512	LS354	20
HC356	8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs	*LS354,LS356	*4512	LS356	20

*Suggested alternative

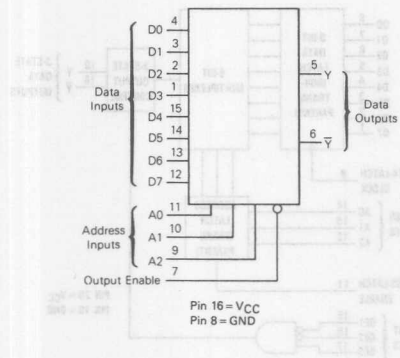
HC Devices Have CMOS-Compatible Inputs.

Device	HC 151	HC 153	HC 157	HC 158	HC 251	HC 253	HC 257	HC 354	HC 356
# Pins	16	16	16	16	16	16	16	20	20
Description	One of 8 inputs is selected	One of 4 inputs is selected	One of two 4-bit words is selected	One of two 4-bit words is selected	One of 8 inputs is selected	One of 4 inputs is selected	One of two 4-bit words is selected	One of 8 inputs is selected	One of 8 inputs is selected
Single Device	•	•	•	•	•	•	•	•	•
Dual Device	•	•	•	•	•	•	•	•	•
Quad Device	•	•	•	•	•	•	•	•	•
Data Latch with Active-Low Latch Enable	•	•	•	•	•	•	•	•	•
Common Address	•	•	•	•	•	•	•	•	•
1-Bit Binary Address	•	•	•	•	•	•	•	•	•
2-Bit Binary Address	•	•	•	•	•	•	•	•	•
3-Bit Binary Address	•	•	•	•	•	•	•	•	•
Address Latch (Transparent)	•	•	•	•	•	•	•	•	•
Address Latch (Non-transparent)	•	•	•	•	•	•	•	•	•
Active-Low Address Latch Enable	•	•	•	•	•	•	•	•	•
Noninverting Output	•	•	•	•	•	•	•	•	•
Inverting Output	•	•	•	•	•	•	•	•	•
3-State Outputs	•	•	•	•	•	•	•	•	•
Common Output Enable	•	•	•	•	•	•	•	•	•
Active-High Output Enable	•	•	•	•	•	•	•	•	•
Active-Low Output Enable	•	•	•	•	•	•	•	•	•

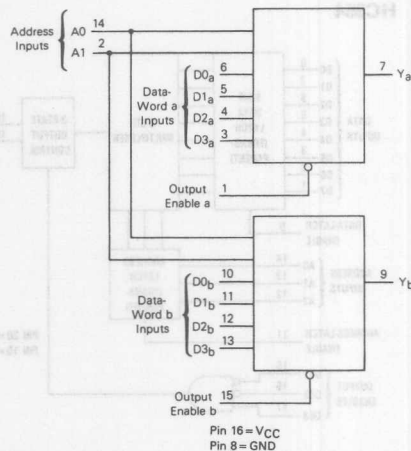
••implies the device has two such enables

DIGITAL DATA SELECTORS/MULTIPLEXERS (Continued)

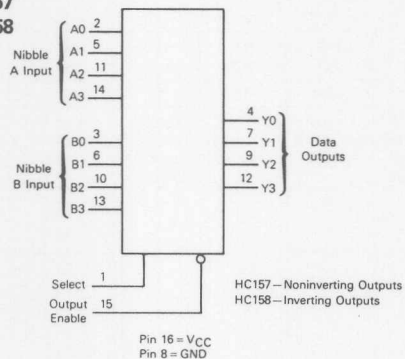
HC151



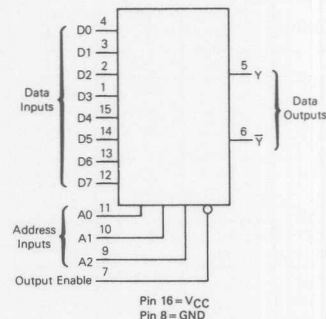
HC153



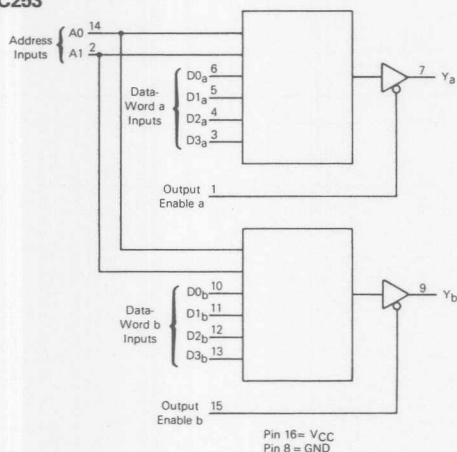
**HC157
HC158**



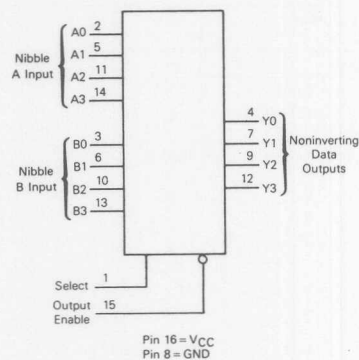
HC251



HC253

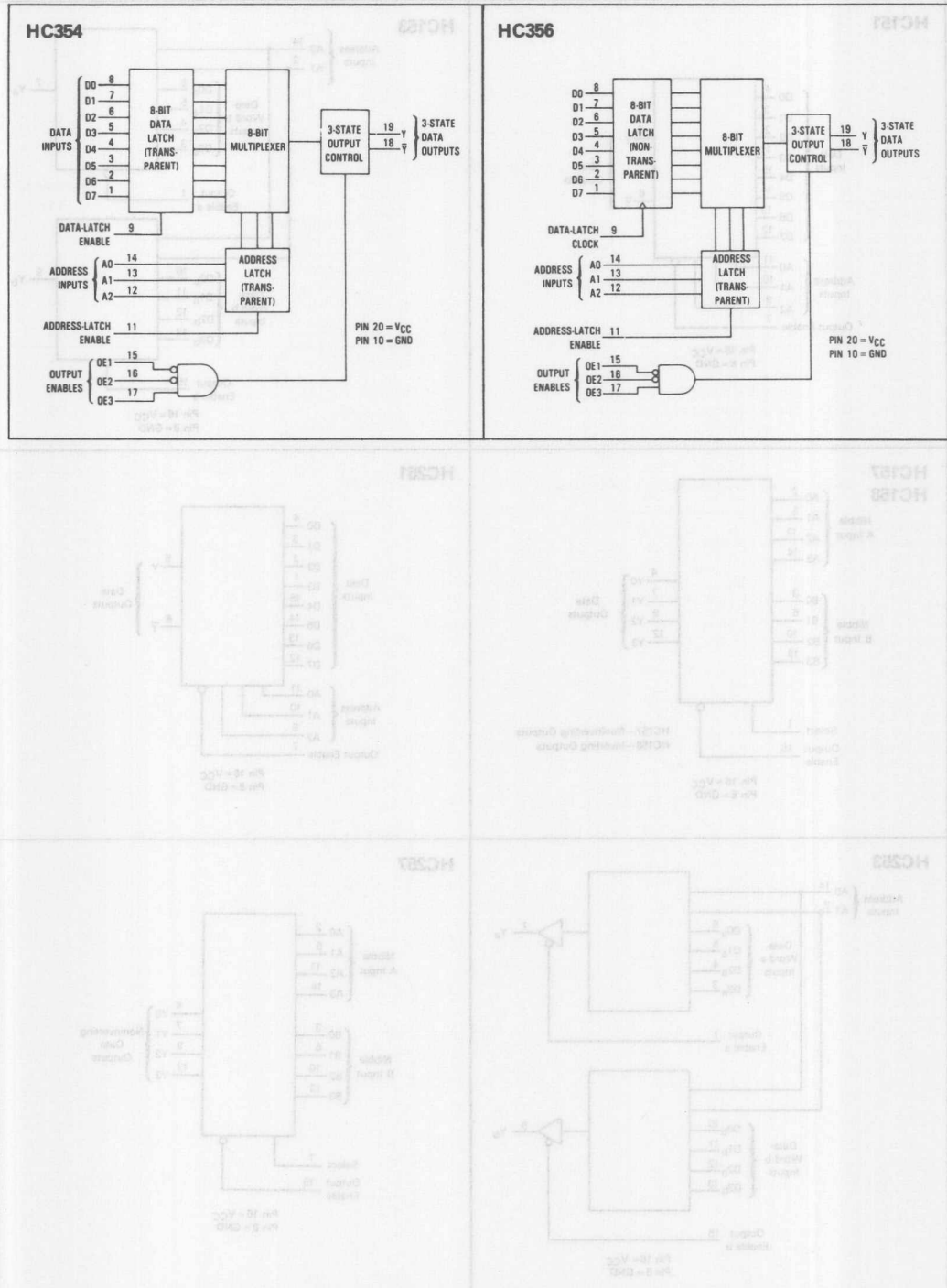


HC257



(b) DIGITAL DATA SELECTORS/MULTIPLEXERS (Continued)

2



DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS

Device	HC 42	HC 137	HC 138	HC 139	HC 154	HC 237	HC 259	HC 4511	HC 4514	HC 4543
Pin	16	16	16	16	16	16	16	16	16	16
Input Description	BCD Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address
Output Description	1-of-10 Decoder	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer
Functional Equivalent LSTTL Device	LS42	LS137	LS138	LS139	LS154	*LS159	*LS137	*LS137	*LS137	*LS137
Functional Equivalent CMOS Device	*4028	*4028	*4028	4556	*4515	*4028	4511	4514	*4515	4543
Direct Pin Compatibility	LS	LS	LS	LS/CMOS	LS	LS	CMOS	CMOS	CMOS	CMOS
Number of Pins	16	16	16	16	24	16	16	16	24	16
Device Number	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74
Function	1-of-10 Decoder	1-of-8 Decoder/Demultiplexer with Address Latch	1-of-8 Decoder/Demultiplexer	Dual 1-of-4 Decoder/Demultiplexer	Decimal-to-BCD Encoder	1-of-16 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer with Address Latch	8-Bit Addressable Latch/1-of-8 Decoder	BCD-to-Seven-Segment Latch/Decoder/Display Driver	BCD-to-Seven-Segment Latch/Decoder/Display Driver for LCDs

*Suggested alternative

★ Exclusive High-Speed CMOS design

Device	HC 42	HC 137	HC 138	HC 139	HC 154	HC 237	HC 259	HC 4511	HC 4514	HC 4543
Pin	16	16	16	16	16	16	16	16	16	16
Input Description	BCD Data	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address	3-Bit Binary Address
Output Description	1-of-10 Decoder	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer
Functional Equivalent LSTTL Device	LS42	LS137	LS138	LS139	LS154	*LS159	*LS137	*LS137	*LS137	*LS137
Functional Equivalent CMOS Device	*4028	*4028	*4028	4556	*4515	*4028	4511	4514	*4515	4543
Direct Pin Compatibility	LS	LS	LS	LS/CMOS	LS	LS	CMOS	CMOS	CMOS	CMOS
Number of Pins	16	16	16	16	24	16	16	16	24	16
Device Number	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74	MC54/MC74
Function	1-of-10 Decoder	1-of-8 Decoder/Demultiplexer with Address Latch	1-of-8 Decoder/Demultiplexer	Dual 1-of-4 Decoder/Demultiplexer	Decimal-to-BCD Encoder	1-of-16 Decoder/Demultiplexer	1-of-8 Decoder/Demultiplexer with Address Latch	8-Bit Addressable Latch/1-of-8 Decoder	BCD-to-Seven-Segment Latch/Decoder/Display Driver	BCD-to-Seven-Segment Latch/Decoder/Display Driver for LCDs

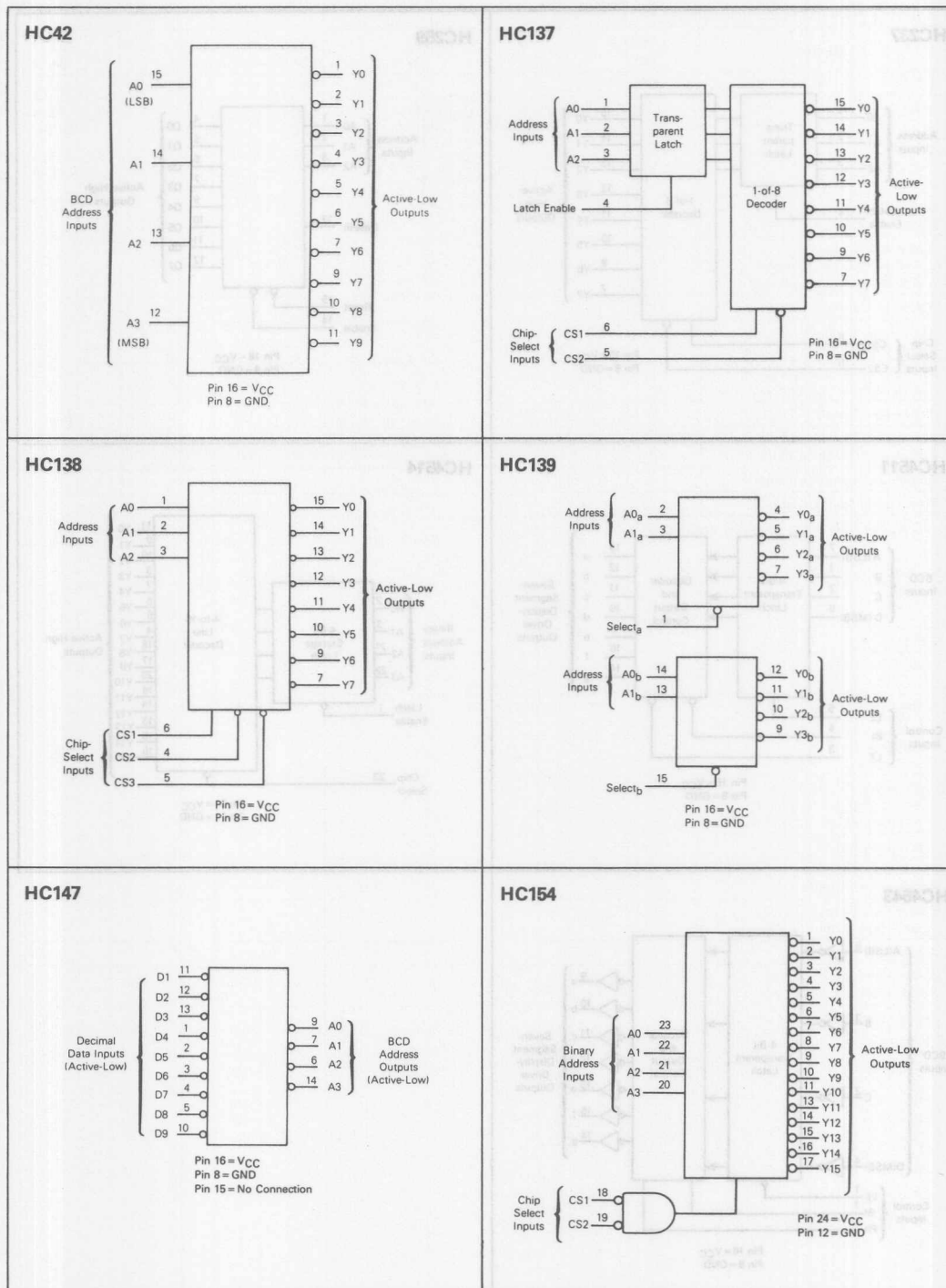
Device	HC 42	HC 137	HC 138	HC 139	HC 147	HC 154
# Pins	16	16	16	16	16	24
Input Description	BCD Address	3-Bit Binary Address	3-Bit Binary Address	2-Bit Binary Address	Any Combination of 9 Inputs	4-Bit Binary Address
Output Description	One of 10	One of 8	One of 8	One of 4	BCD Address of Highest Input	One of 16
Single Device Dual Device	• •	• •	• •	• •	• •	• •
Address Input Latch Active-High Latch Enable Active-Low Latch Enable		• •				
Active-Low Inputs				•	•	
Active-Low Outputs Active-High Outputs	• •	• •	• •	• •	• •	• •
Active-Low Output Enable Active-High Output Enable		• •	• •	• •	• •	• •
Active-Low Reset						
Active-Low Blanking Input Active-High Blanking Input						
Active-Low Lamp-Test Input						
Phase Input (for LCD's)						

••implies the device has two such enables

HC Devices Have CMOS-Compatible Inputs.

Device	HC 237	HC 259	HC 4511	HC 4514	HC 4543
# Pins	16	16	16	24	16
Input Description	3-Bit Binary Address	3-Bit Binary Address	BCD Data	4-Bit Binary Address	BCD Data
Output Description	One of 8	One of 8	7-Segment Display	One of 16	7-Segment Display
Single Device Dual Device	• •	• •	• •	• •	• •
Address Input Latch Active-High Latch Enable Active-Low Latch Enable	• •	• •	• •	• •	• •
Active-Low Inputs					
Active-Low Outputs Active-High Outputs	• •	• •	• •	• •	• •
Active-Low Output Enable Active-High Output Enable	• •	• •	• •	• •	• •
Active-Low Reset		•			
Active-Low Blanking Input Active-High Blanking Input			• •		• •
Active-Low Lamp Test Input			•		
Phase Input (for LCD's)					•

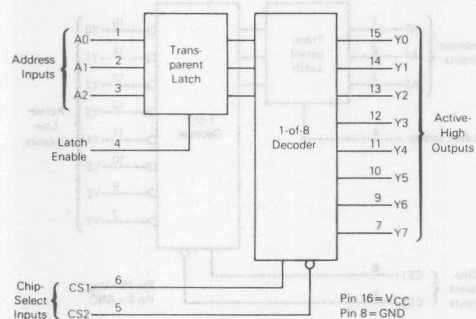
DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS (Continued)



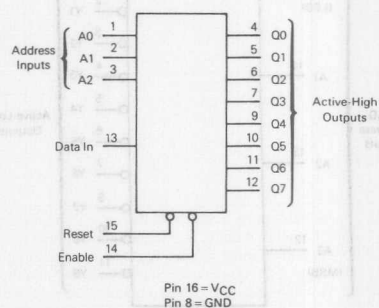
DECODERS/DEMULTIPLEXERS/DISPLAY DRIVERS (Continued)

2

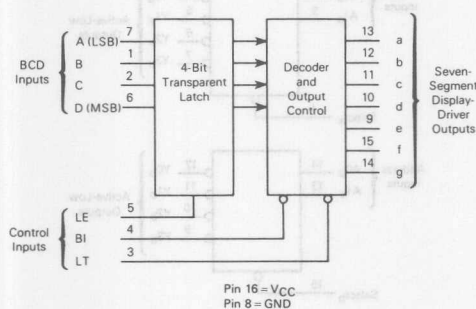
HC237



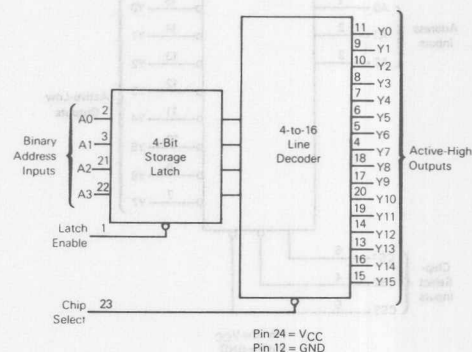
HC259



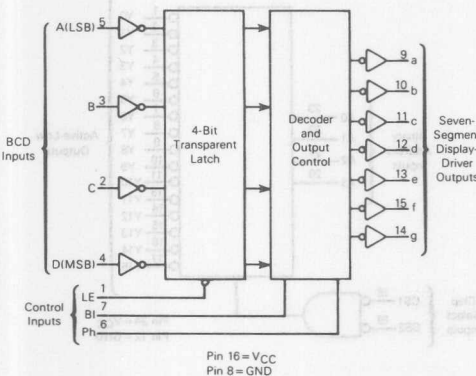
HC4511



HC4514



HC4543



ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS

Device Number	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
MC54/MC74					
HC4016	Quad Analog Switch/Multiplexer/Demultiplexer		4016, 4066	CMOS	14
HC4051	8-Channel Analog Multiplexer/Demultiplexer		4051	CMOS	16
HC4052	Dual 4-Channel Analog Multiplexer/Demultiplexer		4052	CMOS	16
HC4053	Triple 2-Channel Analog Multiplexer/Demultiplexer		4053	CMOS	16
HC4066	Quad Analog Switch/Multiplexer/Demultiplexer		4066, 4016	CMOS	14
★ HC4316	Quad Analog Switch/Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies		*4016		16
★ HC4351	8-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4051		20
★ HC4352	Dual 4-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4052		20
★ HC4353	Triple 2-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4053		20

*Suggested alternative

★ High-Speed CMOS design only

Device	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
MC54/MC74					
HC4016	Quad Analog Switch/Multiplexer/Demultiplexer		4016, 4066	CMOS	14
HC4051	8-Channel Analog Multiplexer/Demultiplexer		4051	CMOS	16
HC4052	Dual 4-Channel Analog Multiplexer/Demultiplexer		4052	CMOS	16
HC4053	Triple 2-Channel Analog Multiplexer/Demultiplexer		4053	CMOS	16
HC4066	Quad Analog Switch/Multiplexer/Demultiplexer		4066, 4016	CMOS	14
★ HC4316	Quad Analog Switch/Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies		*4016		16
★ HC4351	8-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4051		20
★ HC4352	Dual 4-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4052		20
★ HC4353	Triple 2-Channel Analog Multiplexer/Demultiplexer with Address Latch		*4053		20

Device	HC 4016	HC 4051	HC 4052	HC 4053	HC 4066
# Pins	14	16	16	16	14
Description	4 Independently Controlled Switches	A 3-Bit Address Selects One of 8 Switches	A 2-Bit Address Selects One of 4 Switches	A 3-Bit Address Selects Varying Combinations of the 6 Switches	4 Independently Controlled Switches
Single Device		•			
Dual Device			•		
Triple Device				•	
Quad Device	•				•
1-to-1 Multiplexing	•				•
2-to-1 Multiplexing				•	
4-to-1 Multiplexing			•		
8-to-1 Multiplexing		•			
Active-High ON/OFF Control	•				•
Common Address Inputs			•	•	
2-Bit Binary Address			•	•	
3-Bit Binary Address		•			
Address Latch with Active-Low Latch Enable					
Common Switch Enable		•	•	•	
Active-Low Enable		•	•	•	
Active-High Enable					
Separate Analog and Control Reference Power Supplies		•	•		
Switched Tubes (for R_{ON} and Prop. Delay Improvement)					•

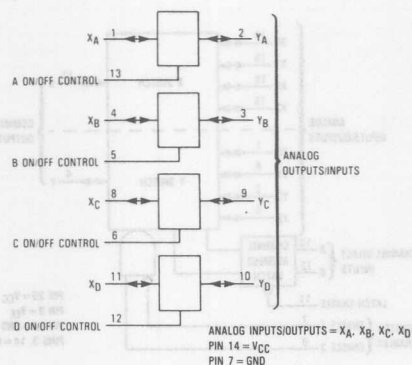
HC Devices Have CMOS-Compatible Inputs.

Device	HC 4316	HC 4351	HC 4352	HC 4353
# Pins	16	20	20	20
Description	4 Independently Controlled Switches (Has a Separate Analog Lower Power Supply)	A 3-Bit Address Selects One of 8 Switches (Has an Address Latch)	A 2-Bit Address Selects One of 4 Switches (Has an Address Latch)	A 3-Bit Address Selects Varying Combinations of the 6 Switches (Has an Address Latch)
Single Device		•		
Dual Device			•	
Triple Device	•			•
Quad Device				
1-to-1 Multiplexing	•			
2-to-1 Multiplexing				•
4-to-1 Multiplexing		•	•	
8-to-1 Multiplexing				
Active-High ON/OFF Control	•			
Common Address Inputs			•	•
2-Bit Binary Address			•	•
3-Bit Binary Address		•		•
Address Latch with Active-Low Latch Enable		•	•	•
Common Switch Enable	•	•	•	•
Active-Low Enable	•	•	•	•
Active-High Enable		•	•	•
Separate Analog and Control Reference Power Supplies	•	•	•	•
Switched Tubes (for R_{ON} and Prop. Delay Improvement)				

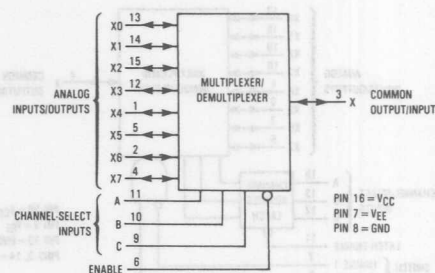
••implies the device has two such enables

ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS (Continued)

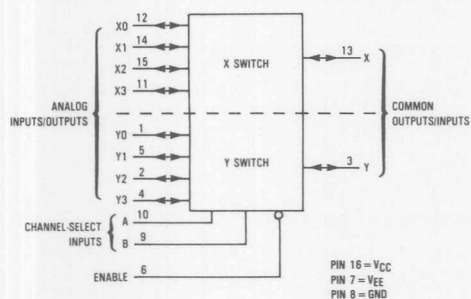
HC4016



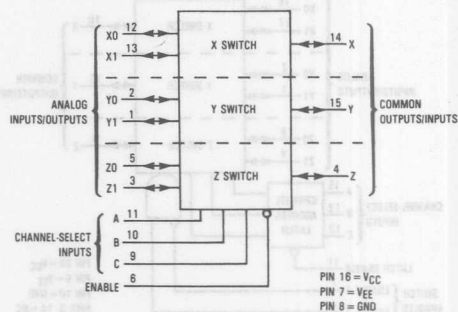
HC4051



HC4052

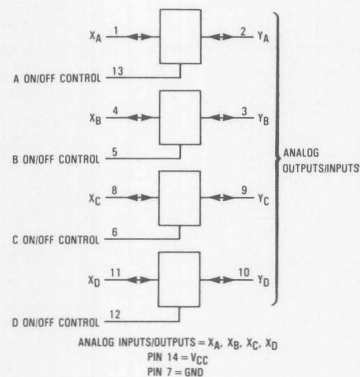


HC4053

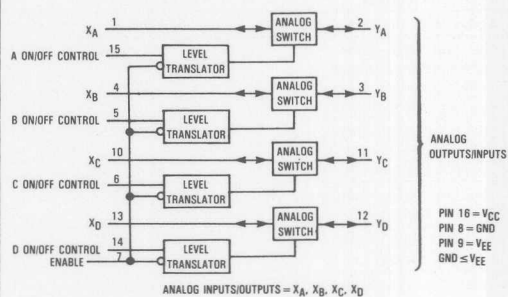


NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X Switch, Input B controls the Y Switch, and Input C controls the Z Switch.

HC4066



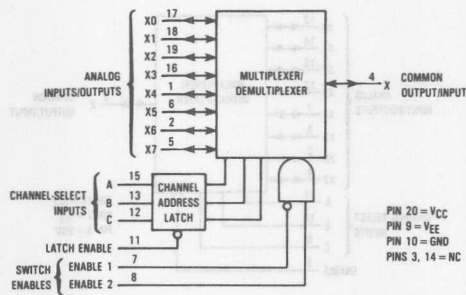
HC4316



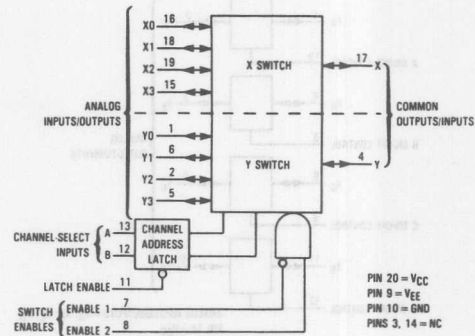
ANALOG SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS (Continued)

2

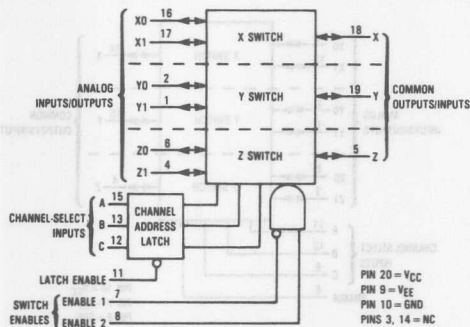
HC4351



HC4352



HC4353



NOTE:

This device allows independent control of each switch. Channel-Select Input A controls the X Switch, Input B controls the Y Switch, and Input C controls the Z Switch.

SHIFT REGISTERS

2

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC164	8-Bit Serial-Input/Parallel-Output Shift Register	LS164	*4034	LS	14
HC165	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register	LS165	*4021	LS	16
HC194	4-Bit Bidirectional Universal Shift Register	LS194, LS194A	4194	LS/CMOS	16
HC195	4-Bit Universal Shift Register	LS195, LS195A	*4035	LS	16
HC299	8-Bit Bidirectional Universal Shift Register with Parallel I/O	LS299		LS	20
HC589	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with 3-State Output	LS589		LS	16
HC595	8-Bit Serial-Input/Serial- or Parallel-Output Shift Register with Latched 3-State Outputs	LS595	*4034	LS	16
HC597	8-Bit Serial- or Parallel-Input/Serial-Output Shift Register with Input Latch	LS597		LS	16

*Suggested alternative

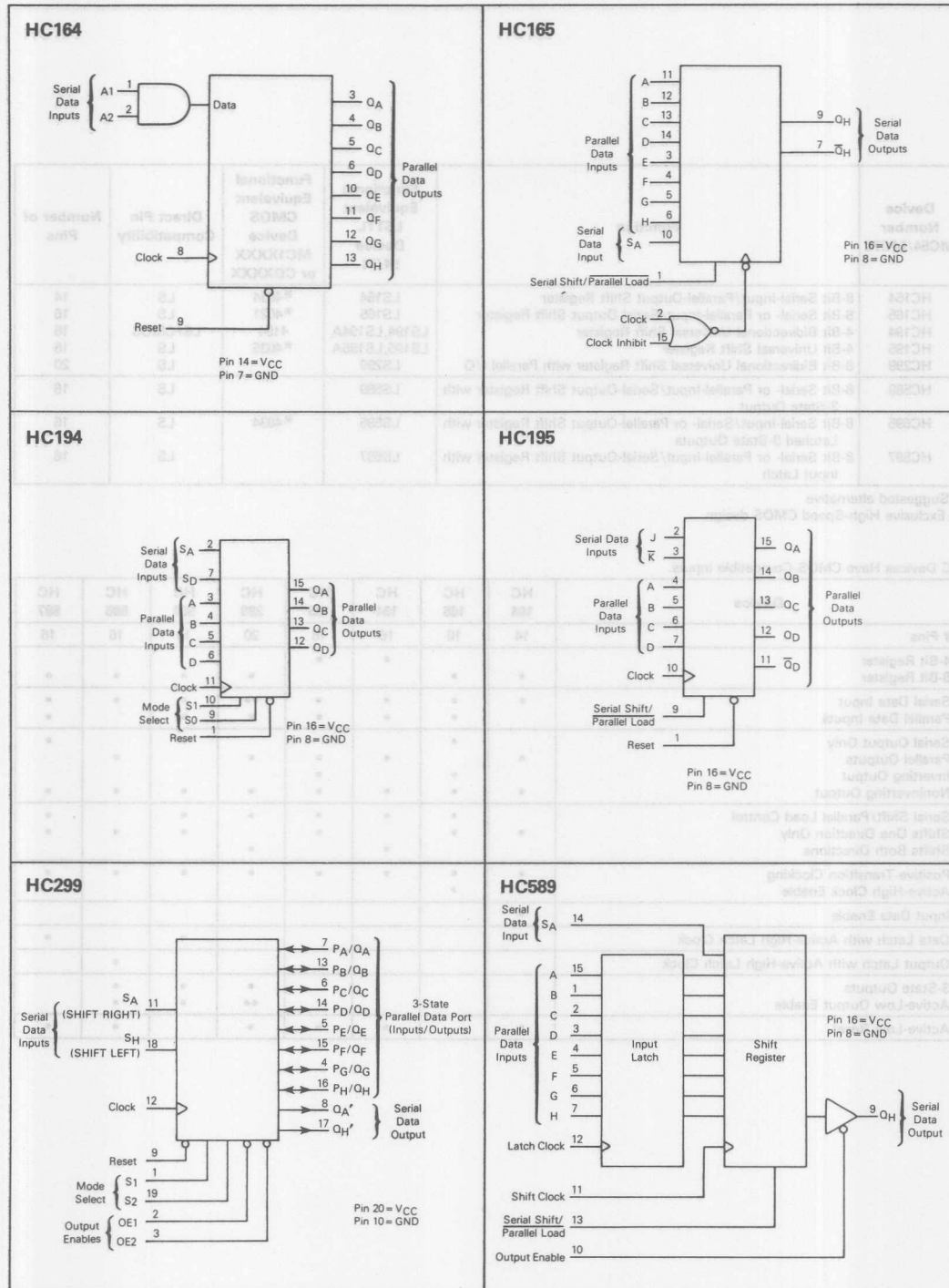
★ Exclusive High-Speed CMOS design

HC Devices Have CMOS-Compatible Inputs.

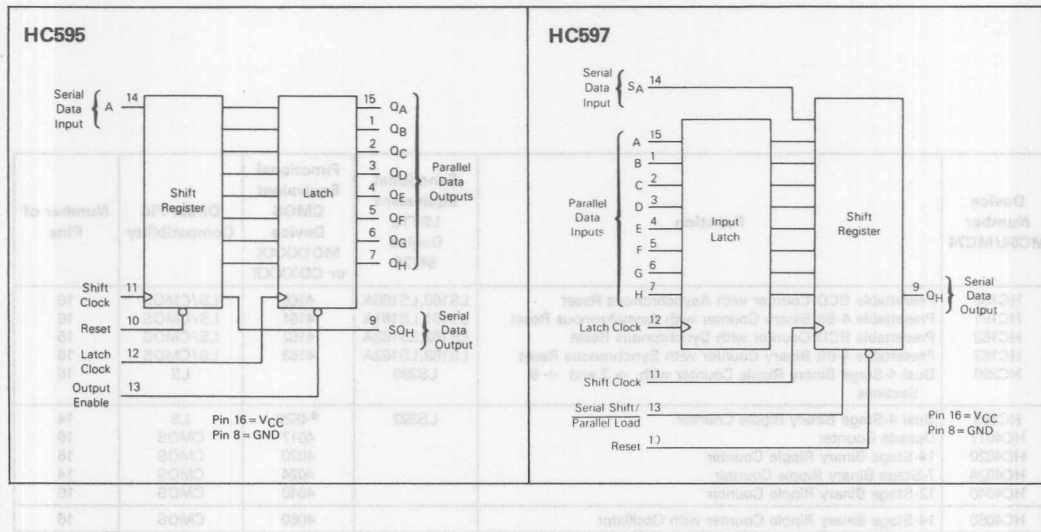
Device	HC 164	HC 165	HC 194	HC 195	HC 299	HC 589	HC 595	HC 597
# Pins	14	16	16	16	20	16	16	16
4-Bit Register	•	•	•	•	•	•	•	•
8-Bit Register	•	•	•	•	•	•	•	•
Serial Data Input	•	•	•	•	•	•	•	•
Parallel Data Inputs	•	•	•	•	•	•	•	•
Serial Output Only	•	•	•	•	•	•	•	•
Parallel Outputs	•	•	•	•	•	•	•	•
Inverting Output	•	•	•	•	•	•	•	•
Noninverting Output	•	•	•	•	•	•	•	•
Serial Shift/Parallel Load Control	•	•	•	•	•	•	•	•
Shifts One Direction Only	•	•	•	•	•	•	•	•
Shifts Both Directions	•	•	•	•	•	•	•	•
Positive-Transition Clocking	•	•	•	•	•	•	•	•
Active-High Clock Enable	•	•	•	•	•	•	•	•
Input Data Enable	•	•	•	•	•	•	•	•
Data Latch with Active-High Latch Clock	•	•	•	•	•	•	•	•
Output Latch with Active-High Latch Clock	•	•	•	•	•	•	•	•
3-State Outputs	•	•	•	•	•	•	•	•
Active-Low Output Enable	•	•	•	•	•	•	•	•
Active-Low Reset	•	•	•	•	•	•	•	•

SHIFT REGISTERS (Continued)

2



SHIFT REGISTERS (Continued)



2

Device	HC595	HC597	HC598	HC599	HC695	HC696	HC697	HC698	HC699	HC795	HC796	HC797	HC798	HC799	HC895	HC896	HC897	HC898	HC899
8-Bit Shift Register	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
8-Bit Shift Register with Latch	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
8-Bit Shift Register with Latch and Parallel Load	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
8-Bit Shift Register with Latch and Parallel Load and Active-Low Reset	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
8-Bit Shift Register with Latch and Parallel Load and Active-Low Reset and Active-Low Output Enable	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
8-Bit Shift Register with Latch and Parallel Load and Active-Low Reset and Active-Low Output Enable and Active-Low Data Input	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
8-Bit Shift Register with Latch and Parallel Load and Active-Low Reset and Active-Low Output Enable and Active-Low Data Input and Active-Low Data Output	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

* Suggested alternative

HC Devices Have CMOS-Compatible Inputs

Examples: the device has two such enables

Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC160	Presetable BCD Counter with Asynchronous Reset	LS160,LS160A	4160	LS/CMOS	16
HC161	Presetable 4-Bit Binary Counter with Asynchronous Reset	LS161,LS161A	4161	LS/CMOS	16
HC162	Presetable BCD Counter with Synchronous Reset	LS162,LS162A	4162	LS/CMOS	16
HC163	Presetable 4-Bit Binary Counter with Synchronous Reset	LS163,LS163A	4163	LS/CMOS	16
HC390	Dual 4-Stage Binary Ripple Counter with $\div 2$ and $\div 5$ Sections	LS390		LS	16
HC393	Dual 4-Stage Binary Ripple Counter	LS393	*4520	LS	14
HC4017	Decade Counter		4017	CMOS	16
HC4020	14-Stage Binary Ripple Counter		4020	CMOS	16
HC4024	7-Stage Binary Ripple Counter		4024	CMOS	14
HC4040	12-Stage Binary Ripple Counter		4040	CMOS	16
HC4060	14-Stage Binary Ripple Counter with Oscillator		4060	CMOS	16

*Suggested alternative

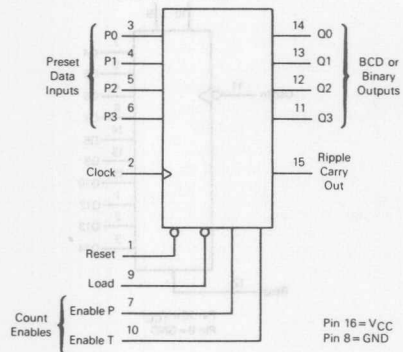
HC Devices Have CMOS-Compatible Inputs.

Device	HC 160	HC 161	HC 162	HC 163	HC 390	HC 393	HC 4017	HC 4020	HC 4024	HC 4040	HC 4060
# Pins	16	16	16	16	16	14	16	16	14	16	16
Single Device	•	•	•	•	•	•	•	•	•	•	•
Dual Device											
Ripple Counter					•	•		•	•	•	•
Number of Ripple Counter Internal Stages					4	4		14	7	12	14
Number of Stages with Available Outputs					4	4		12	7	12	10
Count Up	•	•	•	•	•	•	•	•	•	•	•
4-Bit Binary Counter		•		•		•					
BCD Counter	•		•		•		•				
Decimal Counter											
Separate $\div 2$ Section					•						
Separate $\div 5$ Section					•						
On-Chip Oscillator Capability											•
Positive-Transition Clocking	•	•	•	•		•	•	•	•	•	•
Negative-Transition Clocking					•	•					
Active-High Clock Enable							•				
Active-Low Clock Enable							•				
Active-High Count Enable	••	••	••	••							
Active-High Reset	•	•	•	•	•	•	•	•	•	•	•
4-Bit Binary Preset Data Inputs		•		•							
BCD Preset Data Inputs	•		•								
Active-Low Load Preset	•	•	•	•							
Carry Output	•	•	•	•							

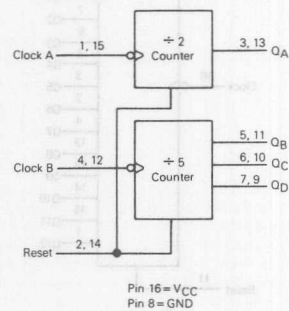
••implies the device has two such enables

COUNTERS (Continued)

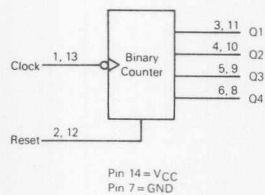
**HC160 HC162
HC161 HC163**



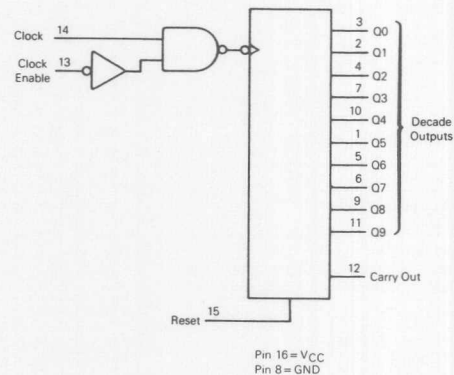
HC390



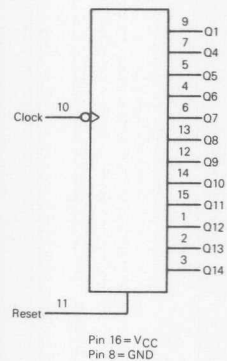
HC393



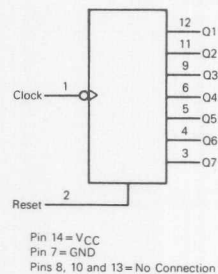
HC4017



HC4020



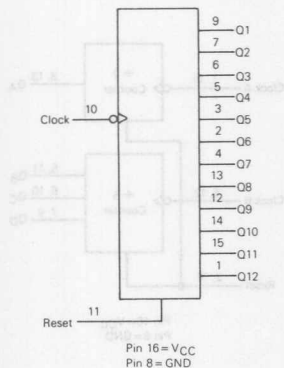
HC4024



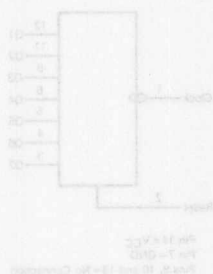
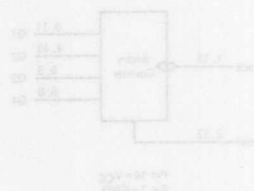
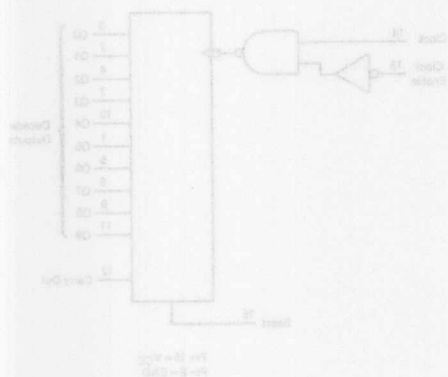
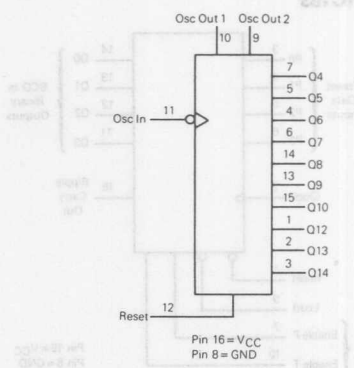
COUNTERS (Continued)

2

HC4040



HC4060

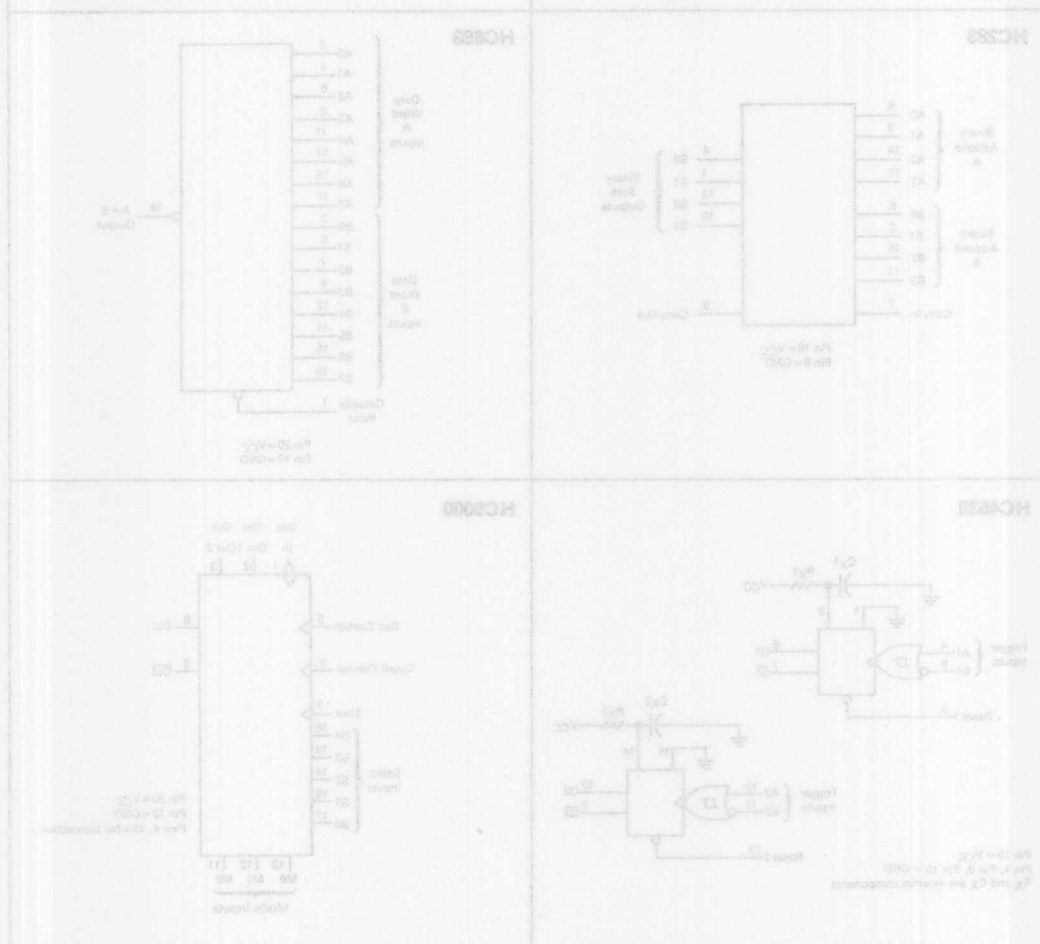


MISCELLANEOUS DEVICES

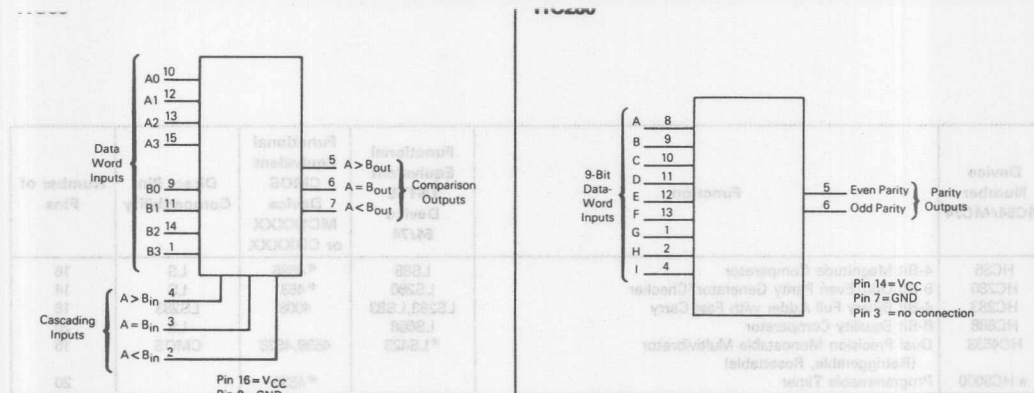
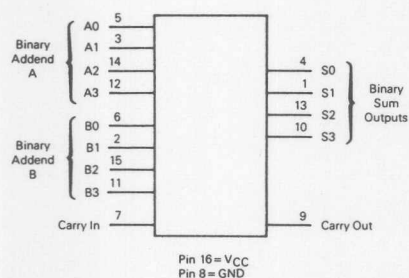
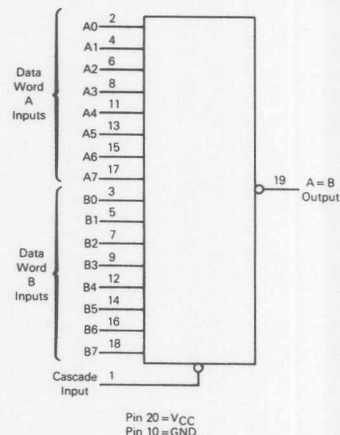
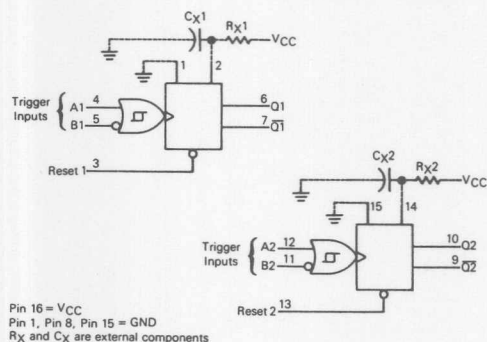
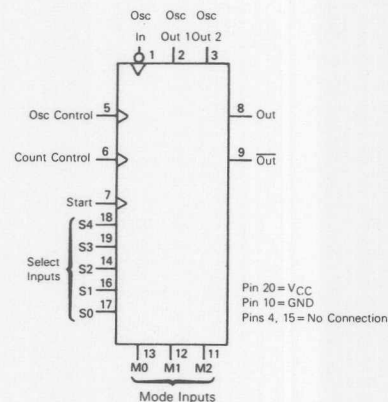
Device Number MC54/MC74	Function	Functional Equivalent LSTTL Device 54/74	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
HC85	4-Bit Magnitude Comparator	LS85	*4585	LS	16
HC280	9-Bit Odd/Even Parity Generator/Checker	LS280	*4531	LS	14
HC283	4-Bit Binary Full Adder with Fast Carry	LS283, LS83	4008	LS283	16
HC688	8-Bit Equality Comparator	LS688		LS	20
HC4538	Dual Precision Monostable Multivibrator (Retriggerable, Resettable)	*LS423	4538, 4528	CMOS	16
*HC9000	Programmable Timer		*4536		20

*Suggested alternative

*Exclusive High-Speed CMOS design



2

**HC283****HC688****HC4538****HC9000**

The “Better” Program **3**

The "BETTER" Program

Motorola's "BETTER" program was developed to provide improved levels of reliability for standard commercial products.

The "BETTER" program is offered on High-Speed CMOS in dual-in-line ceramic and plastic packages, as well as in SOIC packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

LEVEL I — SUFFIX "S"

In addition to standard processing, "BETTER" Level I product is 100% subjected to temperature cycling (10 cycles, -65°C to $+150^{\circ}\text{C}$) and also receives a high temperature functional and D.C. parametric test at the maximum rated temperature.

LEVEL II — SUFFIX "D"

"BETTER" Level II product is standard product which receives static burn-in performed according to MIL-STD-883B. A 2% P.D.A. (Percent Defective Allowed) fallout is permissible; if a greater fallout occurs, the lot is sent through another burn-in cycle. The second P.D.A. is 0.5%; parts failing this criteria are considered unmarketable.

LEVEL III — SUFFIX "DS"

Level III is a combination of "BETTER" Levels I and II. Although Motorola offers temperature cycling in its "BETTER" Level I and III product, reliability studies indicate that High-Speed CMOS routinely passes stresses of 1000 cycles (-65°C to $+150^{\circ}\text{C}$) due to improvements in wafer fabrication and assembly operations. For more information the reader is referred to Chapter 6 "Reliability", the section entitled "Thermal Cycling".

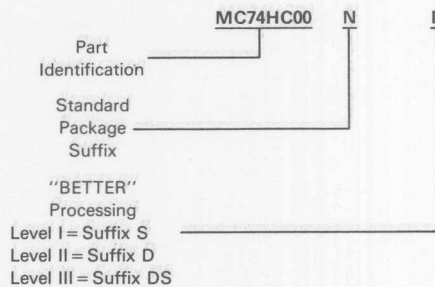
High temperature testing can also be considered unnecessary, for the 25°C test limits for all parametric tests are guard-banded to insure that device performance at the maximum recommended temperature conforms to the guaranteed limits.

High-Speed CMOS devices screened to "BETTER" Level II are recommended for highly complex circuit boards where board rework is difficult and costly. Burn-in eliminates the majority of infant mortalities, thus increasing the degree of board confidence. See Chapter 6, "Reliability" for more information on the overall reliability of High-Speed CMOS. Specifically, refer to the section entitled "Life Test" for information on the effects of burn-in on High-Speed CMOS.

PART ORDERING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

HOW TO ORDER

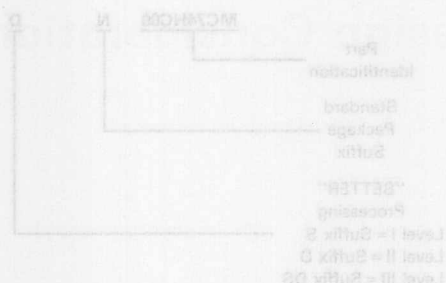


High temperature testing can also be considered unnecessary, for the 125°C test limits for all parameters are guaranteed to ensure that device performance at the maximum recommended temperature conforms to the guaranteed limits. High Speed CMOS devices screened to "BETTER" Level II are recommended for highly complex circuit boards where board rework is difficult and costly. Burn-in eliminates the majority of infant mortality, thus increasing the degree of board confidence. See Chapter 2, "Reliability," for more information on the overall reliability of High-Speed CMOS. Specifically, refer to the section entitled "Life Test," for information on the effects of burn-in on High-Speed CMOS.

PART ORDERING

The Standard Motorola part number with the corresponding "BETTER" suffix can be obtained from your local authorized Motorola distributor or Motorola sales office. "BETTER" pricing will be quoted as an add-on to standard commercial product price.

HOW TO ORDER



Motorola's "BETTER" program was developed to provide improved levels of reliability for standard commercial products. The "BETTER" program is offered on High-Speed CMOS in dual in-line ceramic and plastic packages, as well as SMD packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspection. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

LEVEL I — SUFFIX "S"

In addition to standard processing, "BETTER" Level I product is subjected to temperature cycling (10 cycles, -55°C to +125°C) and also receives a high temperature final burn-in and D.C. parametric test at the maximum rated temperature.

LEVEL II — SUFFIX "D"

"BETTER" Level II product is standard product which receives static burn-in performed according to MIL-STD-883B, A 256 P.D.A. (Percent Defective Allowed) failure is permitted. If a greater failure occurs, the lot is sent through another burn-in cycle. The second P.D.A. is 0.5%; parts failing this criteria are considered unacceptable.

LEVEL III — SUFFIX "DS"

Level III is a combination of "BETTER" Levels I and II. Although Motorola offers temperature cycling in its "BETTER" Level I and II product, reliability studies indicate that High-Speed CMOS routinely passes stresses of 1000 cycles, -55°C to +125°C due to improvements in wafer fabrication and assembly operations. For more information the reader is referred to Chapter 8, "Reliability," the section entitled "Thermal Cycling."

Page	Subject
4-3	Introduction
4-3	Handling Presentations
4-7	Power Supply Sizing
4-7	Battery Systems
4-8	Qp Power Calculation
4-8	Inputs
4-10	Outputs
4-13	3-State Outputs
4-13	Open-Drain Outputs
4-13	Input/Output Pins
4-14	Bus Termination
4-15	Transmission Line Termination
4-15	CMOS Latch Up
4-17	Maximum Power Dissipation
4-17	HC Quiescent Power Dissipation
4-17	HCT Quiescent Power Dissipation
4-17	HC and HCT Dynamic Power Dissipation
4-18	Temperature Effects on DC and AC Parameters
4-19	Supply Voltage Effects on Drive Current and Propagation Delay
4-20	Decoupling Capacitors
4-20	Interfacing
4-22	Typical Parameter Values
4-22	Reduction of Electromagnetic Interference (EMI)
4-22	Hybrid Circuit Guidelines
4-24	Schmitt-Trigger Devices
4-24	HC vs. HCT
4-25	Oscillator Design with High-Speed CMOS
4-25	RC Oscillators
4-25	Crystal Oscillators
4-26	Printed Circuit Board Layout
4-26	Glossary of Terms

Design Considerations

4

Subject	Page
Introduction	4-3
Handling Precautions	4-3
Power Supply Sizing	4-7
Battery Systems	4-7
C _{PD} Power Calculation	4-8
Inputs	4-9
Outputs	4-10
3-State Outputs	4-13
Open-Drain Outputs	4-13
Input/Output Pins	4-13
Bus Termination	4-14
Transmission Line Termination	4-15
CMOS Latch Up	4-15
Maximum Power Dissipation	4-17
HC Quiescent Power Dissipation	4-17
HCT Quiescent Power Dissipation	4-17
HC and HCT Dynamic Power Dissipation	4-17
Capacitive Loading Effects on Propagation Delay	4-18
Temperature Effects on DC and AC Parameters	4-19
Supply Voltage Effects on Drive Current and Propagation Delay	4-19
Decoupling Capacitors	4-20
Interfacing	4-20
Typical Parametric Values	4-22
Reduction of Electromagnetic Interference (EMI)	4-23
Hybrid Circuit Guidelines	4-23
Schmitt-Trigger Devices	4-24
HC vs. HCT	4-24
Oscillator Design with High-Speed CMOS	4-25
RC Oscillators	4-25
Crystal Oscillators	4-25
Printed Circuit Board Layout	4-26
Glossary of Terms	4-26

INTRODUCTION

CMOS devices have been used for many years in applications where the primary concerns were low power consumption, wide power-supply range, and high noise immunity. However, metal-gate CMOS (MC14000 series) is too slow for many applications. Applications requiring high-speed devices, such as microprocessor memory decoding, had to go to the faster families such as LSTTL. This meant sacrificing the best qualities of CMOS. The next step in the logic evolution was to introduce a family of devices that were fast enough for such applications, while retaining the advantages of CMOS. The results of this change can be seen in Table 1 where HSCMOS devices are compared to standard (metal-gate) CMOS, LSTTL, and ALS.

The Motorola CMOS evolutionary process shown in Figure 1 indicates that one advantage of the silicon-gate process is device size. The High-Speed CMOS (HSCMOS) device is about half the size of the metal-gate predecessor, yielding significant chip area savings. The silicon-gate process allows smaller gate or channel lengths due to the self-aligning gate feature. This process uses the gate to define the channel during processing, eliminating registration errors and, therefore, the need for gate overlaps. The elimination of the gate overlap significantly lowers the gate capacitance, resulting in higher speed capability. The smaller gate length also results in higher drive capability per unit gate width, ensuring more efficient use of chip area. Immunity enhancements to electrostatic discharge (ESD) damage and latch up are ongoing. Precautions should still be taken, however, to guard against electrostatic discharge and latch up.

Motorola's High-Speed CMOS family has a broad range of functions from basic gates, flip-flops, and counters to bus-compatible devices. The family is made up of devices that are identical in pinout and are functionally equivalent to LSTTL devices, as well as the most popular metal-gate devices not available in TTL. Thus, the designer has an excellent alternative to existing families without having to become familiar with a new set of device numbers.

HANDLING PRECAUTIONS

High-Speed CMOS devices, like all MOS devices, have an insulated gate that is subject to voltage breakdown. The gate oxide for HSCMOS devices breaks down at a gate-source potential of about 100 volts. All device inputs are protected by a resistor-diode network (Figure 2). Using the test setup shown in Figure 3, the inputs typically withstand a >2 kV discharge.

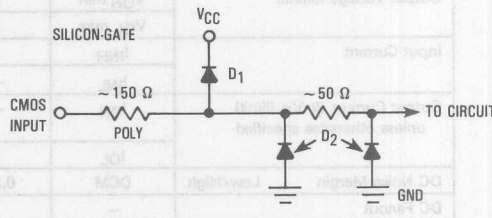


Figure 2. Input Protection Network

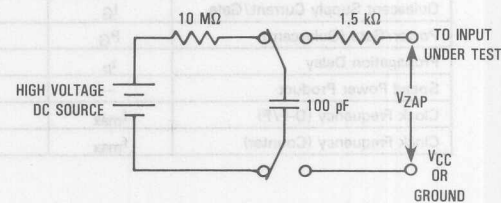


Figure 3. Electrostatic Discharge Test Circuit

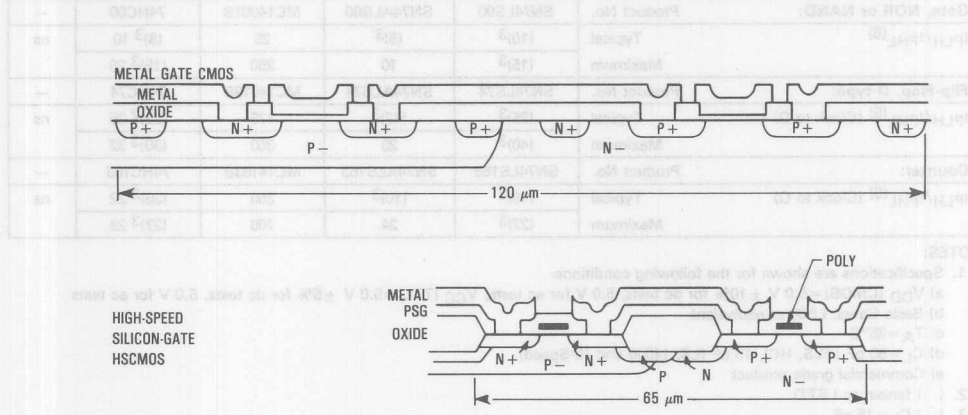


Figure 1. CMOS Evolution

General Characteristics (1) (All Maximum Ratings)

Characteristic	Symbol	TTL		CMOS		Unit
		LS	ALS	MC14000	Hi-Speed	
Operating Voltage Range	$V_{CC}/EE/DD$	$5 \pm 5\%$	$5 \pm 5\%$	3.0 to 18	2.0 to 6.0	V
Operating Temperature Range	T_A	0 to +70	0 to +70	-40 to +85	-55 to +125	°C
Input Voltage (limits)	V_{IH} min	2.0	2.0	3.5 ⁴	3.5 ⁴	V
	V_{IL} max	0.8	0.8	1.5 ⁴	1.0 ⁴	V
Output Voltage (limits)	V_{OH} min	2.7	2.7	$V_{DD} - 0.05$	$V_{CC} - 0.1$	V
	V_{OL} max	0.5	0.5	0.05	0.1	V
Input Current	I_{INH}	20	20	± 0.3	± 1.0	μA
	I_{INL}	-400	-200			
Output Current @ V_O (limit) unless otherwise specified	I_{OH}	-0.4	-0.4	-2.1 @ 2.5 V	-4.0 @ $V_{CC} - 0.8$ V	mA
	I_{OL}	8.0	8.0	0.44 @ 0.4 V	4.0 @ 0.4 V	mA
DC Noise Margin Low/High	DCM	0.3/0.7	0.3/0.7	1.45 ⁴	0.90/1.35 ⁴	V
DC Fanout	—	20	20	$> 50(1)^2$	$50(10)^2$	—

Speed/Power Characteristics (1) (All Typical Ratings)

Characteristic	Symbol	TTL		CMOS		Unit
		LS	ALS	MC14000	Hi-Speed	
Quiescent Supply Current/Gate	I_G	0.4	0.2	0.0001	0.0005	mA
Power/Gate (Quiescent)	P_G	2.0	1.0	0.0006	0.001	mW
Propagation Delay	t_p	9.0	7.0	125	8.0	ns
Speed Power Product	—	18	7.0	0.075	0.01	pJ
Clock Frequency (D-F/F)	f_{max}	33	35	4.0	40	MHz
Clock Frequency (Counter)	f_{max}	40	45	5.0	40	MHz

Propagation Delay (1)

Characteristic		TTL		CMOS		Unit
		LS	ALS	MC14000	Hi-Speed	
Gate, NOR or NAND:	Product No.	SN74LS00	SN74ALS00	MC14001B	74HC00	—
	Typical	(10) ³	(5) ³	25	(8) ³ 10	ns
	Maximum	(15) ³	10	250	(15) ³ 20	
Flip-Flop, D-type:	Product No.	SN74LS74	SN74ALS74	MC14013B	74HC74	—
	Typical	(25) ³	(12) ³	175	(23) ² 25	ns
	Maximum	(40) ³	20	350	(30) ³ 32	
Counter:	Product No.	SN74LS163	SN74ALS163	MC14163B	74HC163	—
	Typical	(18) ³	(10) ³	350	(20) ³ 22	ns
	Maximum	(27) ³	24	700	(27) ³ 29	

NOTES:

- Specifications are shown for the following conditions:
 - V_{DD} (CMOS) = 5.0 V \pm 10% for dc tests, 5.0 V for ac tests; V_{CC} (TTL) = 5.0 V \pm 5% for dc tests, 5.0 V for ac tests
 - Basic Gates: LS00 or equivalent
 - $T_A = 25^\circ C$
 - $C_L = 50$ pF (ALS, HC), 15 pF (LS, 14000 and Hi-Speed)
 - Commercial grade product
- () fanout to LS TTL
- () $C_L = 15$ pF
- DC input voltage specifications are proportional to supply voltage over operating range.
- The number specified is the larger of t_{PLH} and t_{PHL} for each device.

The input protection network uses a polysilicon resistor in series with the input and before the protection diodes. This series resistor slows down the slew rate of static discharge spikes to allow the protection diodes time to turn on. Outputs have a similar ESD protection network except for the series resistor. Although the on-chip protection circuitry guards against ESD damage, additional protection may be necessary once the chip is placed in circuit. Both an external series resistor and ground and V_{CC} diodes, similar to the input protection structure, are recommended if there is a potential of ESD, voltage transients, etc. Several monolithic diode arrays are available from Motorola, such as the MAD130 (dual 10 diode array) or the MAD1104 (dual 8 diode array). These diodes, in chip form, not only provide the necessary protection, but also save board space as opposed to using discrete diodes.

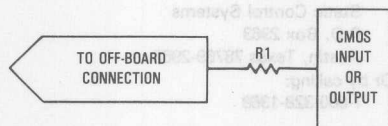
Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged pins are the easiest to detect. An ESD-damaged pin that has been completely destroyed may exhibit a low-impedance path to V_{CC} or GND. Another common failure mode is a fused or open circuit. The effect of both failure modes is that the device no longer properly responds to input signals. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Generally, another effect of static damage is increased chip leakage currents (I_{CC}).

Although the input network does offer significant protection, these devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4 to 15 kV range (depending

on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

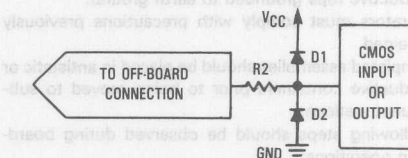
1. Wrist straps and equipment logs should be maintained and audited on a regular basis. Wrist straps malfunction and may go unnoticed. Also, equipment gets moved from time to time and grounds may not be reconnected properly.
2. Do not exceed the Maximum Ratings specified by the data sheet.
3. All unused device inputs should be connected to V_{CC} or GND.
4. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
5. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connectors to a PC board are connected to an input or output of a CMOS device, a resistor should be used in series with the input or output. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. The delay is caused by the time constant formed by the series resistor and input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 4, two possible networks are shown using a series resistor to reduce ESD damage. For convenience, an equation is given for added propagation delay and rise time effects due to series resistance size.

4



Advantage: Requires minimal board area

Disadvantage: $R1 > R2$ for the same level of protection; therefore, rise and fall times, propagation delays, and output drives are severely affected.



Advantage: $R2 < R1$ for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost.

NOTE: These networks are useful for protecting the following:

- | | |
|------------------------------|-----------------------------|
| A digital inputs and outputs | C 3-state outputs |
| B analog inputs and outputs | D bidirectional (I/O) ports |

Propagation Delay and Rise Time vs. Series Resistance

$$R \approx \frac{t}{C \cdot k}$$

where:

- R = the maximum allowable series resistance in ohms
- t = the maximum tolerable propagation delay or rise time in seconds
- C = the board capacitance plus the driven device's input capacitance in farads
- k = 0.7 for propagation delay calculations
- k = 2.3 for rise time calculations

Figure 4. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility

6. All CMOS devices should be stored or transported in materials that are antistatic or conductive. CMOS devices must not be inserted into conventional plastic "snow", styrofoam, or plastic trays, but should be left in their original container until ready for use.
7. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, because a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are essential and should be tested daily. See Figure 5 for an example of a typical work station.
8. Nylon or other static generating materials should not come in contact with CMOS devices.
9. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static buildup by using ionized air blowers, anti-static sprays, and room humidifiers. All conductive parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to earth ground.
10. Cold chambers using CO₂ for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
11. When lead straightening or hand soldering is necessary, provide ground straps for the apparatus used and be sure that soldering iron tips are grounded.
12. The following steps should be observed during wave solder operations:
 - a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to earth ground.
 - b. The loading and unloading work benches should have conductive tops grounded to earth ground.
 - c. Operators must comply with precautions previously explained.
 - d. Completed assemblies should be placed in antistatic or conductive containers prior to being moved to subsequent stations.
13. The following steps should be observed during board-cleaning operations:
 - a. Vapor degreasers and baskets must be grounded to earth ground.
 - b. Brush or spray cleaning should not be used.
 - c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic or conductive container.
 - d. Cleaned assemblies should be placed in antistatic or conductive containers immediately after removal from the cleaning basket.
 - e. High velocity air movement or application of solvents and coatings should be employed only when a static eliminator using ionized air is directed at the printed circuit board.
14. The use of static detection meters for production line surveillance is highly recommended.
15. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
16. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
17. Double check test equipment setup for proper polarity of VCC and GND before conducting parametric or functional testing.
18. Do not recycle shipping rails. Repeated use causes deterioration of their antistatic coating. Exception: carbon rails (black color) may be recycled to some extent. This type of rail is conductive and antistatic.

RECOMMENDED READING

"Total Control of the Static in Your Business"

Available by writing to:

3M Company
Static Control Systems
P.O. Box 2963
Austin, Texas 78769-2963

Or by calling:
1-800-328-1368

S. Cherniak, "A Review of Transients and Their Means of Suppression", Application Note-843, Motorola Semiconductor Products Inc., 1982.

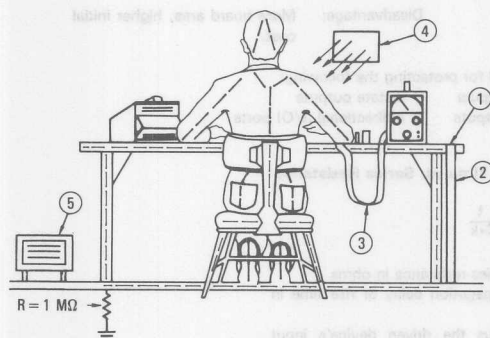


Figure 5. Typical Manufacturing Work Station

NOTES:

1. 1/16 inch conductive sheet stock covering bench-top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside a building to be less than outside humidity.

POWER SUPPLY SIZING

CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive power supplies without cooling fans. In addition, batteries may be used as either a primary power source or as a backup.

The maximum recommended power supply voltage for HC devices is 6.0 V and 5.5 V for HCT devices. Figure 6 offers some insight as to how this specification was derived. In the figure, V_S is the maximum power supply voltage and I_S is the sustaining current for the latch-up mode. The value of V_S was chosen so that the secondary breakdown effect may be avoided. The low-current junction avalanche region is between 10 and 14 volts at $T_A = 25^\circ\text{C}$.

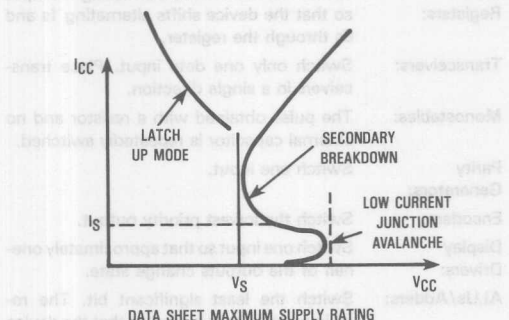


Figure 6. Secondary Breakdown Characteristics

In an ideal system design, the power supply should be designed to deliver only enough current to ensure proper operation of all devices. The obvious benefit of this type of design is cost savings.

BATTERY SYSTEMS

HSCMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery-operated systems.

1. The recommended power supply voltages should be observed. For battery backup systems such as the one in Figure 7, the battery voltage must be at least 2.7 volts (2 volts for the minimum power supply voltage and 0.7 volts to account for the voltage drop across the series diode).
2. Inputs that might go above the battery backup voltage should use the HC4049 or HC4050 buffers (Figure 8). If line power is interrupted, CMOS System A and Buffer A lose power. However, CMOS System B and Buffer B remain active due to the battery backup. Buffer A protects System A from System B by blocking active inputs while the circuit is not powered up. Also, if the power supply voltage drops below the battery voltage, Buffer A acts as a level translator for the outputs from System B. Buffer B acts to protect System B from any overvoltages which might exist. Both buffers may be replaced with current-limiting resistors, however power consumption is increased and propagation delays are lengthened.
3. Outputs that are subject to voltage levels above V_{CC} or below GND should be protected with a series resistor and/or clamping diodes to limit the current to an acceptable level.

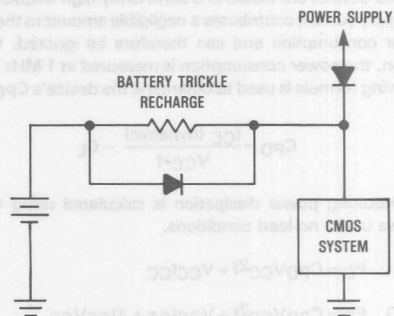


Figure 7. Battery Backup System

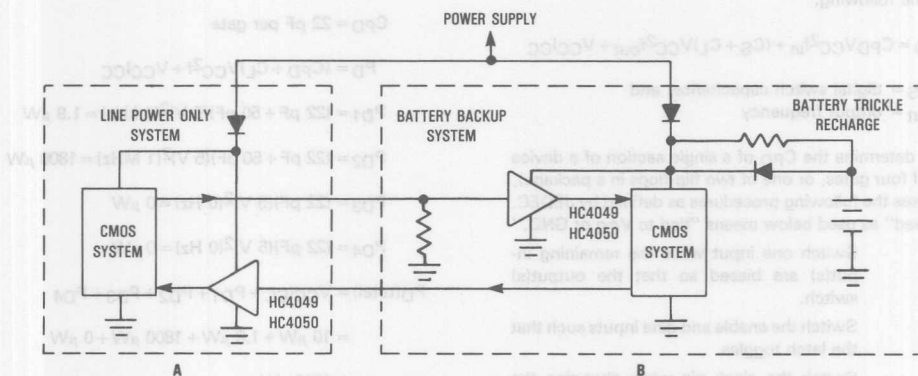


Figure 8. Battery Backup Interface

Power consumption for HCMOS is dependent on the power-supply voltage, frequency of operation, internal capacitance, and load. The power consumption may be calculated for each package by summing the quiescent power consumption, $I_{CC} \cdot V_{CC}$, and the switching power required by each device within the package. For large systems, the most timely method is to bread-board the circuit and measure the current required under a variety of conditions.

The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD}) V_{CC}^2 f$$

where: P_D = power dissipated in μW

C_L = total load capacitance present at the output in pF

C_{PD} = a measure of internal capacitances, called power dissipation capacitance, given in pF

V_{CC} = supply voltage in volts

f = frequency in MHz

If the devices are tested at a sufficiently high frequency, the dc supply current contributes a negligible amount to the overall power consumption and can therefore be ignored. For this reason, the power consumption is measured at 1 MHz and the following formula is used to determine the device's C_{PD} value:

$$C_{PD} = \frac{I_{CC}(\text{dynamic})}{V_{CC} \cdot f} - C_L$$

The resulting power dissipation is calculated using C_{PD} as follows under no-load conditions.

$$(HC) \quad P_D = C_{PD} V_{CC}^2 f + V_{CC} I_{CC}$$

$$(HCT) \quad P_D = C_{PD} V_{CC}^2 f + V_{CC} I_{CC} + \Delta I_{CC} V_{CC} (\delta_1 + \delta_2 + \dots + \delta_n)$$

where the previously undefined variable, δ_n is the duty cycle of each input applied at TTL/NMOS levels.

The power dissipation for analog switches switching digital signals is the following:

$$(HC) \quad P_D = C_{PD} V_{CC}^2 f_{in} + (C_S + C_L) V_{CC}^2 f_{out} + V_{CC} I_{CC}$$

where: C_S = digital switch capacitance, and
 f_{out} = output frequency

In order to determine the C_{PD} of a single section of a device (i.e., one of four gates, or one of two flip-flops in a package), Motorola uses the following procedures as defined by JEDEC. Note: "biased" as used below means "tied to V_{CC} or GND."

- Gates:** Switch one input while the remaining input(s) are biased so that the output(s) switch.
- Latches:** Switch the enable and data inputs such that the latch toggles.
- Flip-Flops:** Switch the clock pin while changing the data pin(s) such that the output(s) change with each clock cycle.

- Data Selectors/Multiplexers:** Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.
- Analog Switches:** Switch one address/select pin which changes two switches. The switch inputs/outputs should be left open. For digital applications where the switch inputs/outputs change between V_{CC} and GND, the respective switch capacitance should be added to the load capacitance.
- Counters:** Switch the clock pin with the other inputs biased so that the device counts.
- Shift Registers:** Switch the clock while alternating the input so that the device shifts alternating 1s and 0s through the register.
- Transceivers:** Switch only one data input. Place transceivers in a single direction.
- Monostables:** The pulse obtained with a resistor and no external capacitor is repeatedly switched.
- Parity Generators:** Switch one input.
- Encoders:** Switch the lowest priority output.
- Display Drivers:** Switch one input so that approximately one-half of the outputs change state.
- ALUs/Adders:** Switch the least significant bit. The remaining inputs are biased so that the device is alternately adding 0000 (binary) or 0001 (binary) to 1111 (binary).

On HCMOS data sheets, C_{PD} is a typical value and is given either for the package or for the individual device (i.e., gates, flip-flops, etc.) within the package. An example of calculating the package power requirement is given using the 74HC00, as shown in Figure 9.

From the data sheet:

$$I_{CC} = 2 \mu A \text{ at room temperature (per package)}$$

$$C_{PD} = 22 \text{ pF per gate}$$

$$P_D = (C_{PD} + C_L) V_{CC}^2 f + V_{CC} I_{CC}$$

$$P_{D1} = (22 \text{ pF} + 50 \text{ pF})(5 \text{ V})^2(1 \text{ kHz}) = 1.8 \mu W$$

$$P_{D2} = (22 \text{ pF} + 50 \text{ pF})(5 \text{ V})^2(1 \text{ MHz}) = 1800 \mu W$$

$$P_{D3} = (22 \text{ pF})(5 \text{ V})^2(0 \text{ Hz}) = 0 \mu W$$

$$P_{D4} = (22 \text{ pF})(5 \text{ V})^2(0 \text{ Hz}) = 0 \mu W$$

$$P_D(\text{total}) = V_{CC} I_{CC} + P_{D1} + P_{D2} + P_{D3} + P_{D4}$$

$$= 10 \mu W + 1.8 \mu W + 1800 \mu W + 0 \mu W$$

$$= 1812 \mu W$$

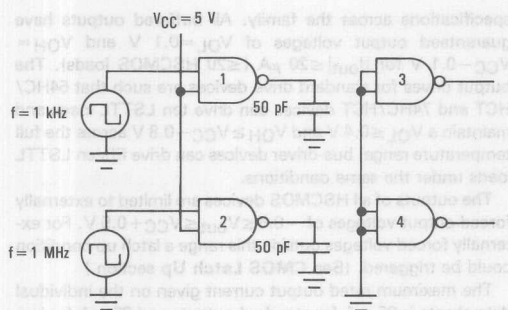


Figure 9. Power Consumption Calculation Example

As seen by this example, the power dissipated by CMOS devices is dependent on frequency. When operating at very high frequencies, HSCMOS devices can consume as much power as LSTTL devices, as shown in Figure 10. The power savings of HSCMOS is realized when used in a system where only a few of the devices are actually switching at the system frequency. The power consumption savings comes from the fact that for CMOS, only the devices that are switching consume significant power.

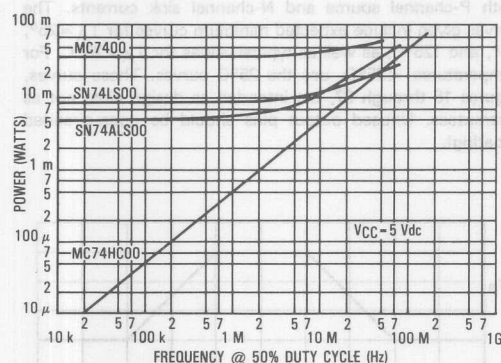


Figure 10. Power Consumption vs. Input Frequency for TTL, LSTTL, ALS, and HSCMOS

INPUTS

A basic knowledge of input and output structures is essential to the HSCMOS designer. This section deals with the various input characteristics and application rules regarding their use. Output characteristics are discussed in the section titled **Outputs**.

All standard HC, HCU and HCT inputs, while in the recommended operating range ($GND \leq V_{in} \leq V_{CC}$), can be modeled as shown in Figure 11. For input voltages in this range, diodes D1 and D2 are modeled as resistors representing the high-impedance of reverse biased diodes. The maximum input current is $1 \mu A$, worst case over temperature, when the inputs are at V_{CC} or GND , and $V_{CC} = 6 V$.

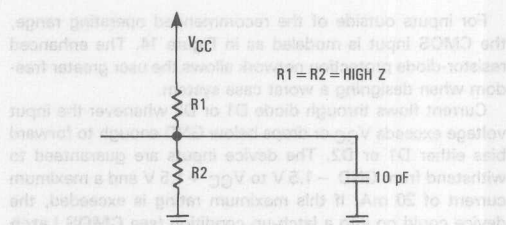


Figure 11. Input Model for $GND \leq V_{in} \leq V_{CC}$

When CMOS inputs are left open-circuited, the inputs may be biased at or near the typical CMOS switchpoint of $0.45 V_{CC}$ for HC devices or $1.3 V$ for HCT devices. At this switchpoint, both the P-channel and the N-channel transistors are conducting, causing excess current drain. Due to the high gain of the buffered devices (see Figure 12), the device can go into oscillation from any noise in the system, resulting in even higher current drain.

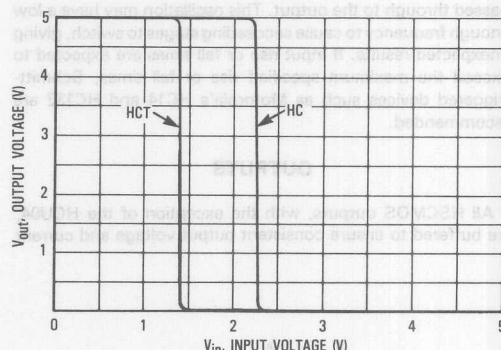


Figure 12. Typical Transfer Characteristics for Buffered Devices

For these reasons, all unused HC/HCT inputs should be connected either to V_{CC} or GND . For applications with inputs going to edge connectors, a $100 k\Omega$ resistor to GND should be used, as well as a series resistor (R_S) for static protection and current limiting (see **Handling Precautions**, this chapter, for series resistor consideration). The resistors should be configured as in Figure 13.

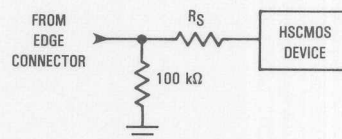


Figure 13. External Protection

For inputs outside of the recommended operating range, the CMOS input is modeled as in Figure 14. The enhanced resistor-diode protection network allows the user greater freedom when designing a worst case system.

Current flows through diode D1 or D2 whenever the input voltage exceeds V_{CC} or drops below GND enough to forward bias either D1 or D2. The device inputs are guaranteed to withstand from GND -1.5 V to $V_{CC} + 1.5$ V and a maximum current of 20 mA. If this maximum rating is exceeded, the device could go into a latch-up condition (see **CMOS Latch Up** section). Voltage should never be applied to any input or output pin before power has been applied to the device's power pins. Bias on input or output pins should be removed before removing the power. However, if the input current is limited to less than 20 mA, and this current only lasts for a brief period of time (< 100 ms), no damage to the device occurs.

Another specification that should be noted is the maximum input rise (t_r) and fall (t_f) times. Figure 15 shows the results of exceeding the maximum rise and fall times recommended by Motorola or contained in JEDEC Standard No. 7A. The reason for the oscillation on the output is that as the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input line is amplified, and is passed through to the output. This oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed the maximum specified rise or fall times, Schmitt-triggered devices such as Motorola's HC14 and HC132 are recommended.

OUTPUTS

All HSCMOS outputs, with the exception of the HCU04, are buffered to ensure consistent output voltage and current

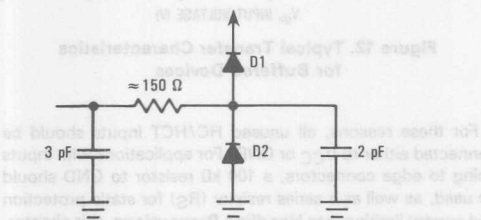


Figure 14. Input Model for $V_{in} > V_{CC}$ or $V_{in} < GND$

specifications across the family. All buffered outputs have guaranteed output voltages of $V_{OL} = 0.1$ V and $V_{OH} = V_{CC} - 0.1$ V for $|I_{out}| \leq 20$ μ A (≤ 20 HSCMOS loads). The output drives for standard drive devices are such that 54HC/HCT and 74HC/HCT devices can drive ten LSTTL loads and maintain a $V_{OL} \leq 0.4$ V and $V_{OH} \geq V_{CC} - 0.8$ V across the full temperature range; bus-driver devices can drive fifteen LSTTL loads under the same conditions.

The outputs of all HSCMOS devices are limited to externally forced output voltages of $-0.5 \leq V_{out} \leq V_{CC} + 0.5$ V. For externally forced voltages outside this range a latch up condition could be triggered. (See **CMOS Latch Up** section.)

The maximum rated output current given on the individual data sheets is 25 mA for standard outputs and 35 mA for bus drivers. The output short circuit currents of these devices typically exceed these limits. The outputs can, however, be shorted for short periods of time for logic testing, if the maximum package power dissipation is not violated. (See individual data sheets for maximum power dissipation ratings.)

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), devices within the same package may be paralleled. Paralleling devices in different packages may result in devices switching at different points on the input voltage waveform, creating output short circuits and yielding undesirable output voltage waveforms.

As a design aid, output characteristic curves are given for both P-channel source and N-channel sink currents. The curves given include expected minimum curves for $T_A = 25^\circ$, 85° , and 125° C, as well as typical values for $T_A = 25^\circ$ C. For temperatures $< 25^\circ$ C, use the 25° C curves. These curves, Figures 16 through 27, are intended as design aids, not as guarantees. Unused output pins should be open-circuited (floating).

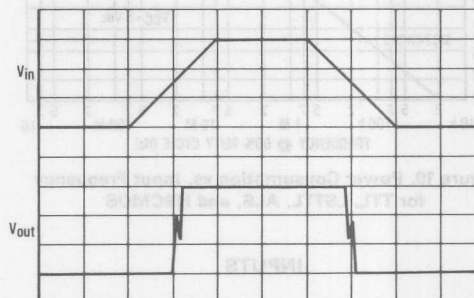


Figure 15. Maximum Rise Time Violation

STANDARD OUTPUT CHARACTERISTICS

N-CHANNEL SINK CURRENT

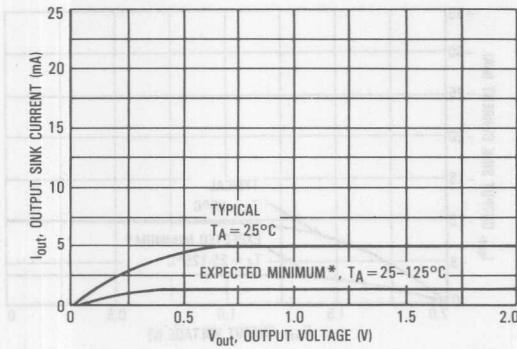


Figure 16. $V_{GS} = 2.0$ V

P-CHANNEL SOURCE CURRENT

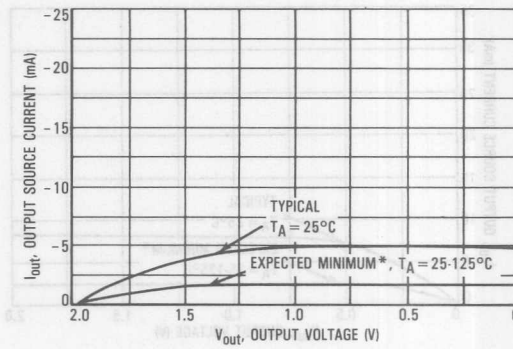


Figure 17. $V_{GS} = -2.0$ V

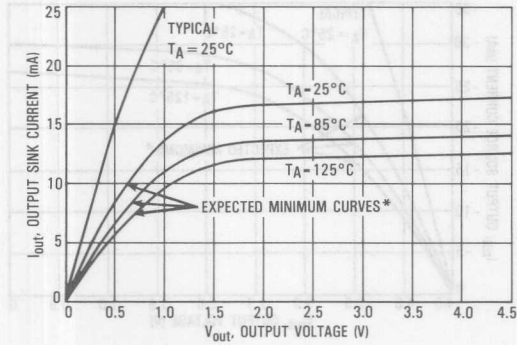


Figure 18. $V_{GS} = 4.5$ V

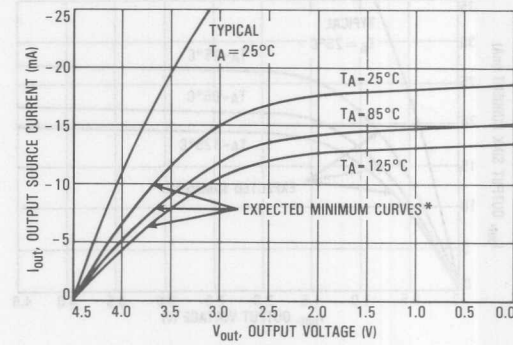


Figure 19. $V_{GS} = -4.5$ V

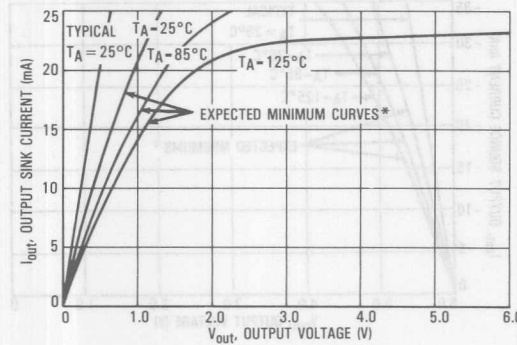


Figure 20. $V_{GS} = 6.0$ V

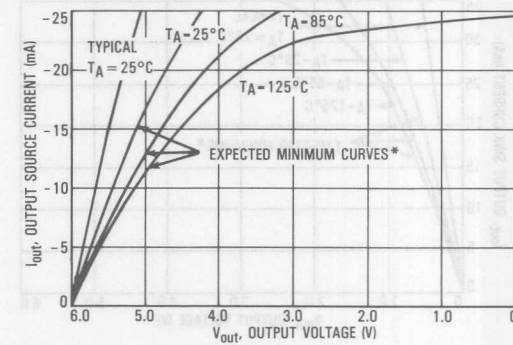


Figure 21. $V_{GS} = -6.0$ V

*The expected minimum curves are not guarantees but are design aids.

N-CHANNEL SINK CURRENT

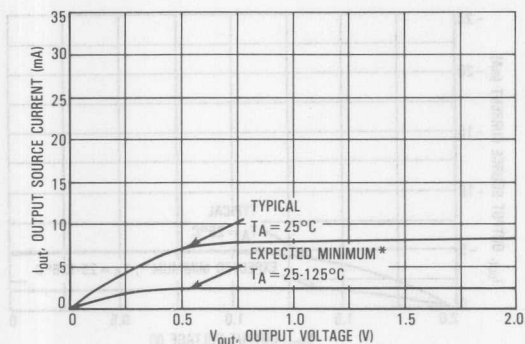


Figure 22. $V_{GS} = 2.0$ V

P-CHANNEL SOURCE CURRENT

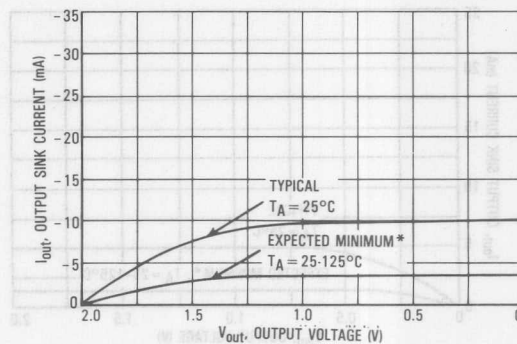


Figure 23. $V_{GS} = -2.0$ V

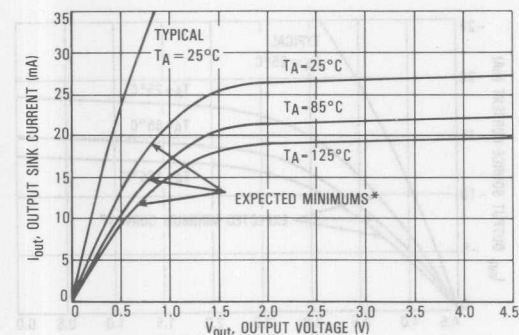


Figure 24. $V_{GS} = 4.5$ V

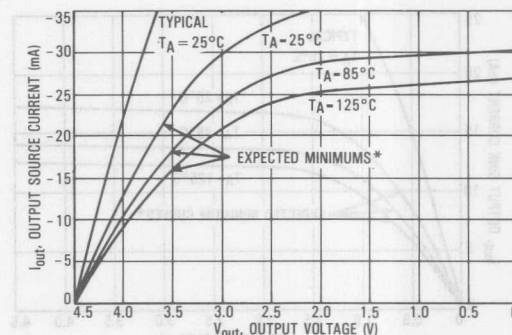


Figure 25. $V_{GS} = -4.5$ V

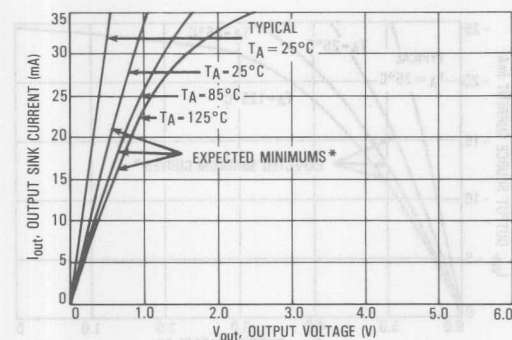


Figure 26. $V_{GS} = 6.0$ V

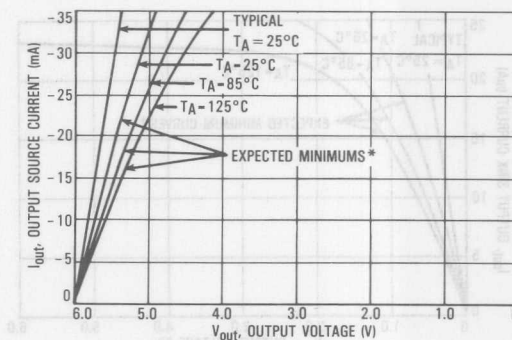


Figure 27. $V_{GS} = -6.0$ V

*The expected minimum curves are not guarantees, but are design aids.

3-STATE OUTPUTS

Some HC/HCT devices have outputs that can be placed into a high-impedance state. These 3-state output devices are very useful for gang connecting to a common line or bus. When enabled, these output pins can be considered as ordinary output pins; as such, all specifications and precautions of standard output pins should be followed. When disabled (high-impedance state), these outputs can be modeled as in Figure 28. Output leakage current ($10\ \mu\text{A}$ worst case over temperature) as well as 3-state output capacitance must be considered in any bus design.

When power is interrupted to a 3-state device, the bus voltage is forced to between GND and $V_{CC} + 0.7\ \text{V}$ regardless of the previous output state.

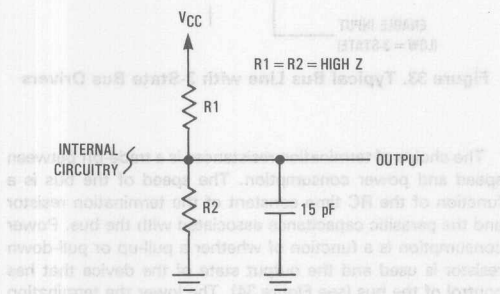


Figure 28. Model for Disabled Outputs

OPEN-DRAIN OUTPUTS

Motorola provides several devices that are designed only to sink current to GND. These open-drain output devices are fabricated using only an N-channel transistor and a diode to V_{CC} (Figure 29). The purpose of the diode is to provide ESD protection. Open-drain outputs can be modeled as shown in Figure 30.

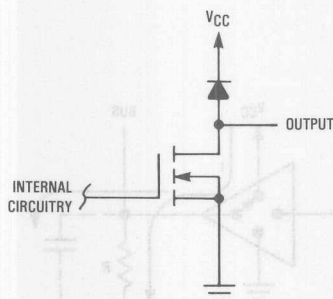


Figure 29. Open-Drain Output

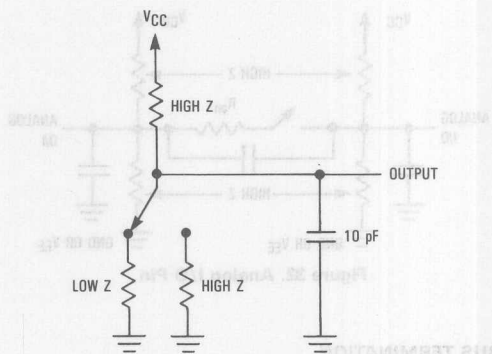


Figure 30. Model of Open-Drain Output

INPUT/OUTPUT PINS

Some HC/HCT devices contain pins that serve both as inputs and outputs of digital logic. These pins are referred to as digital I/O pins. The logic level applied to a control pin determines whether these I/O pins are selected as inputs or outputs.

When I/O pins are selected as outputs, these pins may be considered as standard CMOS outputs. When selected as inputs, except for an increase in input leakage current and input capacitance, these pins should be considered as standard CMOS inputs. These increases come from the fact that a digital I/O pin is actually a combination of an input and a 3-state output tied together (see Figure 31).

As stated earlier, all HC/HCT inputs must be connected to an appropriate logic level. This could pose a problem if an I/O pin is selected as an input while connected to an improperly terminated bus.

Motorola recommends terminating HC/HCT-type buses with resistors to V_{CC} or GND of between $1\ \text{k}\Omega$ to $1\ \text{M}\Omega$ in value. The choice of resistor value is a trade-off between speed and power consumption (see **Bus Termination**, this chapter).

Some Motorola devices have analog I/O pins. These analog I/O pins should not be confused with digital I/O pins. Analog I/O pins may be modeled as in Figure 32. These devices can be used to pass analog signals, as well as digital signals, in the same manner as mechanical switches.

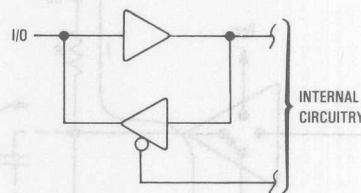


Figure 31. Typical Digital I/O Pin

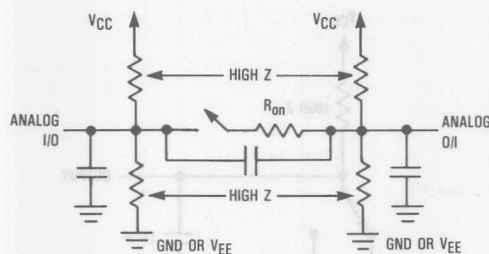
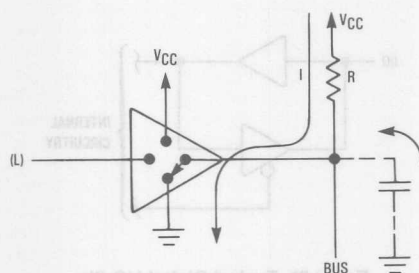


Figure 32. Analog I/O Pin

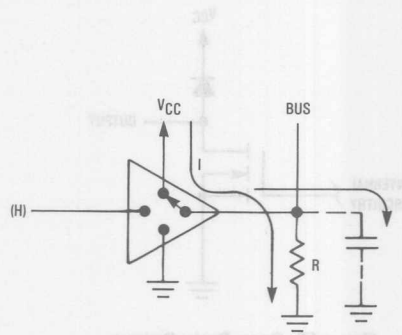
BUS TERMINATION

Because buses tend to operate in harsh, noisy environments, most bus lines are terminated via a resistor to V_{CC} or ground. This low impedance to V_{CC} or ground (depending on preference of a pull-up or pull-down logic level) reduces bus noise pickup. In certain cases a bus line may be released (put in a high-impedance state) by disabling all the 3-state bus drivers (see Figure 33). In this condition all HC/HCT inputs on the bus would be allowed to float. A CMOS input or I/O pin (when selected as an input) should never be allowed to float. (This is one reason why an HCT device may not be a drop-in replacement of an LSTTL device.) A floating CMOS input can put the device into the linear region of operation. In this region excessive current can flow and the possibility of logic errors due to oscillation may occur (see **Inputs**, this chapter). Note that when a bus is properly terminated with pull-up resistors, HC devices, instead of HCT devices, can be driven by an NMOS or LSTTL bus driver. HC devices are preferred over HCT devices in bus applications because of their higher low-level input noise margin. (With a 5 V supply the typical HC switch point is 2.3 V while the switch point of HCT is only 1.3 V.)

Some popular LSTTL bus termination designs may not work for HSCMOS devices. The outputs of HSCMOS may not be able to drive the low value of termination used by some buses. (This is another reason why an HCT device may not be a drop-in replacement for an LSTTL device.) However, because low power operation is one of the main reasons for using CMOS, an optimized CMOS bus termination is usually advantageous.



(a) USING A PULL-UP RESISTOR



(b) USING A PULL-DOWN RESISTOR

Figure 34

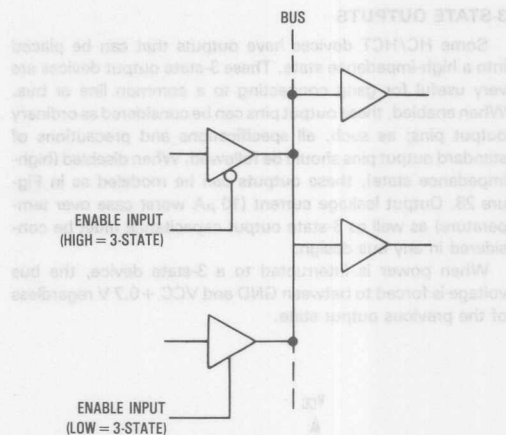


Figure 33. Typical Bus Line with 3-State Bus Drivers

The choice of termination resistances is a trade-off between speed and power consumption. The speed of the bus is a function of the RC time constant of the termination resistor and the parasitic capacitance associated with the bus. Power consumption is a function of whether a pull-up or pull-down resistor is used and the output state of the device that has control of the bus (see Figure 34). The lower the termination resistor the faster the bus operates, but more power is consumed. A large value resistor wastes less power, but slows the bus down. Motorola recommends a termination resistor value between 1 k Ω and 1 M Ω . An alternative to a passive resistor termination would be an active-type termination (see Figure 35). This type termination holds the last logic level on the bus until a driver can once again take control of the bus. An active termination has the advantage of consuming a minimal amount of power. Most HC/HCT bus drivers do not have built-in hysteresis. Therefore, heavily loaded buses can slow down rise and fall signals and exceed the input rise/fall time defined in JEDEC Standard No. 7A. In this event, devices with Schmitt-triggered inputs should be used to condition these slow signals.

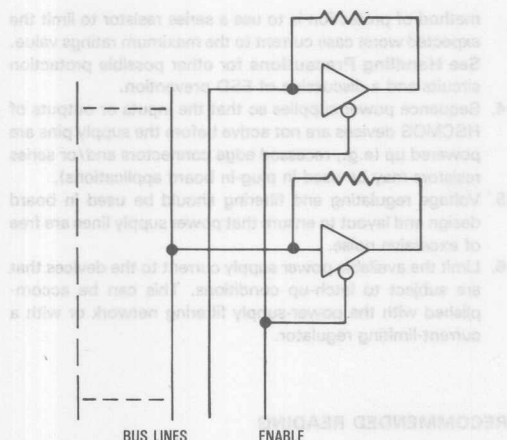


Figure 35. Using Active Termination (HC125)

TRANSMISSION LINE TERMINATION

When data is transmitted over long distances, the line on which the data travels can be considered a transmission line. (Long distance is relative to the data rate being transmitted.) Examples of transmission lines include high-speed buses, long PCB lines, coaxial and ribbon cables. All transmission lines should be properly terminated into a low-impedance termination. A low-impedance termination helps eliminate noise, ringing, overshoot, and crosstalk problems. Also a low-impedance termination reduces signal degradation because the small values of parasitic line capacitance and inductance have lesser effect on a low-impedance line.

The value of the termination resistor becomes a trade-off between power consumption, data rate speeds, and transmission line distance. The lower the resistor value, the faster data can be presented to the receiving device, but the more power the resistor consumes. The higher the resistor value, the longer it will take to charge and discharge the transmission line through the termination resistor ($T = R \cdot C$).

Transmission line distance becomes more critical as data rates increase. As data rates increase, incident (and reflective) waves begin to resemble that of RF transmission line theory. However, due to the nonlinearity of CMOS digital logic, conventional RF transmission theory is not applicable.

HC devices are preferred over HCT devices due to the fact that HC devices have higher switch points than HCT devices. This higher switch point allows HC devices to achieve better incident wave switching on lower impedance lines.

HC/HCT may not have enough drive capability to interface with some of the more popular LSTTL transmission lines. (Possible reason why an HCT device may not be a drop-in replacement of an equivalent TTL device.) This does not pose a major problem since having larger value termination resistors is desirable for CMOS type transmission lines.

By increasing the termination resistance value, the CMOS advantage of low power consumption can be realized. Motorola recommends a minimum termination resistor value as shown in Figure 36. The termination resistor should be as close to the receiving unit as possible. Another method of

terminating the line driver, as well as the receiving unit, is shown in Figure 37. Note that the resistor values in Figure 37 are twice the resistor value of Figure 36; this gives a net equivalent termination value of Figure 36. Even higher values of resistors may be used for either termination method. This reduces power consumption, but at the expense of speed and possible signal degradation.

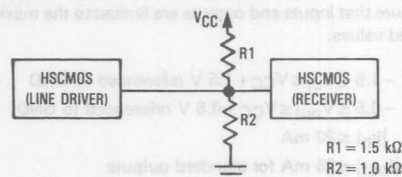


Figure 36. Termination Resistors at the Receiver

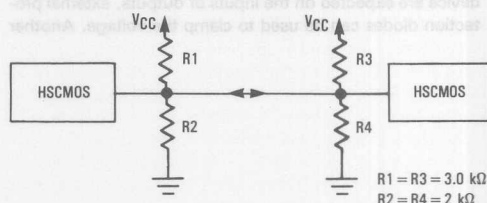


Figure 37. Termination Resistors at Both the Line Driver and Receiver

CMOS LATCH UP

Typically, HSCMOS devices do not latch up with currents of 75 mA forced into or out of the inputs or 300 mA for the outputs under worst case conditions ($T_A = 125^\circ\text{C}$ and $V_{CC} = 6\text{ V}$). Under dc conditions for the inputs, the input protection network typically fails, due to grossly exceeding the maximum input voltage rating of -1.5 V to $V_{CC} + 1.5\text{ V}$ before latch-up currents are reached. For most designs, latch up will not be a problem, but the designer should be aware of it, what causes it, and how it can be prevented.

Figure 38 shows the layout of a typical CMOS inverter and Figure 39 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the device on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than $V_{CC} + 0.5\text{ V}$ or less than -0.5 V and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device can be destroyed or its reliability can be degraded. Ways to prevent such an occurrence are listed below.

environment in which latch up is a potential problem. Also, the ringing due to inductance of long transmission lines in an industrial setting could provide enough energy to latch up CMOS devices. Opto-isolators, such as Motorola's MOC3011, are recommended to reduce chances of latch up. See the Motorola Semiconductor Master Selection Guide for a complete listing of Motorola opto-isolators.

2. Ensure that inputs and outputs are limited to the maximum rated values.

$$\begin{aligned} -1.5 \leq V_{in} &\leq V_{CC} + 1.5 \text{ V referenced to GND} \\ -0.5 \leq V_{out} &\leq V_{CC} + 0.5 \text{ V referenced to GND} \\ |I_{in}| &\leq 20 \text{ mA} \\ |I_{out}| &\leq 25 \text{ mA for standard outputs} \\ |I_{out}| &\leq 35 \text{ mA for bus-driver outputs} \end{aligned}$$

3. If voltage transients of sufficient energy to latch up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another



4

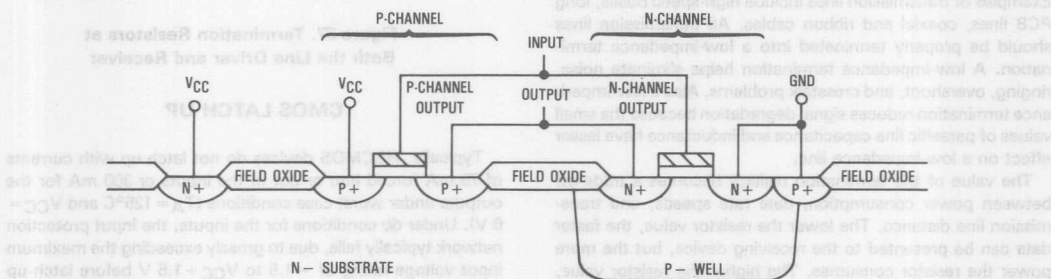


Figure 38. CMOS Wafer Cross Section

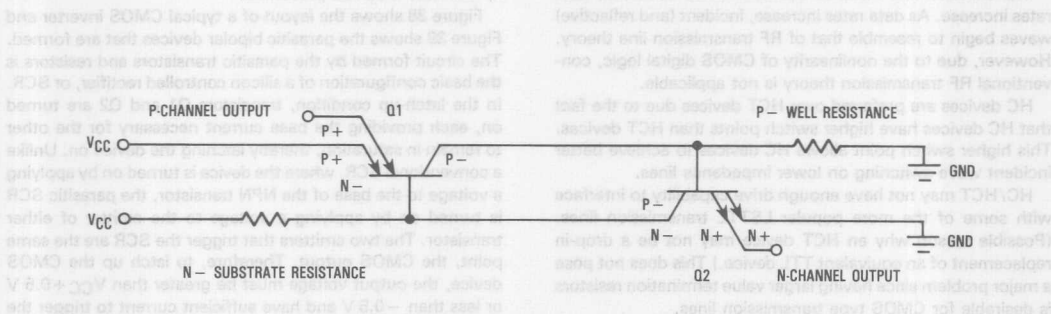


Figure 39. Latch-Up Circuit Schematic

expected worst case current to the maximum ratings value. See **Handling Precautions** for other possible protection circuits and a discussion of ESD prevention.

4. Sequence power supplies so that the inputs or outputs of HSCMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug-in board applications).
5. Voltage regulating and filtering should be used in board design and layout to ensure that power supply lines are free of excessive noise.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power-supply filtering network or with a current-limiting regulator.

RECOMMENDED READING

Paul Mannone, "Careful Design Methods Prevent CMOS Latch-Up", EDN, January 26, 1984.

MAXIMUM POWER DISSIPATION

The maximum power dissipation for Motorola HSCMOS packages is 750 mW for both ceramic and plastic DIPs and 500 mW for SOIC packages. The deratings are $-10 \text{ mW}/^\circ\text{C}$ from 65°C for plastic DIPs, $-10 \text{ mW}/^\circ\text{C}$ from 100°C for ceramic packages, and $-7 \text{ mW}/^\circ\text{C}$ from 65°C for SOIC packages. This is illustrated in Figure 40.

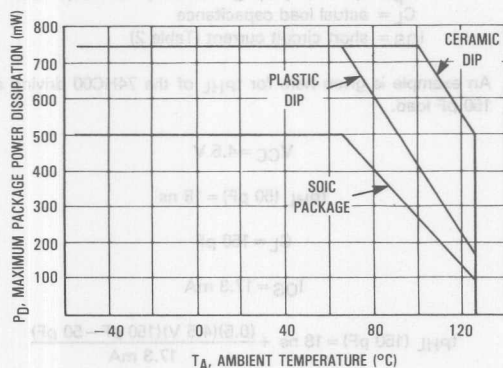


Figure 40. Maximum Package Power Dissipation versus Temperature

Internal heat generation in HSCMOS devices comes from two sources, namely, the quiescent power and dynamic power consumption.

In the quiescent state, either the P-channel or N-channel transistor in each complementary pair is off except for small source-to-drain leakage due to the inputs being either at V_{CC} or ground. Also, there are the small leakage currents flowing in the reverse-biased input protection diodes and the parasitic diodes on the chip. The specification which takes all leakage into account is called Maximum Quiescent Supply Current (per package), or I_{CC} , and is shown on all data sheets.

The three factors which directly affect the value of quiescent power dissipation are supply voltage, device complexity, and temperature. On the data sheets, I_{CC} is specified only at $V_{CC} = 6.0 \text{ V}$ because this is the worst-case supply voltage condition. Also, larger or more complex devices consume more quiescent power because these devices contain a proportionally greater reverse-biased diode junction area and more off (leaky) FETs.

Finally, as can be seen from the data sheets, temperature increases cause I_{CC} to increase. This is because at higher temperatures, leakage currents increase.

HC QUIESCENT POWER DISSIPATION

When HC device inputs are virtually at V_{CC} or GND potential (as in a totally CMOS system), quiescent power dissipation is minimized. The equation for HC quiescent power dissipation is given by:

$$P_D = V_{CC} I_{CC}$$

Worst-case I_{CC} occurs at $V_{CC} = 6.0 \text{ V}$. The value of I_{CC} at $V_{CC} = 6.0 \text{ V}$, as specified in the data sheets, is used for all power supply voltages from 2 to 6 V.

HCT QUIESCENT POWER DISSIPATION

Although HCT devices belong to the CMOS family, their input voltage specifications are identical to those of LSTTL. HCT parts can therefore be either judiciously substituted for or mixed with LS devices in a system.

TTL output voltages are $V_{OL} = 0.4 \text{ V}$ (max) and $V_{OH} = 2.4$ to 2.7 V (min).

Slightly higher I_{CC} current exists when an HCT device is driven with $V_{OL} = 0.4 \text{ V}$ (max) because this voltage is high enough to partially turn on the N-channel transistor. However, when being driven with a TTL V_{OH} , HCT devices exhibit large additional current flow (ΔI_{CC}) as specified on HCT device data sheets. ΔI_{CC} current is caused by the off-rail input voltage turning on both the P and N channels of the input buffer. This condition offers a relatively low impedance path from V_{CC} to GND. Therefore, the HCT quiescent power dissipation is dependent on the number of inputs applied at the TTL V_{IH} logic voltage level.

The equation for HCT quiescent power dissipation is given by:

$$P_D = I_{CC} V_{CC} + \eta \Delta I_{CC} V_{CC}$$

where η = the number of inputs at the TTL V_{IH} level.

HC AND HCT DYNAMIC POWER DISSIPATION

Dynamic power dissipation is calculated in the same way for both HC and HCT devices. The three major factors which directly affect the magnitude of dynamic power dissipation are load capacitance, internal capacitance, and switching transient currents.

The dynamic power dissipation due to capacitive loads is given by the following equation:

$$P_D = C_L V_{CC}^2 f$$

where P_D = power in μW , C_L = capacitive load in pF, V_{CC} = supply voltage in volts, and f = output frequency driving the load capacitor in MHz.

All CMOS devices have internal parasitic capacitances that have the same effect as external load capacitors. The magnitude of this internal no-load power dissipation capacitance, C_{PD} , is specified as a typical value.

Finally, switching transient currents affect the dynamic power dissipation. As each gate switches, there is a short period of time in which both N- and P-channel transistors are partially on, creating a low-impedance path from V_{CC} to ground. As switching frequency increases, the power dissipation due to this effect also increases.

The dynamic power dissipation due to C_{PD} and switching transient currents is given by the following equation:

$$P_D = C_{PD} V_{CC}^2 f$$

Therefore, the total dynamic power dissipation is given by:

$$P_D = (C_L + C_{PD}) V_{CC}^2 f$$

Total power dissipation for HC and HCT devices is merely a summation of the dynamic and quiescent power dissipation elements. When being driven by CMOS logic voltage levels (rail to rail), the total power dissipation for both HC and HCT devices is given by the equation:

$$P_D = V_{CC}I_{CC} + (C_L + C_{PD})V_{CC}^2f$$

When being driven by LSTTL logic voltage levels, the total power dissipation for HCT devices is given by the equation:

$$P_D = V_{CC}I_{CC} + V_{CC}\Delta I_{CC}(\delta_1 + \delta_2 + \dots + \delta_n) + (C_L + C_{PD})V_{CC}^2f$$

where δ_n = duty cycle of LSTTL output applied to each input of an HCT device.

CAPACITIVE LOADING EFFECTS ON PROPAGATION DELAY

In addition to temperature and power-supply effects, capacitive loading effects should be taken into account. The additional propagation delay may be calculated if the short circuit current for the device is known. Expected minimum numbers may be determined from Table 2.

From the equation

$$i = \frac{Cdv_c}{dt}$$

this approximation follows:

$$I = \frac{C\Delta V}{\Delta t}$$

so

$$\Delta t = \frac{C\Delta V}{I}$$

or

$$\Delta t = \frac{C(0.5 V_{CC})}{I}$$

because the propagation delay is measured to the 50% point of the output waveform (typically $0.5 V_{CC}$).

This equation gives the general form of the additional propagation delay. To calculate the propagation delay of a device for a particular load capacitance, C_L , the following equation may be used.

$$t_{PT} = t_p + 0.5 V_{CC} (C_L - 50 \text{ pF}) / I_{OS}$$

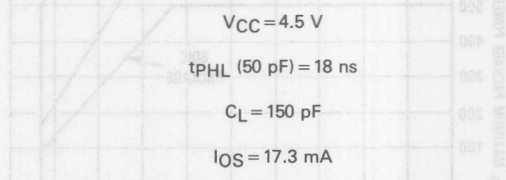
where t_{PT} = total propagation delay

t_p = specified propagation delay with 50 pF load

C_L = actual load capacitance

I_{OS} = short circuit current (Table 2)

An example is given here for t_{PHL} of the 74HC00 driving a 150 pF load.



$$t_{PHL} (150 \text{ pF}) = 18 \text{ ns} + \frac{(0.5)(4.5 \text{ V})(150 \text{ pF} - 50 \text{ pF})}{17.3 \text{ mA}}$$

$$= 18 \text{ ns} + 13 \text{ ns}$$

$$= 31 \text{ ns}$$

Another example for $C_L = 0 \text{ pF}$ and all other parameters the same.

$$t_{PHL} (0 \text{ pF}) = 18 \text{ ns} + \frac{(0.5)(4.5 \text{ V})(0 \text{ pF} - 50 \text{ pF})}{17.3 \text{ mA}}$$

$$= 18 \text{ ns} + (-6.5 \text{ ns})$$

$$t_{PHL} = 11.5 \text{ ns}$$

This method gives the expected propagation delay and is intended as a design aid, not as a guarantee.

Table 2. Expected Minimum Short Circuit Currents*

Parameter	V_{CC}	Standard Drivers			Bus Drivers			Unit
		25°C	85°C	125°C	25°C	85°C	125°C	
Output Short Circuit Source Current	2.0	1.89	1.83	1.80	3.75	3.64	3.60	mA
	4.5	18.5	15.0	13.4	37.0	30.0	26.6	
	6.0	35.2	28.0	24.6	70.6	56.1	49.2	
Output Short Circuit Sink Current	2.0	1.55	1.55	1.55	2.45	2.45	2.43	mA
	4.5	17.3	14.0	12.5	27.2	22.1	19.6	
	6.0	33.4	26.5	23.2	52.6	41.7	36.5	

*These values are intended as design aids, not as guarantees.

TEMPERATURE EFFECTS ON DC AND AC PARAMETERS

One of the inherent advantages of CMOS devices is that characteristics of the N- and P-channel transistors, such as drive current, channel resistance, propagation delay, and output transition time, track each other over a wide temperature range. Figure 41 shows the temperature relationships for these parameters. To illustrate the effects of temperature on noise margin, Figure 42 shows the typical transfer characteristics for devices with buffered inputs and outputs. Note that the typical switch point is at 45% of the supply voltage and is minimally affected by temperature.

The graphs in this section are intended to be design aids, not guarantees.

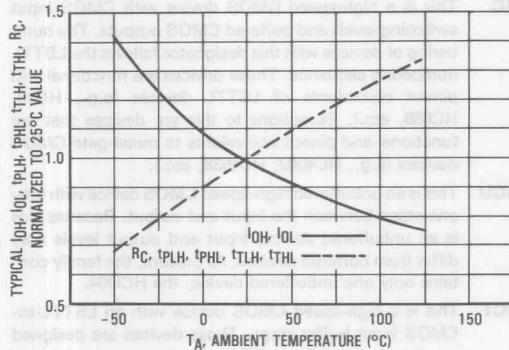


Figure 41. Characteristics of Drive Current, Channel Resistance, and AC Parameters Over Temperature

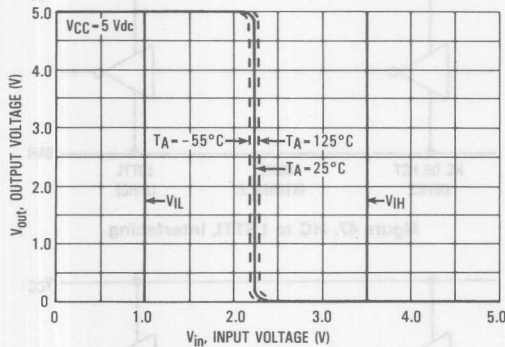


Figure 42. Temperature Effects on the HC Transfer Characteristics

SUPPLY VOLTAGE EFFECTS ON DRIVE CURRENT AND PROPAGATION DELAY

The transconductive gain, I_{out}/V_{in} , of MOSFETs is proportional to the gate voltage minus the threshold voltage, $V_G - V_T$. The gate voltage at the input of the final stage of buffered devices is approximately the power supply voltage, V_{CC} or GND. Because $V_G = V_{CC}$ or GND, the output drive current is proportional to the supply voltage. Propagation delays for CMOS devices are also affected by the power supply voltage, because most of the delay is due to charging and discharging internal capacitances. Figures 43 and 44 show the typical variation of current drive and propagation delay, normalized to $V_{CC} = 4.5$ V for $2.0 \leq V_{CC} \leq 6.0$ V. These curves may be used with the tables on each data sheet to arrive at parametric values over the voltage range.

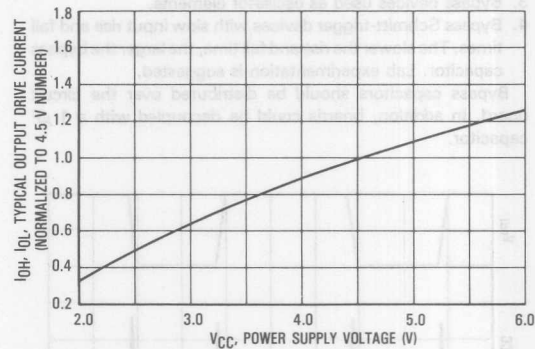


Figure 43. Drive Current versus V_{CC}

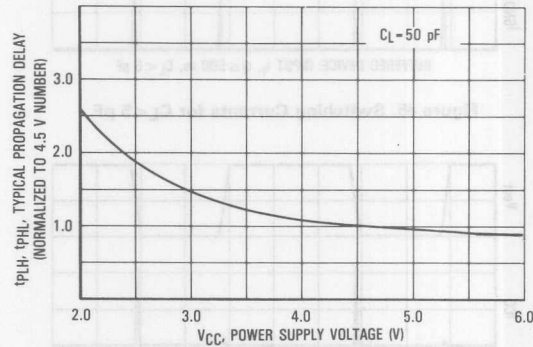


Figure 44. Propagation Delay versus V_{CC}

The switching waveforms shown in Figures 45 and 46 show the current spikes introduced to the power supply and ground lines. This effect is shown for a load capacitance of less than 5 pF and for 50 pF. For ideal power supply lines with no series impedance, the spikes would pose no problem. However, actual power supply and ground lines do possess series impedance, giving rise to noise problems. For this reason, care should be taken in board layouts, ensuring low impedance paths to and from logic devices.

To absorb switching spikes, the following HSCMOS devices should be bypassed with good quality 0.022 μF to 0.1 μF decoupling capacitors:

1. Bypass every device driving a bus with all outputs switching simultaneously.
2. Bypass all synchronous counters.
3. Bypass devices used as oscillator elements.
4. Bypass Schmitt-trigger devices with slow input rise and fall times. The slower the rise and fall time, the larger the bypass capacitor. Lab experimentation is suggested.

Bypass capacitors should be distributed over the circuit board. In addition, boards could be decoupled with a 1 μF capacitor.

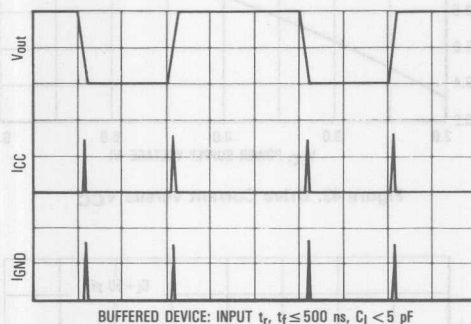


Figure 45. Switching Currents for $C_L < 5 \text{ pF}$

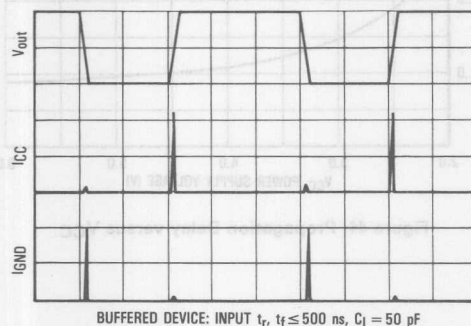


Figure 46. Switching Currents for $C_L = 50 \text{ pF}$

HSCMOS devices have a wide operating voltage range ($V_{CC} = 2$ to 6 V) and sufficient current drive to interface with most other logic families available today. In this section, various interface schemes are given to aid the designer (see Figures 47 through 52). The various types of CMOS devices with their input/output levels and comments are given in Table 3.

Motorola presently has available several CMOS memories and microprocessors (see Table 4) which are designed to directly interface with High-Speed CMOS. With these devices now available, the designer has an attractive alternative to LSTTL/NMOS, and a total HSCMOS system is now possible. (See SG102, CMOS System IC Selection Guide, for more information.)

Device designators are as follows:

HC This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs. The numbering of devices with this designator follows the LSTTL numbering sequence. These devices are functional and pinout equivalents of LSTTL devices (e.g., HC00, HC688, etc.). Exceptions to this are devices that are functional and pinout equivalents to metal-gate CMOS devices (e.g., HC4002, HC4538, etc.).

HCU This is an unbuffered high-speed CMOS device with only one stage between the input and output. Because this is an unbuffered device, input and output levels may differ from buffered devices. At present, the family contains only one unbuffered device, the HCU04.

HCT This is a high-speed CMOS device with an LSTTL-to-CMOS input buffer stage. These devices are designed to interface with LSTTL outputs operating at $V_{CC} = 5 \text{ V} \pm 10\%$. HCT devices have fully buffered CMOS outputs that directly drive HSCMOS or LSTTL devices.

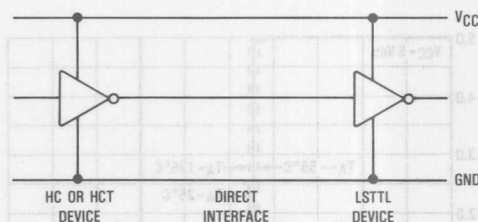


Figure 47. HC to LSTTL Interfacing

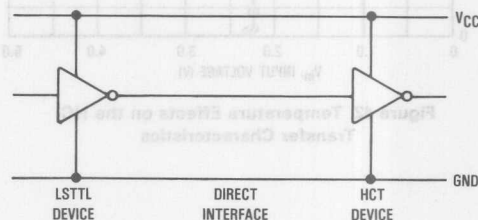


Figure 48. LSTTL to HCT Interfacing

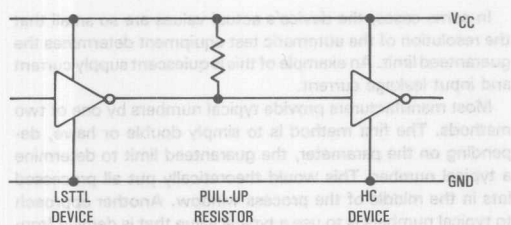


Figure 49. LSTTL to HC Interfacing

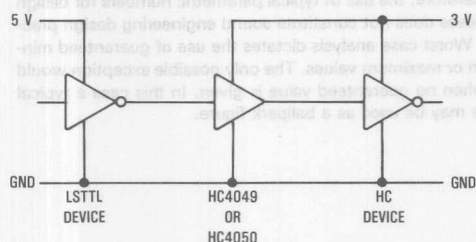
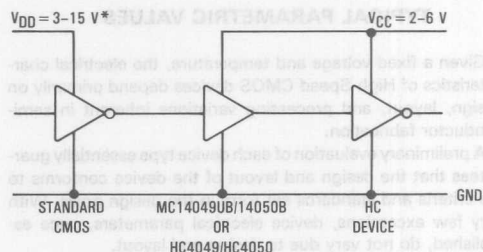


Figure 50. LSTTL to Low-Voltage HSCMOS



* V_{OH} must be greater than V_{IH} of low voltage Device; $V_{DD} = 3-18$ V may be used if interfacing to 14049UB/14050B.

Figure 51. High Voltage CMOS to HSCMOS

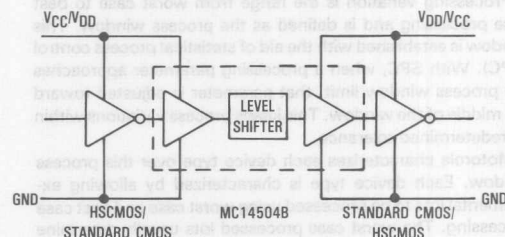


Figure 52. Up/Down Level Shifting Using the MC14504B

Table 3. Interfacing Guide

Device	Input Level	Output Level	Comments
HCXXX	CMOS	CMOS	LSTTL Functional and Pinout Equivalent Devices
HC4XXX	CMOS	CMOS	CMOS Functional and Pinout Equivalent Devices
HCUXX	CMOS	CMOS	Used in Linear Applications
HCTXXX	TTL	CMOS	HSCMOS Device with TTL-to-CMOS Input Buffering
HC4049, HC4050	$-0.5 \leq V_{in} \leq 15$ V	CMOS	High-to-Low Level Translators, CMOS Switching Levels
MC14049UB, MC14050B	$-0.5 \leq V_{in} \leq 18$ V	CMOS	Metal-Gate CMOS High-to-Low Level Translators, CMOS Switching Levels
MC14504B	CMOS or TTL	CMOS	Metal-Gate CMOS High-to-Low or Low-to-High Level Translator

Table 4. CMOS Memories and Microprocessors

CMOS Memories	CMOS Microprocessors	
MCM6147	MC68HC01	MC146805G2
MCM61L47	MC68HC03	MC146805H2
MCM68HC34	MC68HC11A8	MC1468705F2
	MC68HC11D4	MC1468705G2
	MC68HC811A2	MC68HC05C4
	MC68HC811D4	MC68HSC05C4
	MC68HC04P3	MC68HC05C8
	MC146805E2	MC68HC805C4
	MC146805F2	MC68HC000

RECOMMENDED READING

S. Craig, "Using High-Speed CMOS Logic for Microprocessor Interfacing", Application Note-868, Motorola Semiconductor Products Inc., 1982.

TYPICAL PARAMETRIC VALUES

Given a fixed voltage and temperature, the electrical characteristics of High-Speed CMOS devices depend primarily on design, layout, and processing variations inherent in semiconductor fabrication.

A preliminary evaluation of each device type essentially guarantees that the design and layout of the device conforms to the criteria and standards set forth in the design goals. With very few exceptions, device electrical parameters, once established, do not vary due to design and layout.

Of much more concern is processing variation. A digital processing line is allowed to deviate over a fairly broad processing range. This allows the manufacturer to incur reduced processing costs. These reduced processing costs are passed on to the consumer in the form of lower device prices.

Processing variation is the range from worst case to best case processing and is defined as the process window. This window is established with the aid of statistical process control (SPC). With SPC, when a processing parameter approaches the process window limit, that parameter is adjusted toward the middle of the window. This keeps process variations within a predetermined tolerance.

Motorola characterizes each device type over this process window. Each device type is characterized by allowing experimental lots to be processed using worst case and best case processing. The worst case processed lots usually determine the minimum or maximum guaranteed limit. (Whether the limit is a guaranteed minimum or maximum depends on the particular parameter being measured.)

In production, these limits are guaranteed by probe and final test and therefore appear independent of process variation to the end user. However, this does not hold true for the mean value of the total devices processed. The mean value, commonly referred to as a typical value, shifts over processing and therefore varies from lot to lot or even wafer to wafer within a lot.

As with all processing or manufacturing, the total devices being produced fit the normal distribution or bell curve of Figure 53. In order to guarantee a valid typical value, a typical number plus a tolerance, would have to be specified and tested (see Figure 54). However, this would greatly increase processing costs which would have to be absorbed by the consumer.

In some cases, the device's actual values are so small that the resolution of the automatic test equipment determines the guaranteed limit. An example of this is quiescent supply current and input leakage current.

Most manufacturers provide typical numbers by one of two methods. The first method is to simply double or halve, depending on the parameter, the guaranteed limit to determine a typical number. This would theoretically put all processed lots in the middle of the process window. Another approach to typical numbers is to use a typical value that is derived from the aforementioned experimental lots. However, neither method accurately reflects the mean value of devices any one consumer can expect to receive.

Therefore, the use of typical parametric numbers for design purposes does not constitute sound engineering design practice. Worst case analysis dictates the use of guaranteed minimum or maximum values. The only possible exception would be when no guaranteed value is given. In this case a typical value may be used as a ballpark figure.

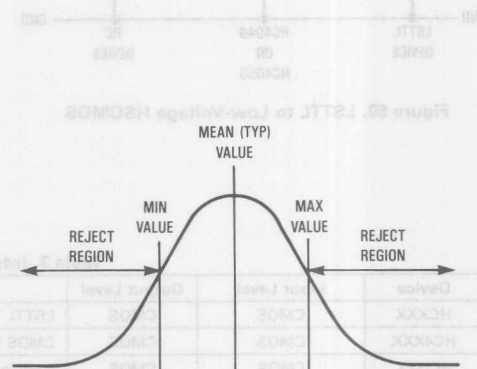


Figure 54

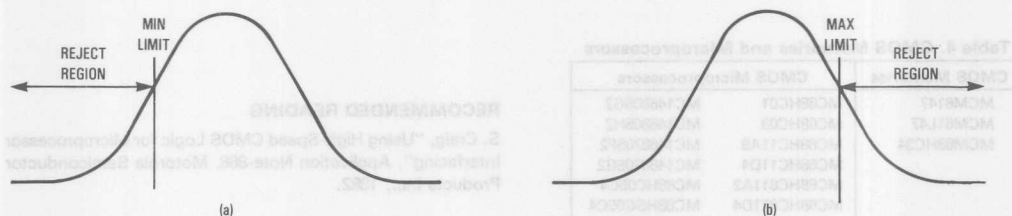


Figure 53

REDUCTION OF ELECTROMAGNETIC INTERFERENCE (EMI)

Electromagnetic interference (EMI) and radio frequency interference (RFI) are phenomena inherent in all electrical systems covering the entire frequency spectrum. Although the characteristics have been well documented, EMI remains difficult to deal with due to numerous variables. EMI should be considered at the beginning of a design, and taken into account during all stages, including production and beyond.

These entities must be present for EMI to be a factor: (1) a source of EMI, (2) a transmission medium for EMI, and (3) a receiver of EMI. Several sources include relays, FM transmitters, local oscillators in receivers, power lines, engine ignitions, arc welders, and lighting. EMI transmission paths include ground connections, cables, and the space between conductors. Some receivers of EMI are radar receivers, computers, and television receivers.

For microprocessor based equipment, the source of emissions is usually a current loop on a PC board. The chips and their associated loop areas also function as receivers of EMI. The fact is that PC boards which radiate high levels of EMI are also more likely to act as receivers of EMI.

All logic gates are potential transmitters and receivers of emissions. Noise immunity and noise margin are two criterion which measure a gate's immunity to noise which could be caused by EMI. CMOS technology, as opposed to the other commonly used logic families, offers the best value for noise margin, and is therefore an excellent choice when considering EMI.

The electric and magnetic fields associated with ICs are proportional to the current used, the current loop area, and the switching transition times. CMOS technology is preferred due to smaller currents. Also, the current loop area can be reduced by the use of surface mount packages.

In a system where several pieces of equipment are connected by cables, at least five coupling paths should be taken into account to reduce EMI. They are: (1) common ground impedance coupling (a common impedance is shared between an EMI source and receiver), (2) common-mode, field-to-cable coupling (electromagnetic fields enter the loop found by two pieces of equipment, the cable connecting them, and the ground plane), (3) differential-mode, field-to-cable coupling (electromagnetic fields enter the loop formed by two pieces of equipment and the cable connecting them), (4) crosstalk coupling (signals in one transmission line are coupled into another transmission line), and (5) a conductive path through power lines.

Shielding is a means of reducing EMI. Some of the more commonly used shields against EMI and RFI contain stainless steel fiber-filled polycarbonate, aluminum flake-filled polycarbonate/ABS coated with nickel and copper electrolysis plating or cathode sputtering, nickel coated graphite fiber, and polyester SMC with carbon-fiber veil. Several manufacturers who make conductive compounds and additives are listed below.

SHIELDING MANUFACTURERS

General Electric Co., Plastics Group, Pittsfield, MA

Mobay Chemical Corp., Pittsburg, PA

Wilson-Fiberfil International, Evansville, IN

American Cyanamid Co., Wayne, NJ

Fillite U.S.A., Inc., Huntington, WV

Transnet Corp., Columbus, OH

Motorola does not recommend, or in any way warrant the manufacturers listed here. Additionally, no claim is made that this list is by any means complete.

RECOMMENDED READING

D. White, K. Atkinson, and J. Osburn, "Taming EMI in Microprocessor Systems", *IEEE Spectrum*, Vol. 22, Number 12, Dec. 1985.

D. White and M. Mardiguian, *EMI Control Methodology and Procedures*, 1985.

H. Denny, *Grounding for the Control of EMI*.

M. Mardiguian, *How to Control Electrical Noise*.

D. White, *Shielding Design Methodology and Procedures*.

For more information on this subject, contact:

Interference Control Technologies
Don White Consultants, Inc., Subsidiary
State Route 625
P.O. Box D
Gainesville, VA 22065

HYBRID CIRCUIT GUIDELINES

High-Speed CMOS devices, when purchased in chip (die) form, are useful in hybrid circuits. Most high-speed devices are fabricated with P wells and N substrates. Therefore, the substrates should be tied to V_{CC} (+ supply).

Several devices however, are fabricated with N wells and P substrates. In this case, the substrates should be tied to GND. The best solution to alleviate confusion about the substrate is the use of nonconductive or insulative substrates. This averts the necessity of tying the substrate off to either V_{CC} or GND.

For more information on hybrid technology, contact:

International Society for Hybrid Microelectronics
P.O. Box 3255
Montgomery, AL 36109

Schmitt-trigger devices exhibit the effect of hysteresis. Hysteresis is characterized by two different switching threshold levels, one for positive-going input transitions and the other for negative-going input transitions.

Schmitt triggers offer superior noise immunity when compared to standard gates and inverters. Applications for Schmitt triggers include line receivers, sine to square wave converters, noise filters, and oscillators. Motorola offers six versatile Schmitt-trigger devices in the High-Speed CMOS logic family (see Table 5).

The typical voltage transfer characteristics of a standard CMOS inverter and a CMOS Schmitt-trigger inverter are compared in Figures 55 and 56. The singular transfer threshold of the standard inverter is replaced by two distinct thresholds in a Schmitt-trigger inverter. During a positive-going transition of V_{in} , the output begins to go low after the V_{T+} threshold is reached. During a negative-going V_{in} transition, V_{out} begins to go high after the V_{T-} threshold is reached. The difference between V_{T+} and V_{T-} is defined as V_H , the hysteresis voltage.

As a direct result of hysteresis, Schmitt-trigger circuits provide excellent noise immunity and the ability to square up signals with long rise and fall times. Positive-going input noise excursions must rise above the V_{T+} threshold before they affect the output. Similarly, negative-going input noise excursions must drop below the V_{T-} threshold before they affect the output.

The HC132 can be used as a direct replacement for the HC00 NAND gate, which does not have Schmitt-trigger capability. The HC132 has the same pin assignment as the HC00. Schmitt-trigger logic elements act as standard logic elements in the absence of noise or slow rise and fall times, making direct substitution possible.

Versatility and low cost are attractive features of CMOS Schmitt triggers. With six Schmitt triggers per HC14 package, one trigger can be used for a noise elimination application while the other five function as standard inverters. Similarly, each of the four triggers in the HC132 can be used as either Schmitt triggers or NAND gates or some combination of both.

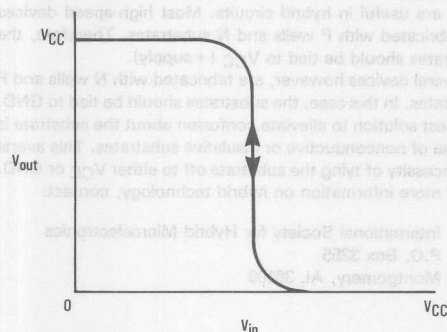


Figure 55. Standard Inverter Transfer Characteristic

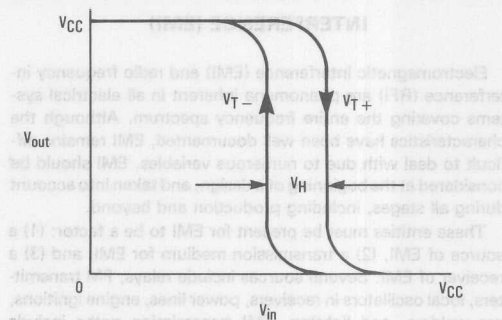


Figure 56. Schmitt-Trigger Inverter Transfer Characteristic

Table 5. Schmitt-Trigger Devices

HC14	Hex Schmitt-Trigger Inverter
HC132	Quad 2-Input NAND Gate with Schmitt-Trigger Inputs
HC9014	Nine-Wide Schmitt-Trigger Inverter
HC9015	Nine-Wide Schmitt-Trigger Noninverting Buffer
HC9114	Nine-Wide Schmitt-Trigger Inverter with Open-Drain Outputs
HC9115	Nine-Wide Schmitt-Trigger Noninverting Buffer with Open-Drain Outputs

HC vs. HCT

Motorola's High-Speed CMOS is intended to give the designer an alternative to LSTTL. HSCMOS, with the faster speed advantage over metal-gate CMOS (MC14000 series) and the lower power consumption advantage over LSTTL, is an optimum choice for new midrange designs. With the advent of high-speed CMOS microprocessors and memories, the ability to design a 100% CMOS system is now possible.

HCT devices offer a short-term solution to the TTL/NMOS-to-CMOS interface problem. To achieve this interface capability, some CMOS advantages had to be compromised. These compromises include power consumption, operating voltage range, and noise immunity.

In most cases HCT devices are drop-in replacements of TTL devices with significant advantages over the TTL devices. However, in some cases, an equivalent HCT device may not replace a TTL device without some form of circuit modification.

The wise designer uses HCT devices to perform logic level conversions only. In new designs, the designer wants all the advantages of a true CMOS system and designs using only HC devices.

OSCILLATOR DESIGN WITH HIGH-SPEED CMOS

Oscillator design is a fundamental requirement of many systems and several types are discussed in this section. In general, an oscillator is comprised of two parts: an active network and a feedback network. The active network is usually in the form of an amplifier, or an unbuffered inverter, such as the HCU04. The feedback network is mainly comprised of resistors, capacitors, and depending upon the application, a quartz crystal or ceramic resonator.

Buffered inverters are never recommended in oscillator applications due to their high gain and added propagation delay. For this reason Motorola manufactures the HCU04, which is an unbuffered hex inverter.

Oscillators for use in digital systems fall into two general categories, RC oscillators and crystal or ceramic resonator oscillators. Crystal oscillators have the best performance, but are more costly, especially for nonstandard frequencies. RC oscillators are more useful in applications where stability and accuracy are not of prime importance. Where high performance at low frequencies is desired, ceramic resonators are sometimes used.

RC OSCILLATORS

The circuit in Figure 57 shows a basic RC oscillator using the HCU04. When the input voltage of the first inverter reaches the threshold voltage, the outputs of the two inverters change state, and the charging current of the capacitor changes direction. The frequency at which this circuit oscillates depends upon $R1$ and C . The equation to calculate these component values is given in Figure 57.

Certain constraints must be met while designing this type of oscillator. Stray capacitance and inductance must be kept to a minimum by placing the passive components as close to the chip as possible. Also, at higher frequencies, the HCU04's

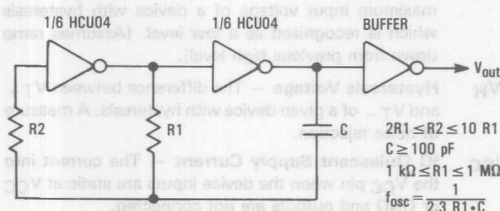


Figure 57. RC Oscillator

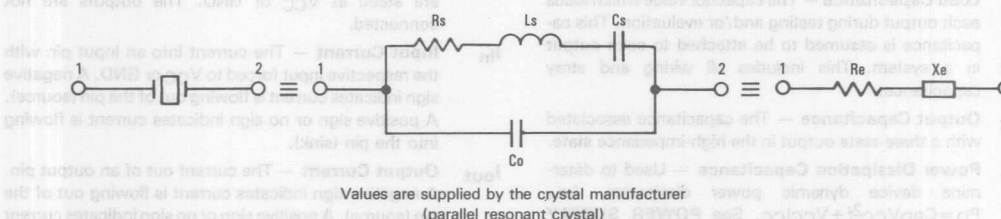


Figure 58. Equivalent Crystal Networks

propagation delay becomes a dominant effect and affects the cycle time. A polystyrene capacitor is recommended for optimum performance.

CRYSTAL OSCILLATORS

Crystal oscillators provide the required stability and accuracy which is necessary in many applications. The crystal can be modeled as shown in Figure 58.

The power dissipated in a crystal is referred to as the drive level and is specified in mW. At low drive levels, the resonant resistance of the crystal can be so large as to cause start-up problems. To overcome this problem, the amplifier (inverter) should provide enough amplification, but not too much as to overdrive the crystal.

Figure 59 shows a Pierce crystal oscillator circuit, which is a popular configuration with CMOS.

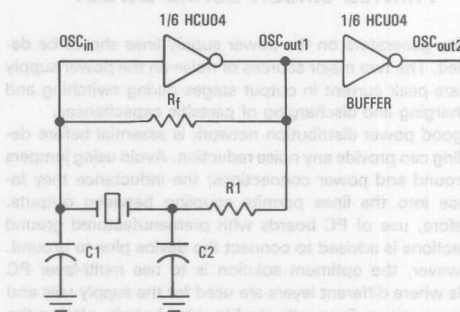


Figure 59. Pierce Crystal Oscillator Circuit

Choosing R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. $R1$ limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency at Osc Out 2. The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or $R1$ must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of $R1$.

Selecting R_f

The feedback resistor (R_f) typically ranges up to 20 M Ω . R_f determines the gain and bandwidth of the amplifier. Proper bandwidth ensures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone. R_f must be large enough so as not to affect the phase of the feedback network in an appreciable manner.

RECOMMENDED READING

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

PRINTED CIRCUIT BOARD LAYOUT

Noise generators on the power supply lines should be decoupled. The two major sources of noise on the power supply lines are peak current in output stages during switching and the charging and discharging of parasitic capacitances.

A good power distribution network is essential before decoupling can provide any noise reduction. Avoid using jumpers for ground and power connections; the inductance they introduce into the lines permits coupling between outputs. Therefore, use of PC boards with premanufactured ground connections is advised to connect the device pins to ground.

However, the optimum solution is to use multi-layer PC boards where different layers are used for the supply rails and interconnections. Even with double-sided boards, placing the power and ground lines on opposite sides of the board whenever possible is recommended. The multi-wire board is a less expensive approach than the multi-layer PC board, while retaining the same noise reduction characteristics. As a rule of thumb, there should be several ground pins per connector to give good ground distribution.

The precautions for ground lines also apply to V_{CC} lines: 1) separate power stabilization for each board; 2) isolate noise sources; and 3) avoid the use of large, single voltage regulators.

After all of these precautions, decoupling is an added measure to reduce supply noise. See the **Decoupling Capacitors** section.

GLOSSARY OF TERMS

- C_{in} Input Capacitance** — The parasitic capacitance associated with a given input pin.
- C_L Load Capacitance** — The capacitor value which loads each output during testing and/or evaluation. This capacitance is assumed to be attached to each output in a system. This includes all wiring and stray capacitance.
- C_{out} Output Capacitance** — The capacitance associated with a three-state output in the high-impedance state.
- C_{PD} Power Dissipation Capacitance** — Used to determine device dynamic power dissipation, i.e., $P_D = C_{PD}V_{CC}^2f + V_{CC}I_{CC}$. See **POWER SUPPLY SIZING** for a discussion of C_{PD} .

f_{max} Maximum Clock Frequency — The maximum clocking frequency attainable with the following input and output conditions being met:

Input Conditions — (HC) $t_r = t_f = 6$ ns, voltage swing from GND to V_{CC} with 50% duty cycle. (HCT) $t_r = t_f = 6$ ns, voltage swing from GND to 3.0 V with 50% duty cycle.

Output Conditions — (HC and HCT) waveform must swing from 10% of ($V_{OH} - V_{OL}$) to 90% of ($V_{OH} - V_{OL}$) and be functionally correct under the given load condition: $C_L = 50$ pF, all outputs.

V_{CC} Positive Supply Voltage — +dc supply voltage (referenced to GND). The voltage range over which ICs are functional.

V_{in} Input Voltage — DC input voltage (referenced to GND).

V_{out} Output Voltage — DC output voltage (referenced to GND).

V_{IH} Minimum High Level Input Voltage — The worst case voltage that is recognized by a device as the HIGH state.

V_{IL} Maximum Low Level Input Voltage — The worst case voltage that is recognized by a device as the LOW state.

V_{OH} Minimum High Level Output Voltage — The worst case high-level voltage at an output for a given output current (I_{out}) and supply voltage (V_{CC}).

V_{OL} Maximum Low Level Output Voltage — The worst case low-level voltage at an output for a given output current (I_{out}) and supply voltage (V_{CC}).

V_{T+} Positive-Going Input Threshold Voltage — The minimum input voltage of a device with hysteresis which is recognized as a high level. (Assumes ramp up from previous low level.)

V_{T-} Negative-Going Input Threshold Voltage — The maximum input voltage of a device with hysteresis which is recognized as a low level. (Assumes ramp down from previous high level.)

V_H Hysteresis Voltage — The difference between V_{T+} and V_{T-} of a given device with hysteresis. A measure of noise rejection.

I_{CC} IC Quiescent Supply Current — The current into the V_{CC} pin when the device inputs are static at V_{CC} or GND and outputs are not connected.

ΔI_{CC} Additional Quiescent Supply Current — The current into the V_{CC} pin when one of the device inputs is at 2.4 V with respect to GND and the other inputs are static at V_{CC} or GND. The outputs are not connected.

I_{in} Input Current — The current into an input pin with the respective input forced to V_{CC} or GND. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).

I_{out} Output Current — The current out of an output pin. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).

I_{IH}	Input Current (High) — The input current when the input voltage is forced to a high level.	THL	Output High-to-Low Transition Time — The time interval between the 90% and 10% voltage levels of the falling edge of a switching output.
I_{IL}	Input Current (Low) — The input current when the input voltage is forced to a low level.	t_{su}	Setup Time — The time interval immediately preceding the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative setup time indicates that the data at the input may be applied sometime after the active clock or latch transition and still be recognized. For HC devices, the setup time is measured from the 50% level of the data waveform to the 50% level of the clock or latch input waveform. For HCT devices, the setup time is measured from the 1.3 V level (with respect to GND) of the data waveform to the 1.3 V level (with respect to GND) of the clock or latch input waveform.
I_{OH}	Output Current (High) — The output current when the output voltage is at a high level.	t_h	Hold Time — The time interval immediately following the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative hold time indicates that the data at the input may be changed prior to the active clock or latch transition and still be recognized. For HC devices, the hold time is measured from the 50% level of the clock or latch input waveform to the 50% level of the data waveform. For HCT devices, the hold time is measured from the 1.3 V level (with respect to GND) of the clock or latch input waveform to the 1.3 V level (with respect to GND) of the data waveform.
I_{OL}	Output Current (Low) — The output current when the output voltage is at a low level.	t_{rec}	Recovery Time (HC) — The time interval between the 50% level of the transition from active to inactive state of an asynchronous control input and the 50% level of the active clock or latch enable edge required to guarantee proper operation of a device. (HCT) — The time interval between the 1.3 V level (with respect to GND) of the transition from active to inactive state of an asynchronous control input and the 1.3 V level (with respect to GND) of the active clock or latch edge required to guarantee proper operation of a logic device.
I_{OZ}	Three-State Leakage Current — The current into or out of a three-state output in the high-impedance state with that respective output forced to V _{CC} or GND.	t_w	Pulse Width (HC) — The time interval between 50% levels of an input pulse required to guarantee proper operation of a logic device. (HCT) — The time interval between 1.3 V levels (with respect to GND) of an input pulse required to guarantee proper operation of a logic device.
tp_{LH}	Low-to-High Propagation Delay (HC) — The time interval between the 0.5 V _{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from low level to high level. (HCT) — The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from low level to high level.	t_r	Input Rise Time (HC) — The time interval between the 10% and 90% voltage levels on the rising edge of an input signal. (HCT) — The time interval between the 0.3 V level and 2.7 V level (with respect to GND) on the rising edge of an input signal.
tp_{HL}	High-to-Low Propagation Delay (HC) — The time interval between the 0.5 V _{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from high level to low level. (HCT) — The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from high level to low level.	t_f	Input Fall Time (HC) — The time interval between the 90% and 10% voltage levels on the falling edge of an input signal. (HCT) — The time interval between the 2.7 V level and 0.3 V level (with respect to GND) on the falling edge of an input signal.
tp_{LZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 0.5 V _{CC} level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 10% level of the output waveform, with the output changing from the low level to high-impedance (off) state.		
tp_{HZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 0.5 V _{CC} level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 90% level of the output waveform, with the output changing from the high level to high-impedance (off) state.		
tp_{ZL}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between 0.5 V _{CC} level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.		
tp_{ZH}	High-Impedance to High-Level Propagation Delay (Enable Time) — The time interval between the 0.5 V _{CC} level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a high level.		
TLH	Output Low-to-High Transition Time — The time interval between the 10% and 90% voltage levels of the rising edge of a switching output.		

t _{PLH}	Output Low-to-High Transition Time — The time interval between the 50% and 50% voltage levels at the rising edge of a switching output.	t _{PHL}	Output High-to-Low Transition Time — The time interval between the 50% and 50% voltage levels at the falling edge of a switching output.	t _{OL}	Output Current (Low) — The input current when the output voltage is forced to a low level.	t _{OH}	Output Current (High) — The output current when the output voltage is at a high level.	t _{IL}	Input Current (Low) — The input current when the input voltage is forced to a low level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time interval between the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% VCC level (HCT) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high-impedance (off) state to a low level.	t _{PHZ}	High-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PLZ}	Low-Level to High-Impedance Propagation Delay (Disable Time) — The time interval between the 50% VCC level for HC devices (1.3 V with respect to GND) or HCT devices of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from the low level to high-impedance (off) state.	t _{PHZ}	High-to-Low Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from high level to low level.	t _{PLH}	Low-to-High Propagation Delay (HCT) — The time interval between the 50% VCC level of the controlling input waveform and the 50% VCC level of the output waveform, with the output changing from low level to high level.
t _{PLZ}	High-Impedance to Low-Level Propagation Delay (Enable Time) — The time								

High-Performance Silicon-Gate CMOS Quad 2-Input NAND Gate

The MC54V74HC00 is identical in pinout to the 7400. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interfaced to CMOS, NMOS, and TTL
- Operating Voltage Range: 3 to 5 V
- Low Input Current: 1 nA
- High Noise Immunity: Characteristics of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 32 FETs or 8 Equivalent Gates



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

LOGIC DIAGRAM



Data Sheets 5

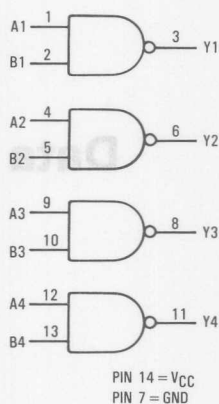
Quad 2-Input NAND Gate

High-Performance Silicon-Gate CMOS

The MC54/74HC00 is identical in pinout to the LS00. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

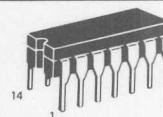
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 32 FETs or 8 Equivalent Gates

LOGIC DIAGRAM

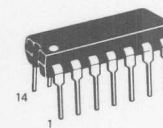


$$Y = \overline{AB}$$

MC54/74HC00



J SUFFIX
 CERAMIC
 CASE 632



N SUFFIX
 PLASTIC
 CASE 646



D SUFFIX
 SOIC
 CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	B4
Y1	3	12	A4
A2	4	11	Y4
B2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MC54/74HC00

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	
		22	pF

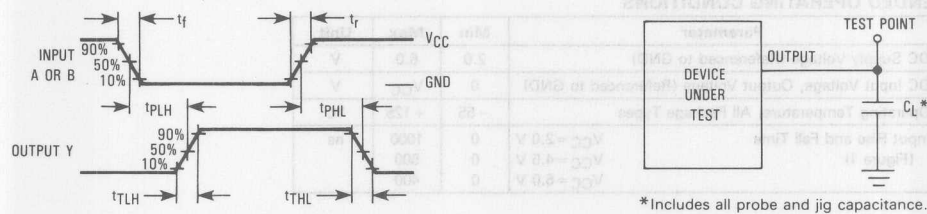
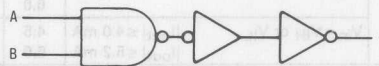


Figure 1. Switching Waveforms

Figure 2. Test Circuit

Symbol	Parameter	Test Conditions	25°C V _{CC} V	25°C pF	25°C ns	Unit
V _{IH}	Minimum High-Level Input Voltage	V _{CC} = 5.0 V to 0.1 V I _{OH} = 0 A	2.0 4.5 6.0	7.5 3.2 4.2	1.5 3.1 4.3	V
V _{IL}	Maximum Low-Level Input Voltage	V _{CC} = 5.0 V I _{OL} = 0 A	2.0 4.5 6.0	0.9 0.6 1.2	0.5 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _I = V _{IH} to V _{IL} I _{OH} = 0 A	2.0 4.5 6.0	7.5 3.2 4.2	1.5 3.1 4.3	V
V _{OL}	Maximum Low-Level Output Voltage	V _I = V _{IH} to V _{IL} I _{OL} = 0 A	2.0 4.5 6.0	0.9 0.6 1.2	0.5 0.9 1.2	V
I _{OH}	Maximum Output Sinking Current	V _I = V _{IH} to V _{IL} V _{CC} = 5.0 V	2.0 4.5 6.0	7.5 3.2 4.2	1.5 3.1 4.3	A
I _{OL}	Maximum Output Sourcing Current	V _I = V _{IH} to V _{IL} V _{CC} = 5.0 V	2.0 4.5 6.0	0.9 0.6 1.2	0.5 0.9 1.2	A

EXPANDED LOGIC DIAGRAM
(% of the Device)

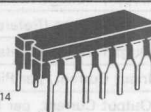


MC54/74HC02

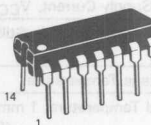
Quad 2-Input NOR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC02 is identical in pinout to the LS02. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 40 FETs or 10 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



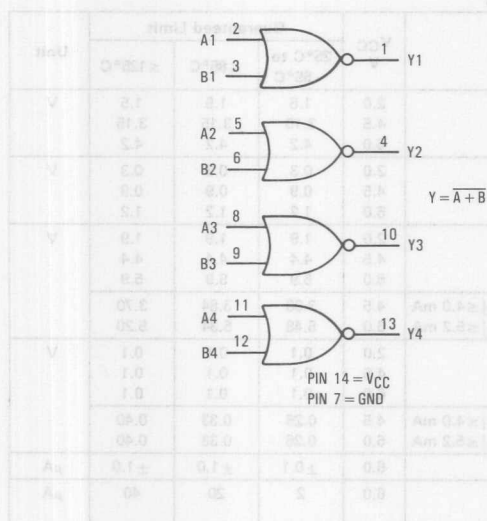
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Y1	1	14	V_{CC}
A1	2	13	Y4
B1	3	12	B4
Y2	4	11	A4
A2	5	10	Y3
B2	6	9	B3
GND	7	8	A3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		22	pF

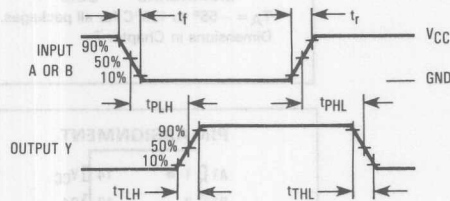
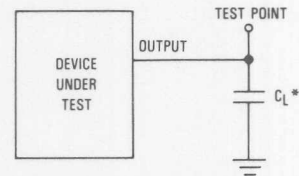
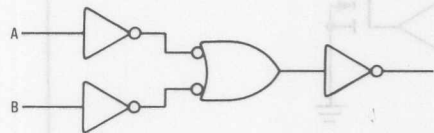


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(1/4 of the Device)

Inputs	Output
A B	Y
L L	L
L H	L
H L	L
H H	L

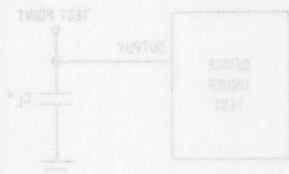
L = High Impedance

Quad 2-Input NAND Gate with Open-Drain Outputs High-Performance Silicon-Gate CMOS

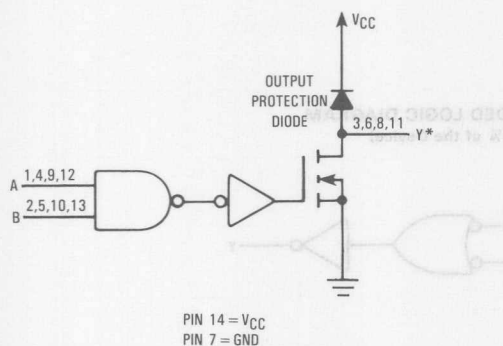
The MC54/74HC03 is identical in pinout to the LS03. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC03 NAND gate has, as its output, a high-performance MOS N-Channel transistor. This NAND gate can, therefore, with a suitable pullup resistor, be used in wired-AND applications. Having the output characteristic curves given in this data sheet, this device can be used as an LED driver or in any other application that only requires a sinking current.

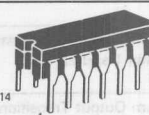
- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 28 FETs or 7 Equivalent Gates



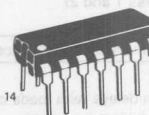
LOGIC DIAGRAM



*Denotes open-drain outputs.



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	B4
Y1	3	12	A4
A2	4	11	Y4
B2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z = High Impedance

MC54/74HC03

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V _{CC}	V
T _A	Operating Temperature, All Package Types		− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V, $I_{out} = 0$ μ A or $V_{out} = V_{CC} - 0.1$ V, R_{pu} per Figure 2	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V, $I_{out} = 0$ μ A or $V_{out} = V_{CC} - 0.1$ V, R_{pu} per Figure 2	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	6.0	2	20	40	μ A
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μ A

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC03

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLZ} , t_{PZL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		8	

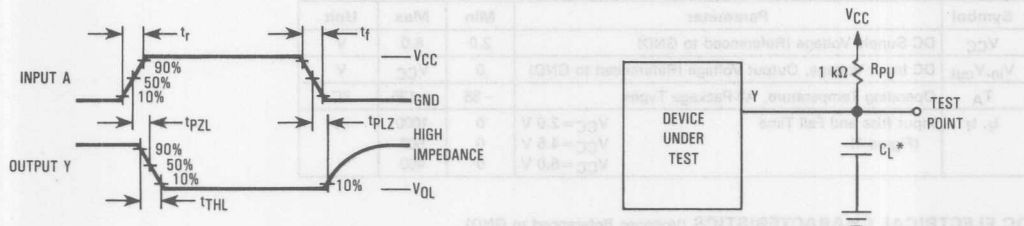
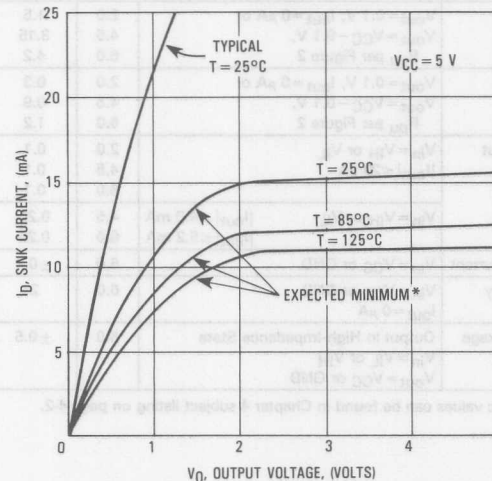


Figure 1. Switching Waveforms

*Includes all probe and jig capacitance.

Figure 2. Test Circuit

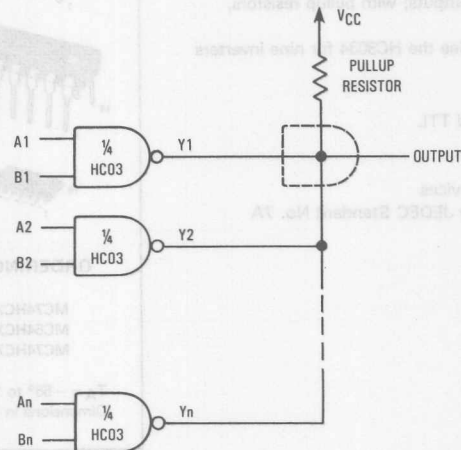


*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

TYPICAL APPLICATIONS

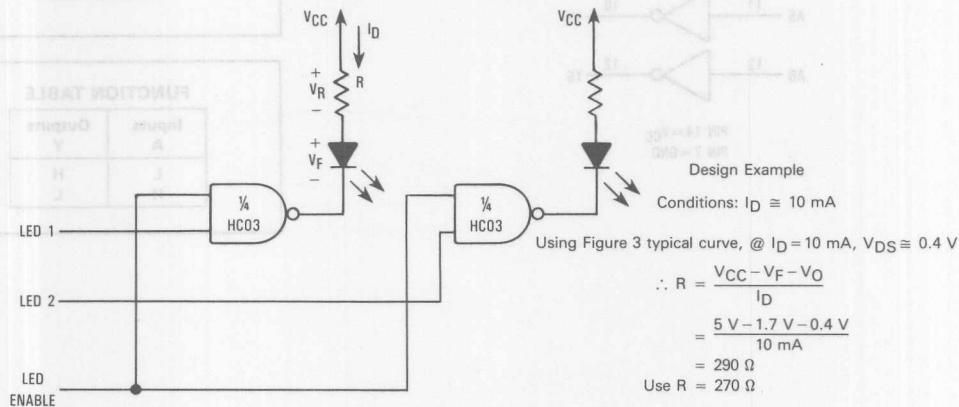
Wired AND



$$\text{Output} = Y1 \cdot Y2 \cdot \dots \cdot Yn$$

$$= A1B1 \cdot A2B2 \cdot \dots \cdot AnBn$$

LED Driver with Blanking



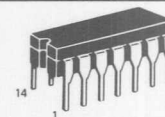
Hex Inverter

High-Performance Silicon-Gate CMOS

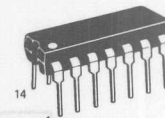
The MC54/74HC04 is identical in pinout to the LS04 and the MC14069. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six three-stage inverters. See the HC9034 for nine inverters in one package.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



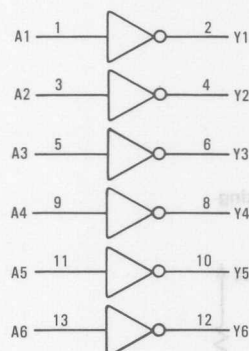
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

$$Y = \bar{A}$$

PIN ASSIGNMENT

A1	1	14	V_{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Inputs A	Outputs Y
L	H
H	L

MC54/74HC04

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC04

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		20	pF

SWITCHING WAVEFORMS

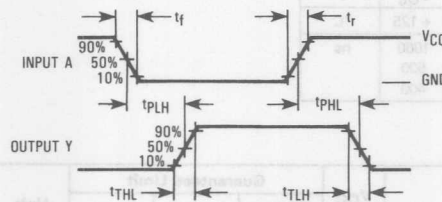
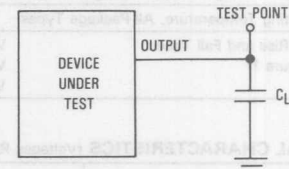


Figure 1



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM (1/6 of Device Shown)



MC54/74HCT04

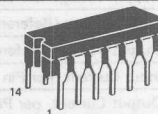
Advance Information

Hex Inverter with LSTTL- Compatible Inputs High-Performance Silicon-Gate CMOS

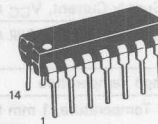
The MC54/74HCT04 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT04 is identical in pinout to the LS04.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



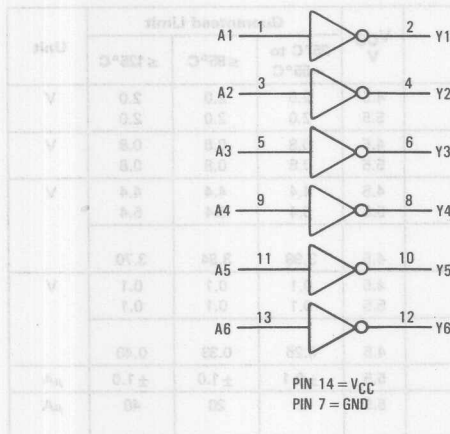
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCTXXN	Plastic
MC54HCTXXJ	Ceramic
MC74HCTXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

A1	1	14	V_{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Inputs A	Outputs Y
L	H
H	L

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$ $V_{in} = V_{IH}$ $ I_{out} \leq 4.0 \text{ mA}$	4.5 5.5 4.5	0.1 0.1 0.26	0.1 0.1 0.33	0.1 0.1 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	5.5	2	20	40	μA

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V}$, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT04

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	20	25	30	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		22	

SWITCHING WAVEFORMS

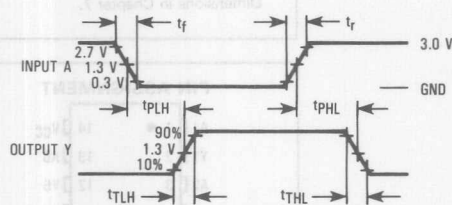
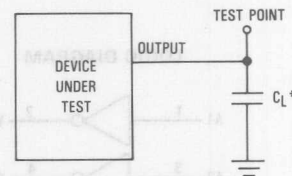


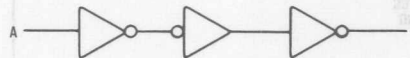
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM (1/6 of Device Shown)



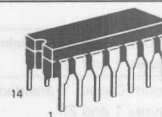
MC54/74HCU04

Hex Unbuffered Inverter High Performance Silicon-Gate CMOS

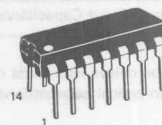
The MC54/74HCU04 is identical in pinout to the LSO4 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single-stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high-input impedance amplifier. For digital applications, the HC04 is recommended.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V; 2.5 to 6 V in Oscillator Configurations
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 12 FETs or 3 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



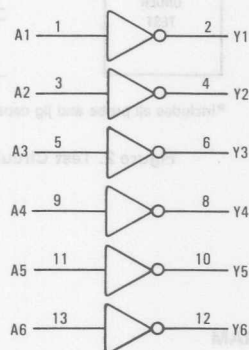
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCUXN	Plastic
MC54HCUXJ	Ceramic
MC74HCUXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



$$Y = \bar{A}$$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Inputs A	Outputs Y
L	H
H	L

MC54/74HCU04

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	No Limit	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.5 V^*$ $ I_{out} \leq 20 \mu A$	2.0	1.7	1.7	1.7	V
			4.5	3.6	3.6	3.6	
			6.0	4.8	4.8	4.8	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.5 V^*$ $ I_{out} \leq 20 \mu A$	2.0	0.3	0.3	0.3	V
			4.5	0.8	0.8	0.8	
			6.0	1.1	1.1	1.1	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = GND$ $ I_{out} \leq 20 \mu A$	2.0	1.8	1.8	1.8	V
			4.5	4.0	4.0	4.0	
			6.0	5.5	5.5	5.5	
		$V_{in} = GND$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	3.86	3.76	3.70	
			6.0	5.36	5.26	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{CC}$ $ I_{out} \leq 20 \mu A$	2.0	0.2	0.2	0.2	V
			4.5	0.5	0.5	0.5	
			6.0	0.5	0.5	0.5	
		$V_{in} = V_{CC}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	0.32	0.37	0.40	
			6.0	0.32	0.37	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

*For $V_{CC} = 2.0 \text{ V}$, $V_{out} = 0.2 \text{ V}$ or $V_{CC} - 0.2 \text{ V}$.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	pF
		15	

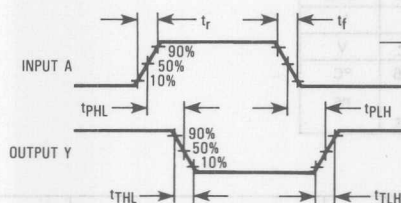
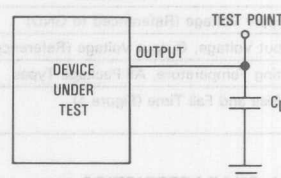
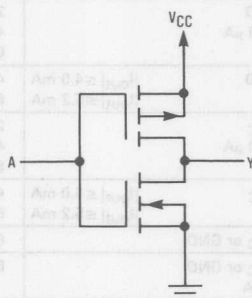


Figure 1. Switching Waveforms



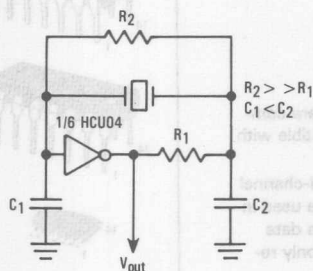
*Includes all probe and jig capacitance.

**LOGIC DETAIL
(1/6 of Device Shown)**

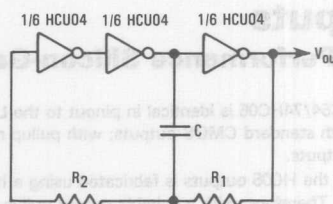


TYPICAL APPLICATIONS

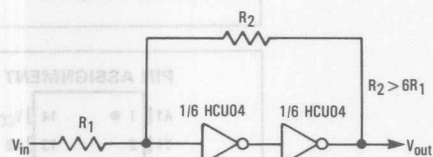
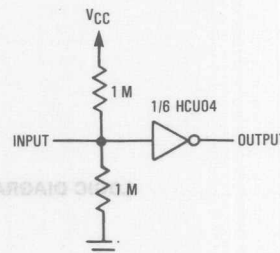
Crystal Oscillator



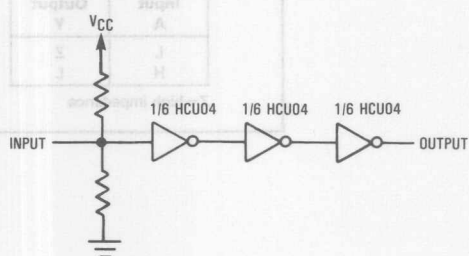
Stable RC Oscillator



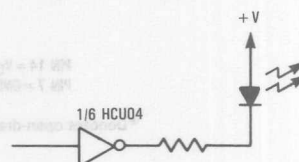
Schmitt Trigger

High Input Impedance Single-Stage Amplifier
with a 2 to 6 V Supply Range

Multi-Stage Amplifier



LED Driver



For reduced power supply current, use high-efficiency LEDs such as the Hewlett-Packard HLMP series or equivalent.

Product Preview

Hex Inverter with Open-Drain Outputs

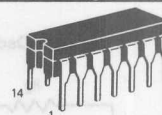
High-Performance Silicon-Gate CMOS

The MC54/74HC05 is identical in pinout to the LS05. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

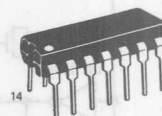
Each of the HC05 outputs is fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, this gate can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads — with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates

MC54/74HC05



J SUFFIX
 CERAMIC
 CASE 632



N SUFFIX
 PLASTIC
 CASE 646



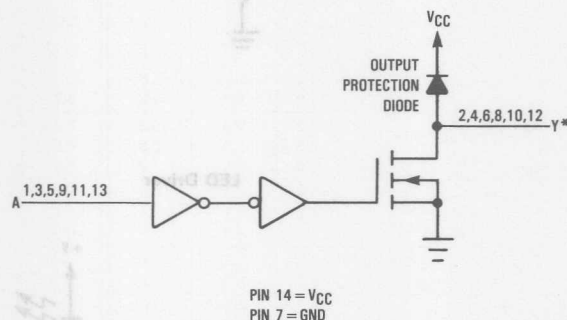
D SUFFIX
 SOIC
 CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



*Denotes open-drain outputs.

PIN ASSIGNMENT

A1	1	14	V_{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Input A	Output Y
L	Z
H	L

Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74HC05

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ R_{pu} per Figure 2	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA
I_{OZ}	Maximum Output Leakage Current	$A = V_{IL}$ $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Projected Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
tpLZ, tpZL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		TBD	

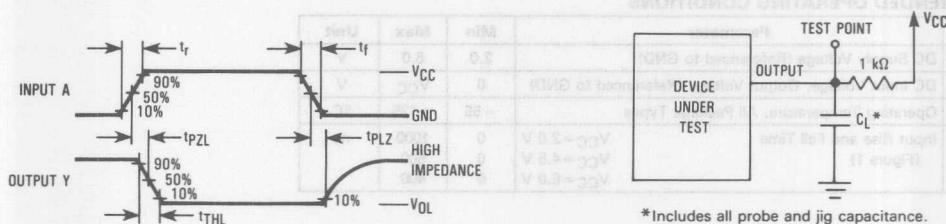
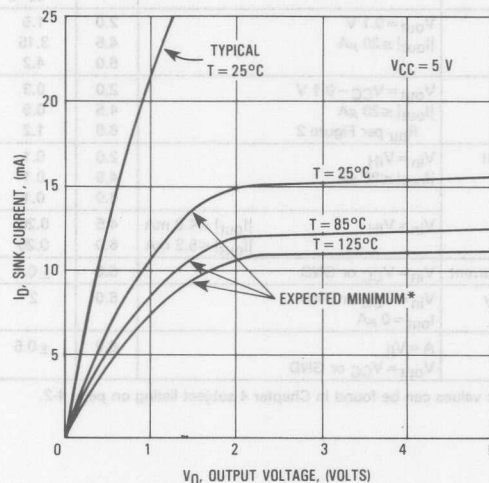


Figure 1. Switching Waveforms

Figure 2. Test Circuit

5



*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

MC54/74HCT05

Product Preview

Hex Inverter with Open-Drain Outputs and LSTTL-Compatible Inputs

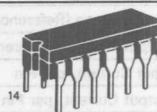
High-Performance Silicon-Gate CMOS

The MC54/74HCT05 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

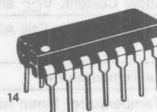
The HCT05 is identical in pinout to the LS05.

Each of the HCT05 outputs is fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, this gate can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads — with Suitable Pullup Resistor
- TTL/NMOS-Compatible Input Levels
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 632**



**N SUFFIX
PLASTIC
CASE 646**



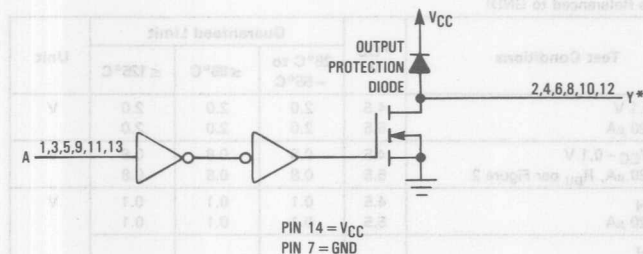
**D SUFFIX
SOIC
CASE 751A**

ORDERING INFORMATION

MC74HCTXXN	Plastic
MC54HCTXXJ	Ceramic
MC74HCTXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



*Denotes open-drain outputs.

PIN ASSIGNMENT

A1	1	14	VCC
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Input A	Output Y
L	Z
H	L

Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$, R_{PU} per Figure 2	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 4.0 \text{ mA}$	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	5.5	2	20	40	μA
I_{OZ}	Maximum Output Leakage Current	$A = V_{IL}$ $V_{out} = V_{CC}$ or GND	5.5	± 0.5	± 5.0	± 10.0	μA

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V}$, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT05

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Projected Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLZ}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	22	28	33	ns
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	pF
		TBD	

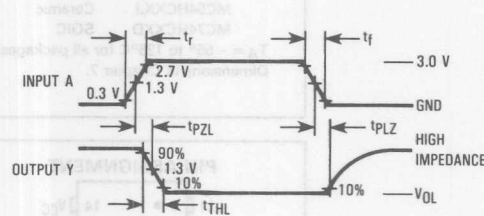
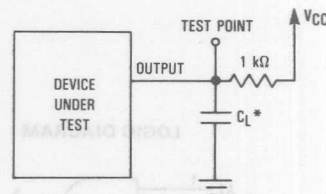
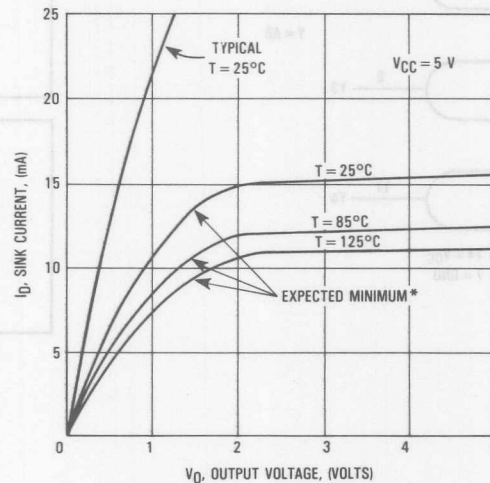


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit



*The expected minimum curves are not guarantees, but are design aids.

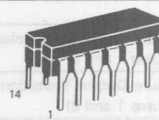
Figure 3. Open-Drain Output Characteristics

Quad 2-Input AND Gate

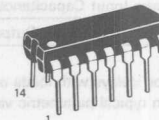
High-Performance Silicon-Gate CMOS

The MC54/74HC08 is identical in pinout to the LS08. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 24 FETs or 6 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



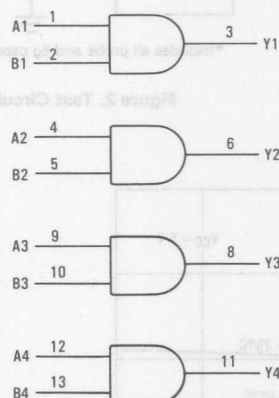
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	B4
Y1	3	12	A4
A2	4	11	Y4
B2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

MC54/74HC08

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

Ceramic DIP: - 10 mW/°C from 100° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	- 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400 ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to - 55°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC08

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		20	

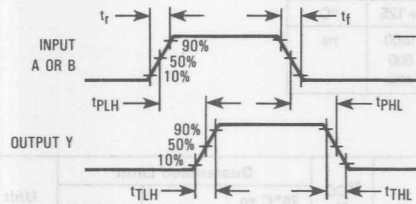


Figure 1. Switching Waveforms

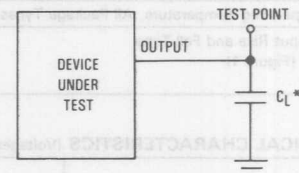
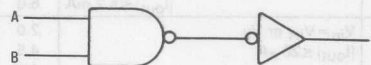


Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM (% of the Device)

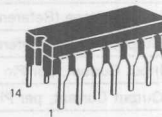


MC54/74HC10

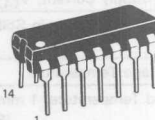
Triple 3-Input NAND Gate High-Performance Silicon-Gate CMOS

The MC54/74HC10 is identical in pinout to the LS10. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



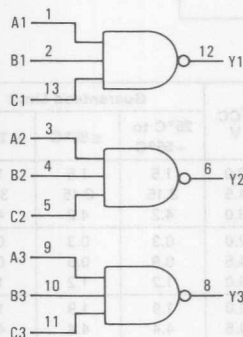
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN Plastic
 MC54HCXXJ Ceramic
 MC74HCXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



$$Y = \overline{ABC}$$

PIN 14 = V_{CC}
 PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	C1
A2	3	12	Y1
B2	4	11	C2
C2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

FUNCTION TABLE

Inputs			Output
A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

	Parameter	value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

†Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		25	

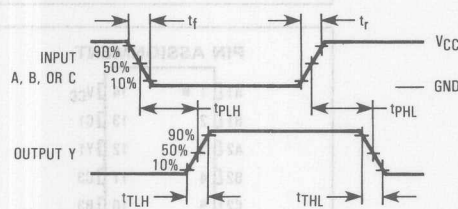
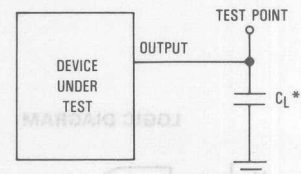


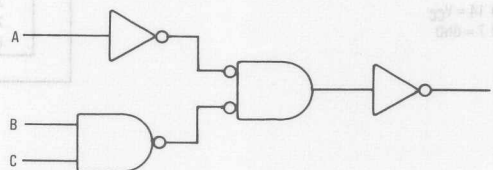
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

FUNCTION TABLE				
Output Y	A	B	C	
L	X	X	L	
L	L	X	L	
L	X	L	L	
L	H	H	H	

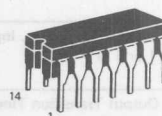
EXPANDED LOGIC DIAGRAM
(1/3 of the Device)

MC54/74HC11

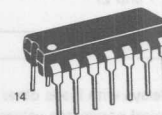
Triple 3-Input AND Gate High-Performance Silicon-Gate CMOS

The MC54/74HC11 is identical in pinout to the LS11. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



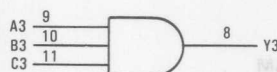
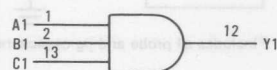
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN Plastic
 MC54HCXXJ Ceramic
 MC74HCXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
 PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	C1
A2	3	12	Y1
B2	4	11	C3
C2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

FUNCTION TABLE

Inputs			Output
A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

MC54/74HC11

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

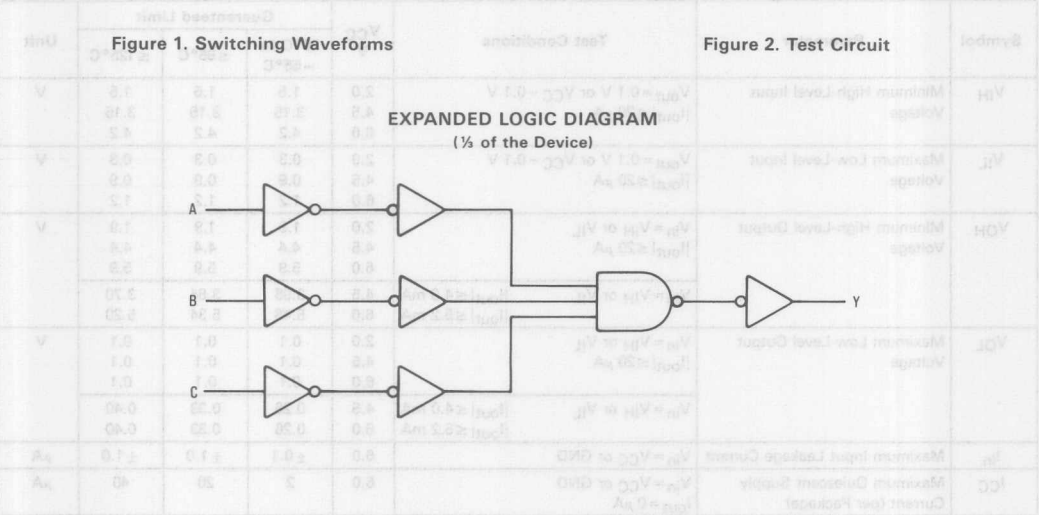
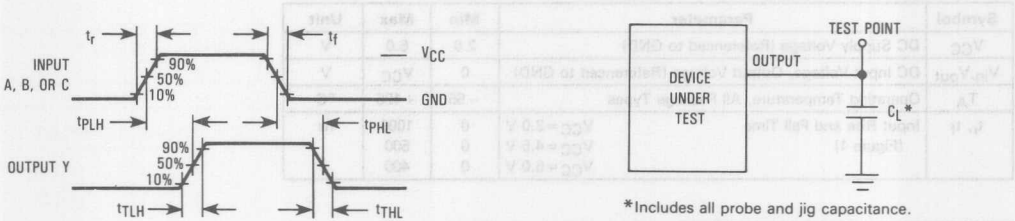
Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

- NOTES:
- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
 - Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		27	



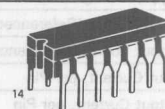
MC54/74HC14

Hex Schmitt-Trigger Inverter High-Performance Silicon-Gate CMOS

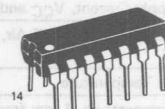
The MC54/74HC14 is identical in pinout to the LS14, LS04, and HC04. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC54/74HC14 is useful to "square up" slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HC14 finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



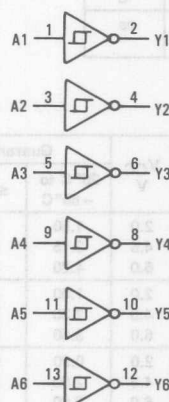
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



$$Y = \bar{A}$$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	No Limit*	ns

*When $V_{in} \approx 50\% V_{CC}$, $I_{CC} > 1$ mA.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{T+max}	Maximum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V_{T+min}	Minimum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.00 2.30 3.00	0.95 2.25 2.95	0.95 2.25 2.95	V
V_{T-max}	Maximum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.90 2.00 2.60	0.95 2.05 2.65	0.95 2.05 2.65	V
V_{T-min}	Minimum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.30 0.90 1.20	0.30 0.90 1.20	0.30 0.90 1.20	V
V_{Hmax} Note 2	Maximum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.20 2.25 3.00	1.20 2.25 3.00	1.20 2.25 3.00	V
V_{Hmin} Note 2	Minimum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.20 0.40 0.50	0.20 0.40 0.50	0.20 0.40 0.50	V

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- $V_{Hmin} > (V_{T+min}) - (V_{T-max})$; $V_{Hmax} = (V_{T+max}) - (V_{T-min})$.

MC54/74HC14

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{OH}	Minimum High-Level Output Voltage	V _{in} ≤ V _{T- min} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} ≤ V _{T- min} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} ≥ V _{T+ max} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} ≥ V _{T+ max} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	2	20	40	μA

NOTES:

1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
2. V_{Hmin} > (V_{T+ min}) - (V_{T- max}); V_{Hmax} = (V_{T+ max}) - (V_{T- min}).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		22	

5

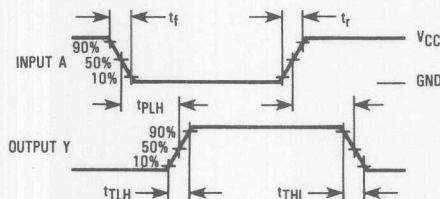
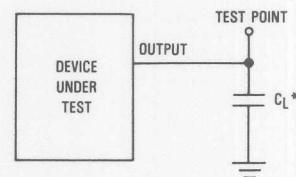


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit*

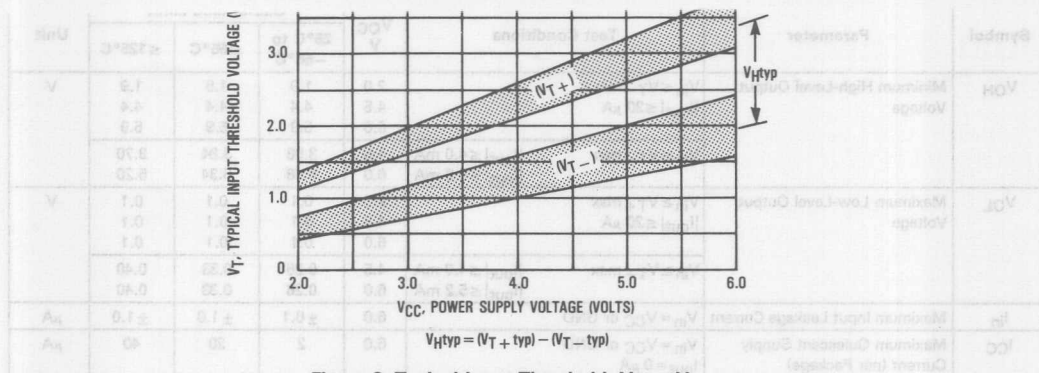


Figure 3. Typical Input Threshold, V_{T+} , V_{T-} Versus Power Supply Voltage

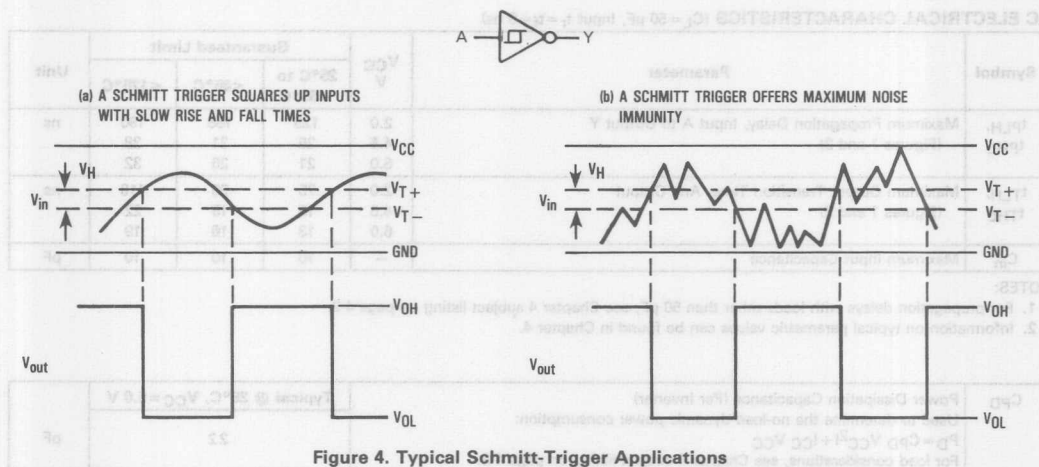


Figure 4. Typical Schmitt-Trigger Applications

5

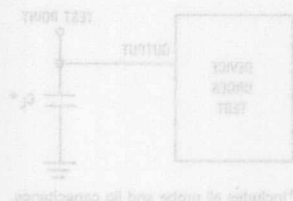


Figure 5. Test Circuit

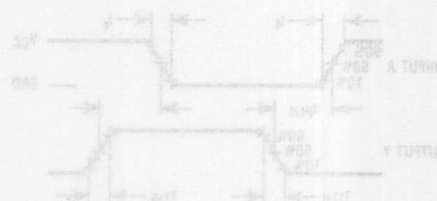


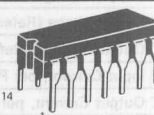
Figure 7. Switching Waveforms

MC54/74HC20

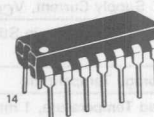
Dual 4-Input NAND Gate High-Performance Silicon-Gate CMOS

The MC54/74HC20 is identical in pinout to the LS20. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: $1 \mu\text{A}$
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 28 FETs or 7 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 632**



**N SUFFIX
PLASTIC
CASE 646**



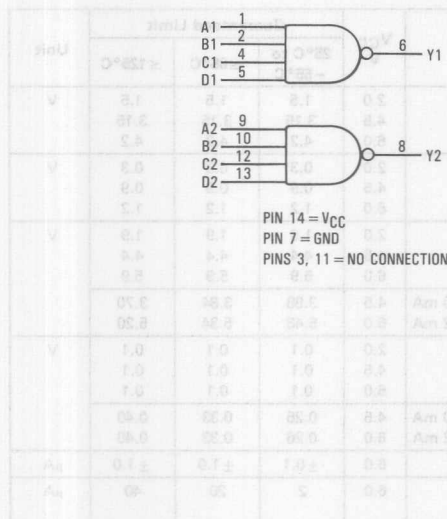
**D SUFFIX
SOIC
CASE 751A**

ORDERING INFORMATION

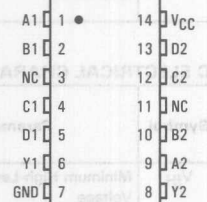
MC74HCXXN Plastic
MC54HCXXJ Ceramic
MC74HCXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Output
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	– 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A, B, C, or D to Output Y (Figures 1 and 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		26	

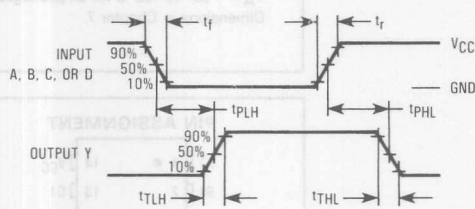
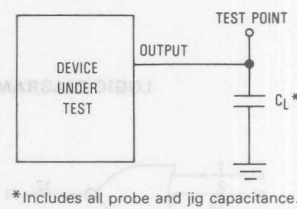


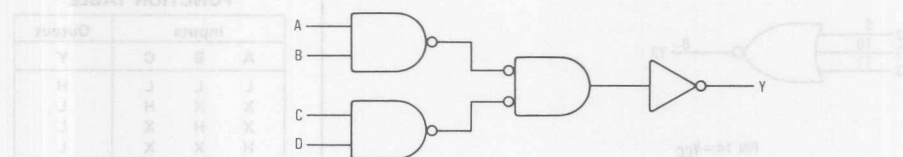
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
($\frac{1}{2}$ of the Device)

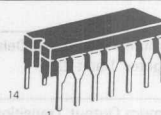


Triple 3-Input NOR Gate

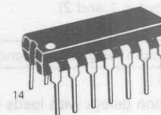
High-Performance Silicon-Gate CMOS

The MC54/74HC27 is identical in pinout to the LS27. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



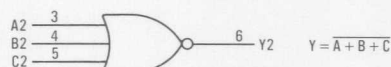
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

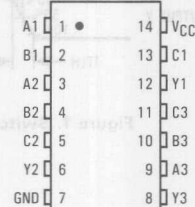
$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

MC54/74HC27

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC27

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		27	pF

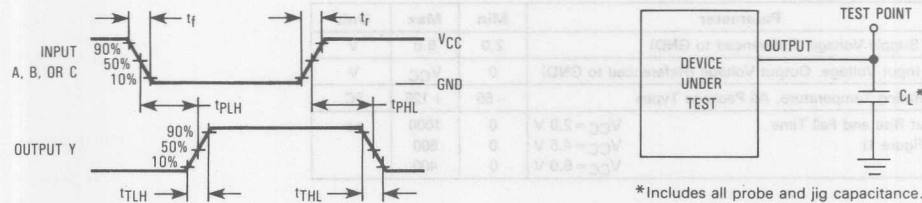
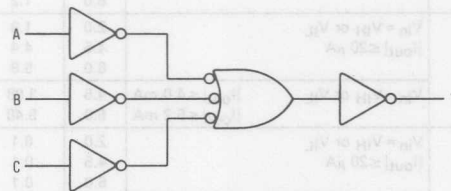


Figure 1. Switching Waveforms

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM (% of the Device)

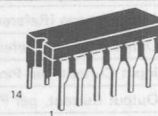


MC54/74HC30

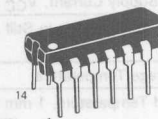
8-Input NAND Gate High-Performance Silicon-Gate CMOS

The MC54/74HC30 is identical in pinout to the LS30. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 32 FETs or 8 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



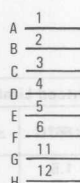
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



$$Y = \overline{ABCDEFGH}$$

PINS 9, 10, 13 = NO CONNECTION

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A	1	14	V_{CC}
B	2	13	NC
C	3	12	H
D	4	11	G
E	5	10	NC
F	6	9	NC
GND	7	8	Y

NC = NO CONNECTION

FUNCTION TABLE

Inputs A through H	Output Y
All inputs H	L
One or more inputs L	H

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to –55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$	pF
		27	

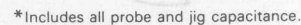
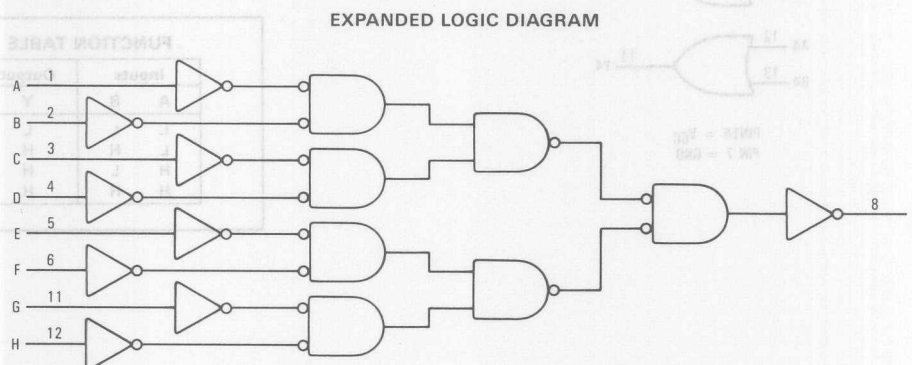


Figure 2. Test Circuit

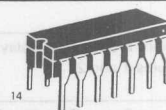


MC54/74HC32

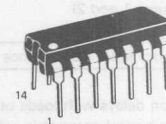
Quad 2-Input OR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC32 is identical in pinout to the LS32. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



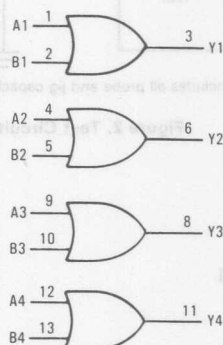
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN Plastic
 MC54HCXXJ Ceramic
 MC74HCXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

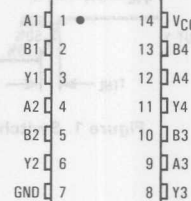
LOGIC DIAGRAM



$$Y = A + B$$

PIN14 = V_{CC}
 PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

MC54/74HC32

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

Ceramic DIP: - 10 mW/°C from 100° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	- 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to - 55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	
		20	pF

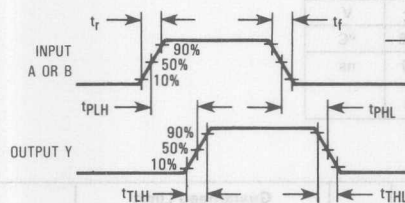
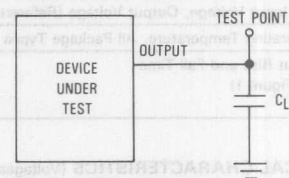


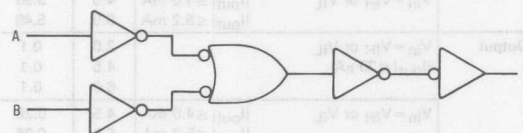
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

**EXPANDED LOGIC DIAGRAM
(% of the Device)**



MC54/74HC34

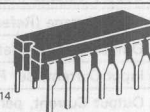
Product Preview

Hex Noninverting Buffer

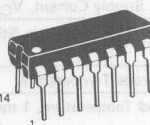
High-Performance Silicon-Gate CMOS

The MC54/74HC34 is identical in pinout to the HC04 and LS04, but the HC34 has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



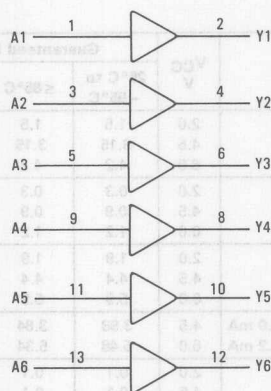
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Input A	Output Y
L	L
H	H

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400 ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Projected Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		TBD	

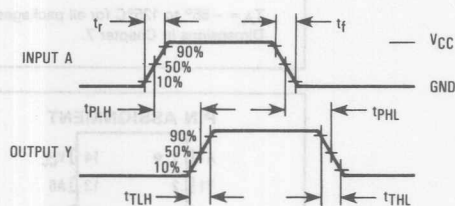
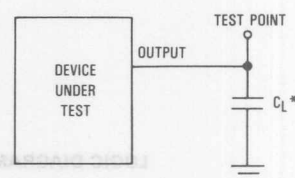


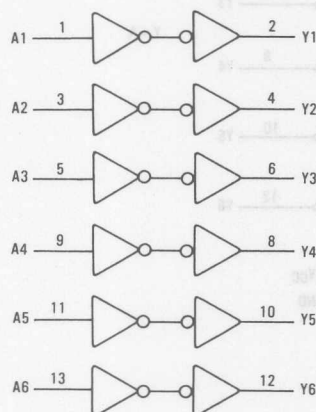
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM



Product Preview

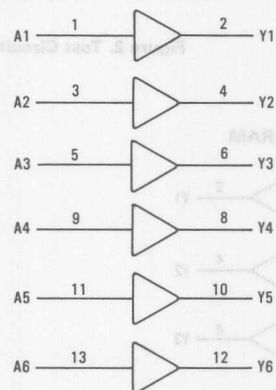
Hex Noninverting Buffer with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT34 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT34 is identical in pinout to the LS04 and HCT04, but the HCT34 has non-inverting outputs.

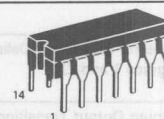
- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates

LOGIC DIAGRAM

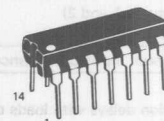


PIN 14 = V_{CC}

PIN 7 = GND



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCTXXN	Plastic
MC54HCTXXJ	Ceramic
MC74HCTXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

A1	1	14	V_{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Input A	Output Y
L	L
H	H

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74HCT34

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V $ I_{out} \leq 20$ μ A	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20$ μ A	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 4.0$ mA	4.5	3.98	3.84	3.70	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 20$ μ A	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	
		$V_{in} = V_{IL}$ $ I_{out} \leq 4.0$ mA	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	5.5	± 0.1	± 1.0	± 1.0	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	5.5	2	20	40	μ A

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4$ V, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0$ μ A	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT34

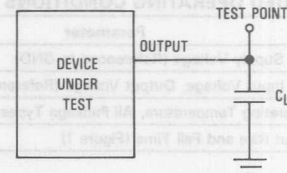
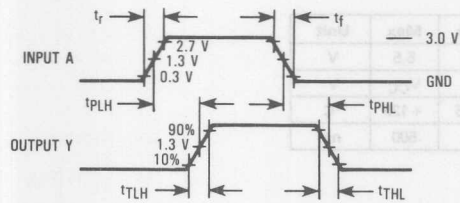
AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Projected Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	22	28	33	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = CPD \cdot V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	pF
		TBD	

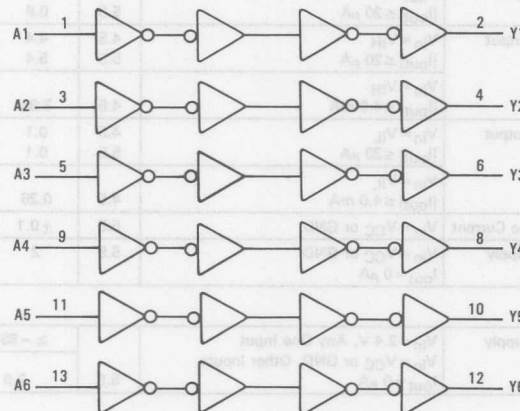


*Includes all probe and jig capacitance.

Figure 1. Switching Waveforms

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM



MC54/74HC35

Product Preview

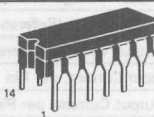
Hex Noninverting Buffer with Open-Drain Outputs

High-Performance Silicon-Gate CMOS

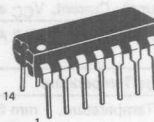
The MC54/74HC35 is identical in pinout to the LS05 and HC05, but the HC35 has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each of the HC35 outputs is fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, this gate can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads — with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

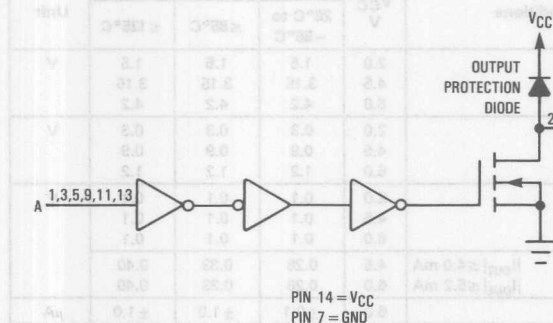
A1	1	14	V _{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Input A	Output Y
L	L
H	Z

Z = high impedance

LOGIC DIAGRAM



*Denotes open-drain outputs.

5

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125° C

Ceramic DIP: -10 mW/°C from 100° to 125° C

SOIC Package: -7 mW/°C from 65° to 125° C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0$ V 0 $V_{CC} = 4.5$ V 0 $V_{CC} = 6.0$ V 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A R_{pu} per Figure 2	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	6.0	2	20	40	μ A
I_{OZ}	Maximum Output Leakage Current	$A = V_{IH}$ $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μ A

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Projected Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLZ} , t_{PZL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	
		TBD	pF

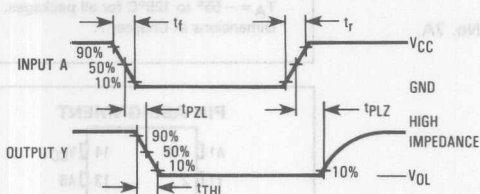
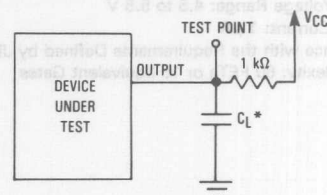
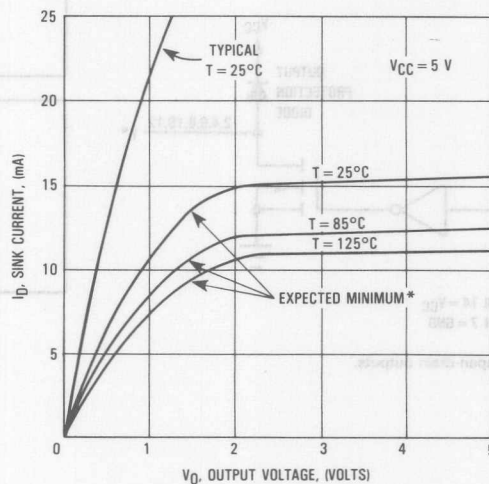


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit



*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

MC54/74HCT35

Product Preview

Hex Noninverting Buffer with Open-Drain Outputs and LSTTL- Compatible Inputs

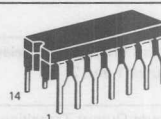
High-Performance Silicon-Gate CMOS

The MC54/74HCT35 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

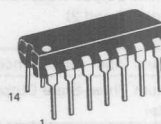
The HCT35 is identical in pinout to the LS05 and HCT05, but the HCT35 has non-inverting outputs.

Each of the HCT35 outputs is fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, this gate can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

- Output Drive Capability: 10 LSTTL Loads — with Suitable Pullup Resistor
- TTL/NMOS-Compatible Input Levels
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 60 FETs or 15 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCTXXN	Plastic
MC54HCTXXJ	Ceramic
MC74HCTXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

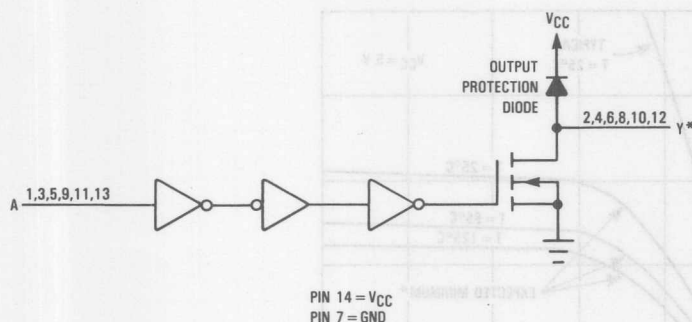
A1	1	14	V _{CC}
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

FUNCTION TABLE

Input A	Output Y
L	L
H	Z

Z = high impedance

LOGIC DIAGRAM



*Denotes open-drain outputs.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74HCT35

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu A$, R_{pu} per Figure 2	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V $ I_{out} \leq 20 \mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 4.0$ mA	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	5.5	2	20	40	μA
I_{OZ}	Maximum Output Leakage Current	$A = V_{IH}$ $V_{out} = V_{CC}$ or GND	5.5	± 0.5	± 5.0	± 10.0	μA

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4$ V, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu A$	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

Symbol	Parameter	Projected Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t _{PLZ} , t _{PZL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	24	30	36	ns
t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		TBD	

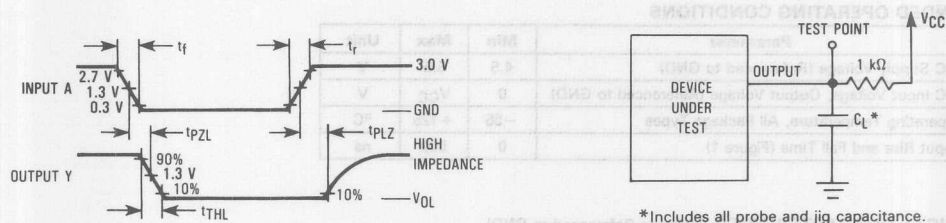
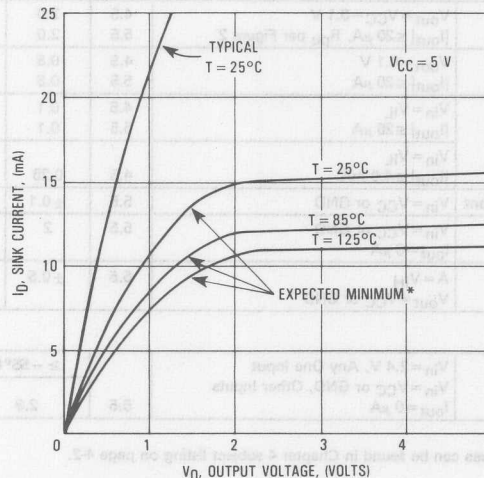


Figure 1. Switching Waveforms

Figure 2. Test Circuit



*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

MC54/74HC42

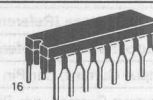
1-of-10 Decoder

High-Performance Silicon-Gate CMOS

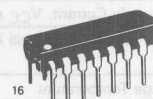
The MC54/74HC42 is identical in pinout to the LS42. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC42 decodes a BCD Address to one-of-ten active-low outputs. For Address inputs with a hexadecimal equivalent greater than 9, all outputs, Y0-Y9, remain high (inactive).

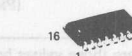
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 104 FETs or 26 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 620**



**N SUFFIX
PLASTIC
CASE 648**



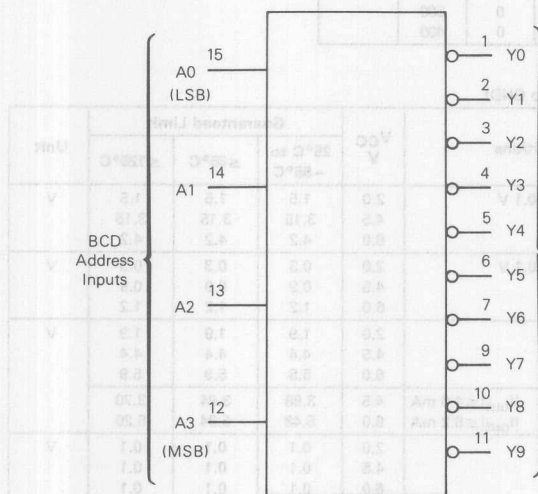
**D SUFFIX
SOIC
CASE 751**

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Y0	1	16	VCC
Y1	2	15	A0
Y2	3	14	A1
Y3	4	13	A2
Y4	5	12	A3
Y5	6	11	Y9
Y6	7	10	Y8
GND	8	9	Y7

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC42

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		65	

FIGURE 1 — SWITCHING WAVEFORMS

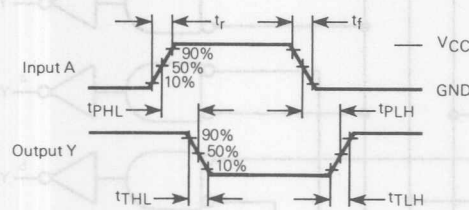
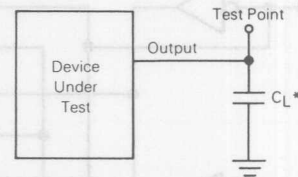


FIGURE 2 — TEST CIRCUIT



* Includes all probe and jig capacitance.

FUNCTION TABLE

Inputs				Outputs									
A3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

INPUTS

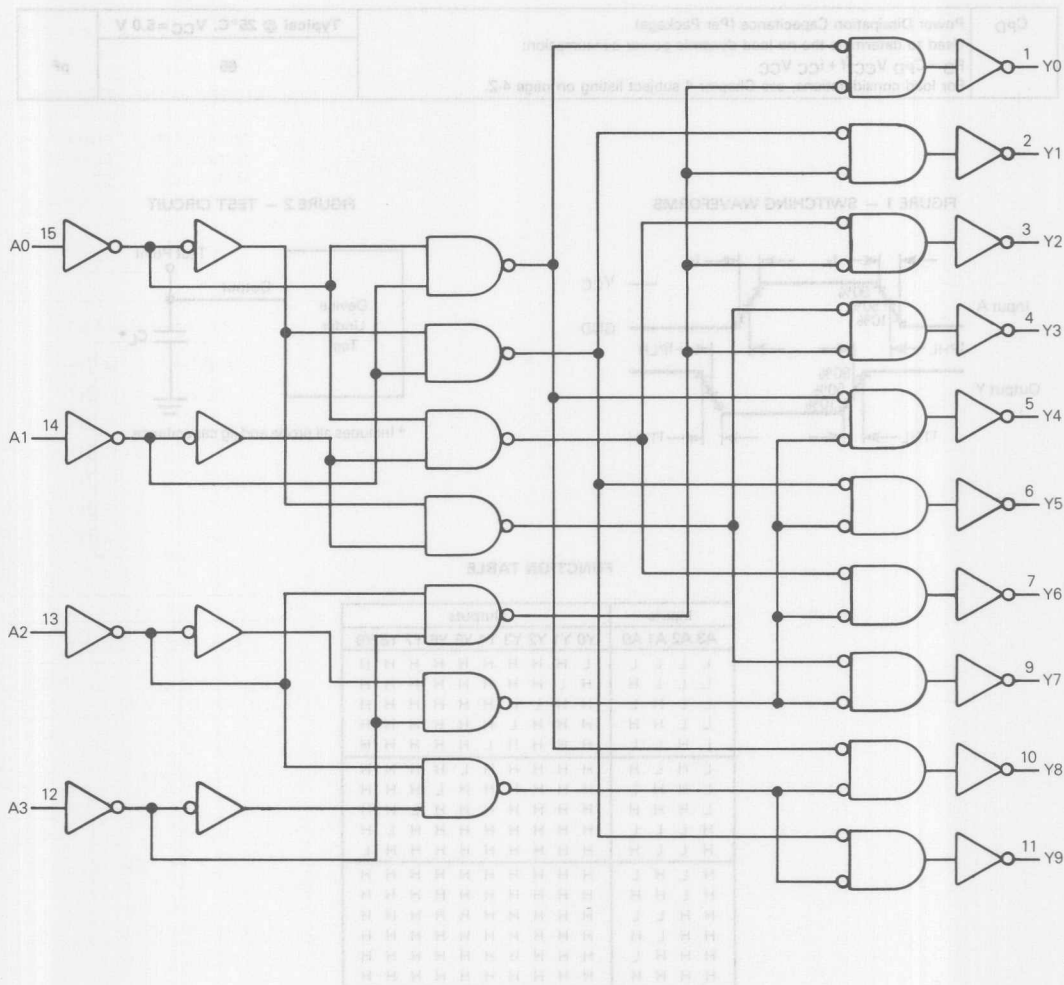
A0, A1, A2, A3, (PINS 15, 14, 13, 12) — BCD Address Inputs. The BCD address present at these inputs determines which output is active-low. These inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. Addresses with a hexadecimal equivalent

number greater than nine are not decoded.

OUTPUTS

Y0-Y9 (PINS 1-7, 9-11) — Active-Low Decoded Outputs. These outputs assume a low level when addressed and remain high when not addressed.

EXPANDED LOGIC DIAGRAM

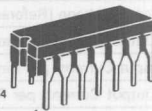


MC54/74HC51

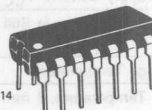
2-Wide, 2-Input/2-Wide, 3-Input AND-NOR Gates High-Performance Silicon-Gate CMOS

The MC54/74HC51 is identical in pinout to the LS51. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



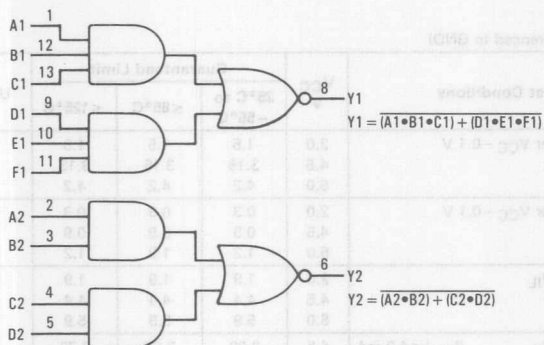
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
A2	2	13	C1
B2	3	12	B1
C2	4	11	F1
D2	5	10	E1
Y2	6	9	D1
GND	7	8	Y1

FUNCTION TABLES

Inputs						Output
A1	B1	C1	D1	E1	F1	Y1
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

Inputs				Output
A2	B2	C2	D2	Y2
H	H	X	X	L
X	X	H	H	L
All other combinations				H

MC54/74HC51

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Section) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		23	

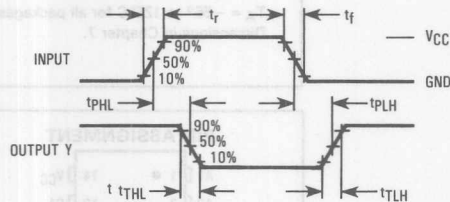
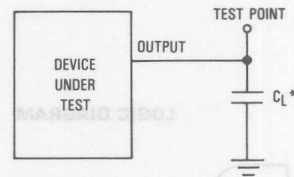


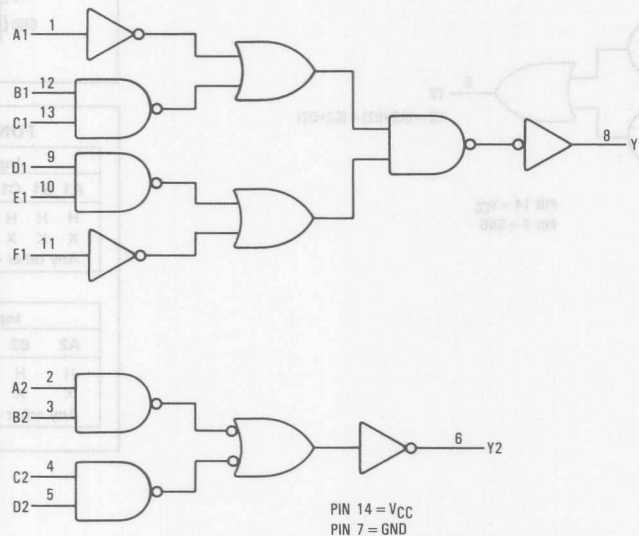
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM

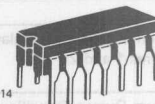


2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates

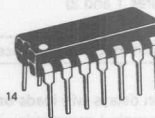
High-Performance Silicon-Gate CMOS

The MC54/74HC58 is identical to the MC54/74HC51 except that the outputs are inverted. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 632**



**N SUFFIX
PLASTIC
CASE 646**



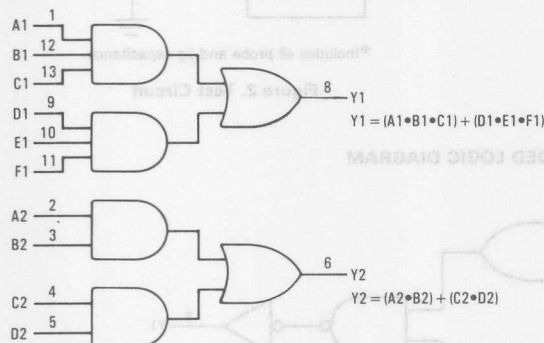
**D SUFFIX
SOIC
CASE 751A**

ORDERING INFORMATION

MC74HCXXN Plastic
MC54HCXXJ Ceramic
MC74HCXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
A2	2	13	C1
B2	3	12	B1
C2	4	11	F1
D2	5	10	E1
Y2	6	9	D1
GND	7	8	Y1

FUNCTION TABLES

Inputs						Output
A1	B1	C1	D1	E1	F1	Y1
H	H	H	X	X	X	H
X	X	X	H	H	H	H
Any other combination						L

Inputs				Output
A2	B2	C2	D2	Y2
H	H	X	X	H
X	X	H	H	H
Any other combination				L

MC54/74HC58

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC58

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Section) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		22	pF

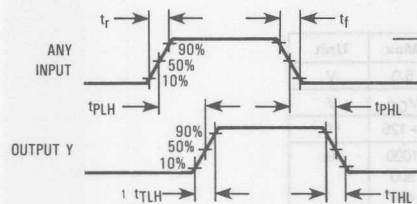
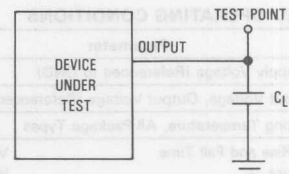


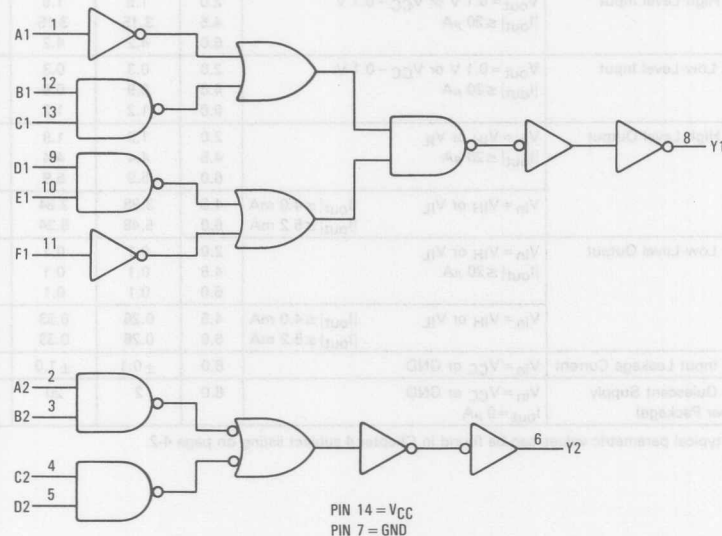
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM



MC54/74HC73

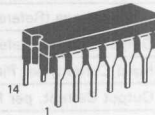
Dual J-K Flip-Flop with Reset High-Performance Silicon-Gate CMOS

The MC54/74HC73 is identical in pinout to the LS73. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

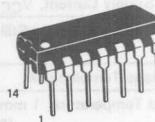
Each flip-flop is negative-edge clocked and has an active-low asynchronous reset.

The MC54/74HC73 is identical in function to the HC107, but has a different pinout.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 632**



**N SUFFIX
PLASTIC
CASE 646**



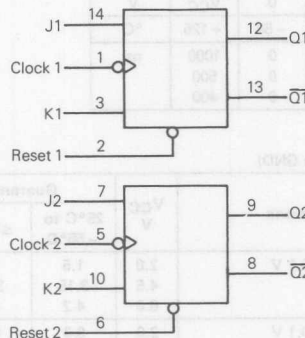
**D SUFFIX
SOIC
CASE 751A**

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



Pin 4 = V_{CC}
Pin 11 = GND

PIN ASSIGNMENT

Clock 1	1	14	J1
Reset 1	2	13	$\overline{Q1}$
K1	3	12	Q1
V_{CC}	4	11	GND
Clock 2	5	10	K2
Reset 2	6	9	Q2
J2	7	8	$\overline{Q2}$

FUNCTION TABLE

Inputs				Outputs	
Reset	Clock	J	K	Q	\overline{Q}
L	X	X	X	L	H
H	\sim	L	L	No Change	
H	\sim	L	H	L	H
H	\sim	H	L	H	L
H	\sim	H	H	Toggle	
H	L	X	X	No Change	
H	H	X	X	No Change	
H	\sim	X	X	No Change	

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	- 65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

Ceramic DIP: - 10 mW/°C from 100° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to - 55°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC54/74HC73

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Reset to Q or \bar{Q} (Figures 2 and 4)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

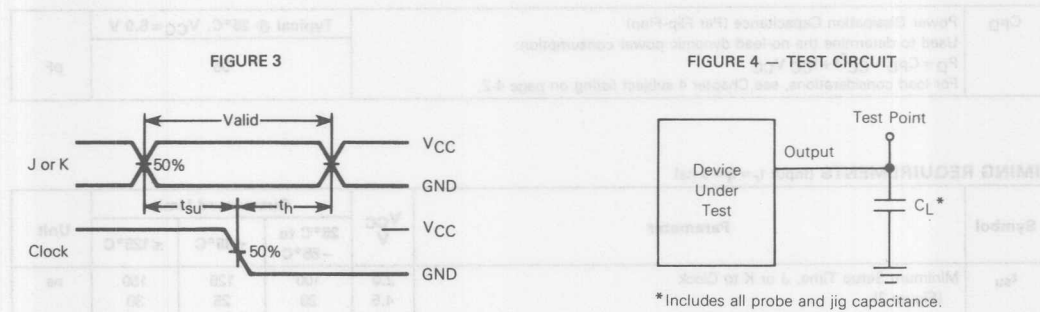
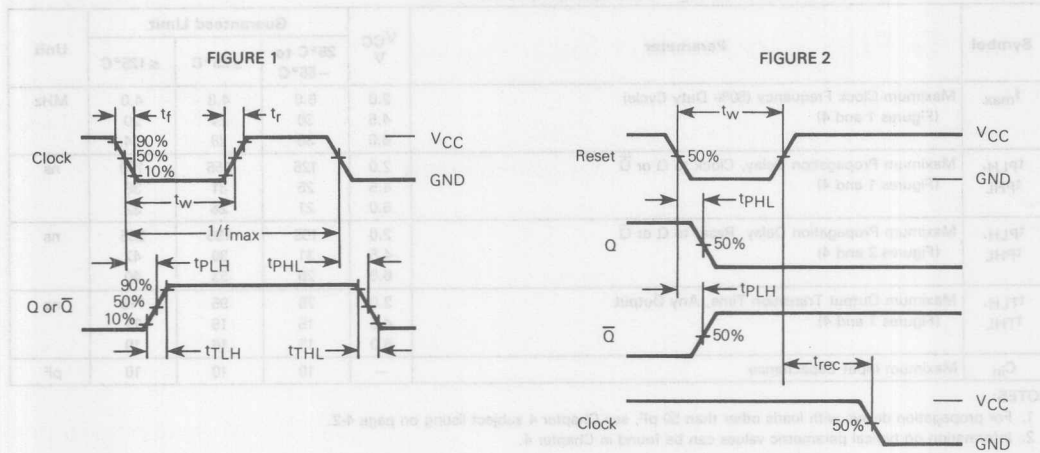
TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

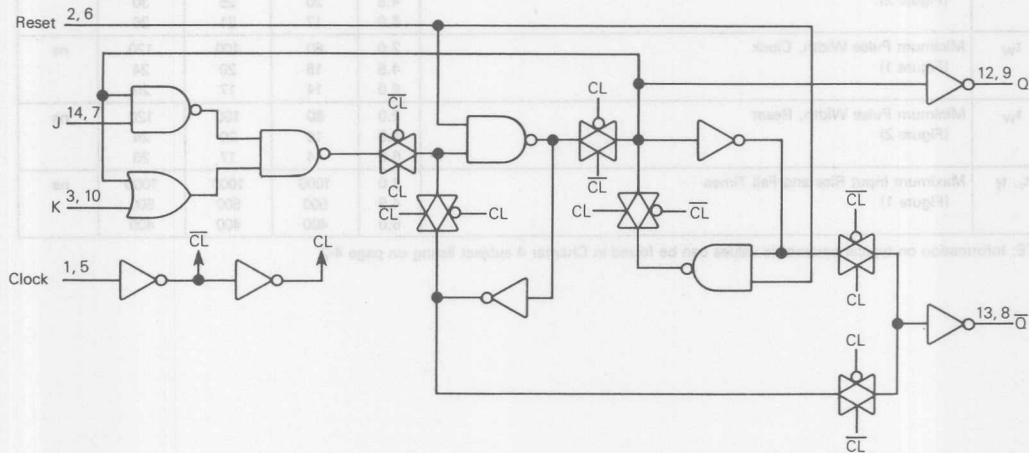
MC54/74HC73

SWITCHING WAVEFORMS



5

EXPANDED LOGIC DIAGRAM



Dual D Flip-Flop with Set and Reset

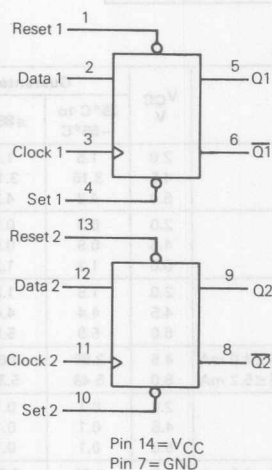
High-Performance Silicon-Gate CMOS

The MC54/74HC74 is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and \bar{Q} outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

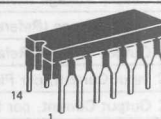
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 128 FETs or 32 Equivalent Gates

LOGIC DIAGRAM

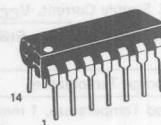


Pin 14 = VCC
Pin 7 = GND

MC54/74HC74



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

Reset 1	1	14	VCC
Data 1	2	13	Reset 2
Clock 1	3	12	Data 2
Set 1	4	11	Clock 2
Q1	5	10	Set 2
Q1-bar	6	9	Q2
GND	7	8	Q2-bar

FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	Q-bar
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	—	H	H	L
H	H	—	L	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H	X	X	No Change	No Change

* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

5

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125° C

Ceramic DIP: -10 mW/°C from 100° to 125° C

SOIC Package: -7 mW/°C from 65° to 125° C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0$ V 0 $V_{CC} = 4.5$ V 0 $V_{CC} = 6.0$ V 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	6.0	4	40	80	μ A

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC74

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set or Reset to Q or \bar{Q} (Figures 2 and 4)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} =5.0 V	pF
		39	

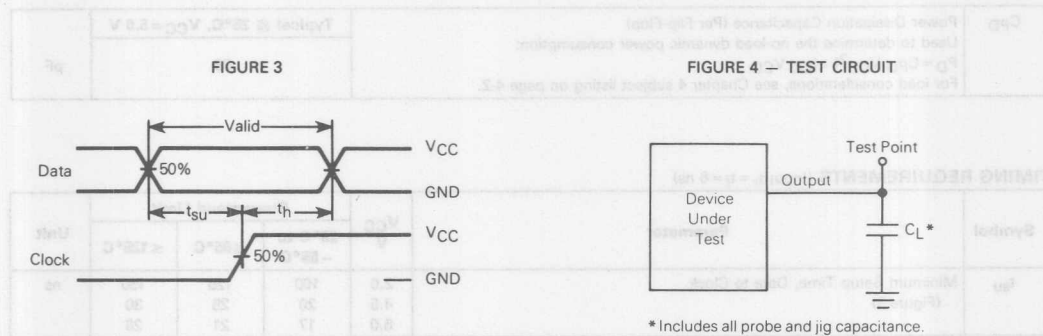
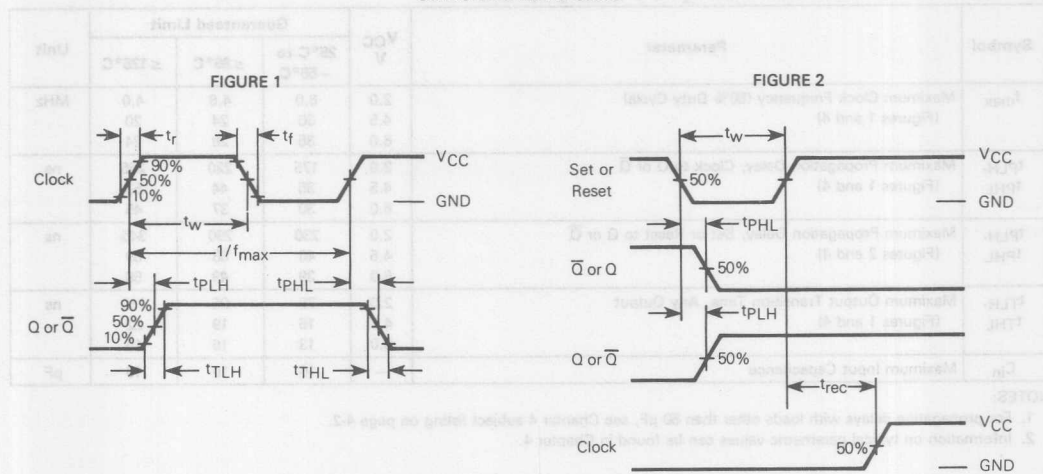
TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

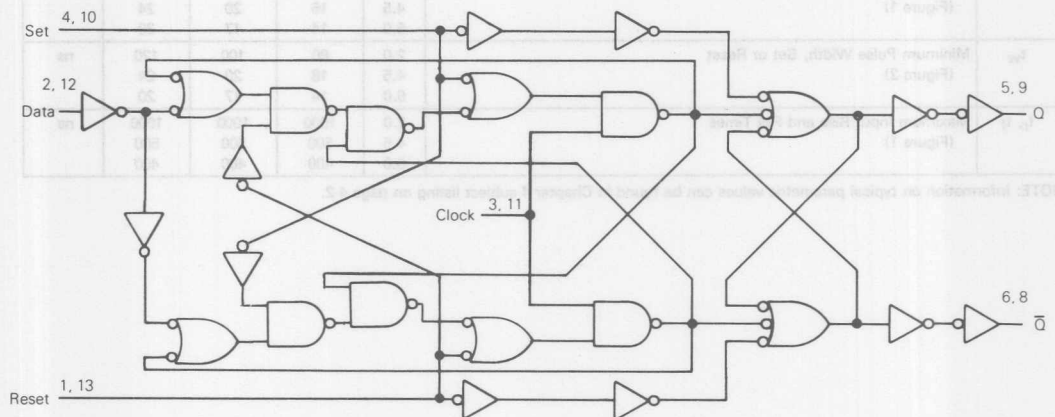
NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC74

SWITCHING WAVEFORMS



EXPANDED LOGIC DIAGRAM



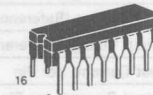
MC54/74HC75

Dual 2-Bit Transparent Latch High-Performance Silicon-Gate CMOS

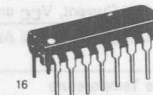
The MC54/74HC75 is identical in pinout to the LS75. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 2-bit transparent latches. Each latch stores the input data while Latch Enable is at a logic low. The outputs follow the data inputs when Latch Enable is at a logic high.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 80 FETs or 20 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



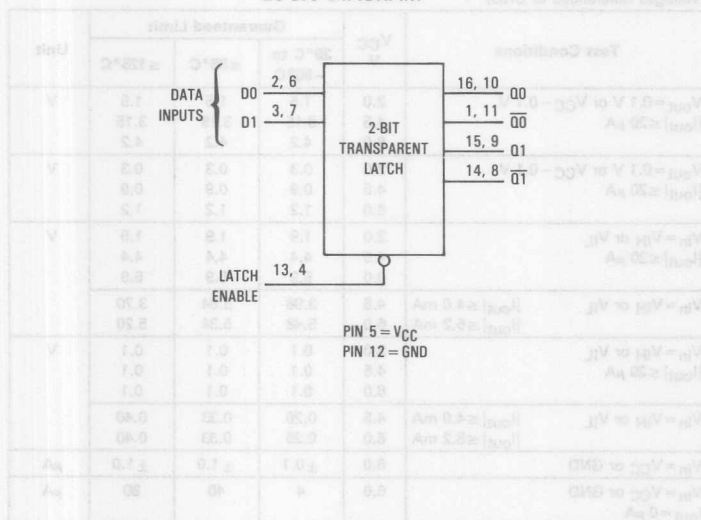
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

$\overline{Q0}_a$	1	16	$Q0_a$
$\overline{Q1}_a$	2	15	$Q1_a$
$\overline{Q1}_b$	3	14	$Q1_b$
\overline{LE}_b	4	13	LE_a
V_{CC}	5	12	GND
$\overline{Q0}_b$	6	11	$Q0_b$
$\overline{Q1}_b$	7	10	$Q0_b$
$\overline{Q1}_b$	8	9	$Q1_b$

FUNCTION TABLE

Inputs		Outputs	
D	Latch Enable	Q	\overline{Q}
L	H	L	H
H	H	H	L
X	L	Q0	$\overline{Q0}$

X = don't care
Q0 = latched data

		value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC75

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, D to Q (Figures 1 and 5)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, D to \bar{Q} (Figures 1 and 5)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to \bar{Q} (Figures 2 and 5)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, D to Latch Enable (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Enable to D (Figure 4)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t _w	Minimum Pulse Width, Latch Enable Input (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC75

SWITCHING WAVEFORMS

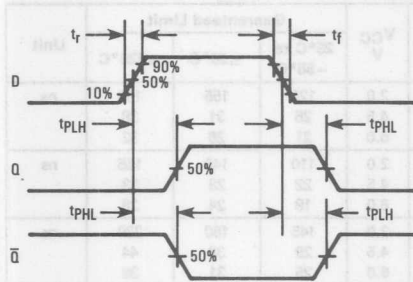


Figure 1

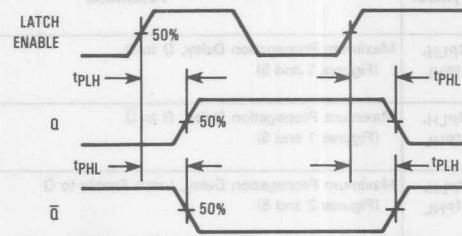


Figure 2

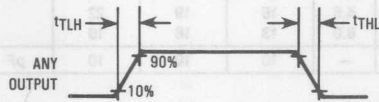


Figure 3

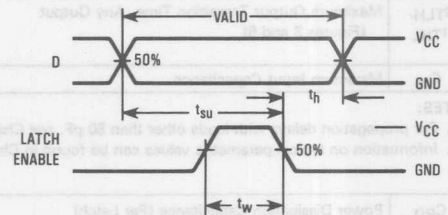
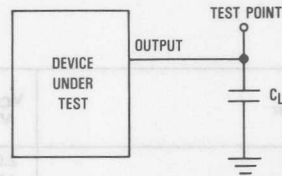


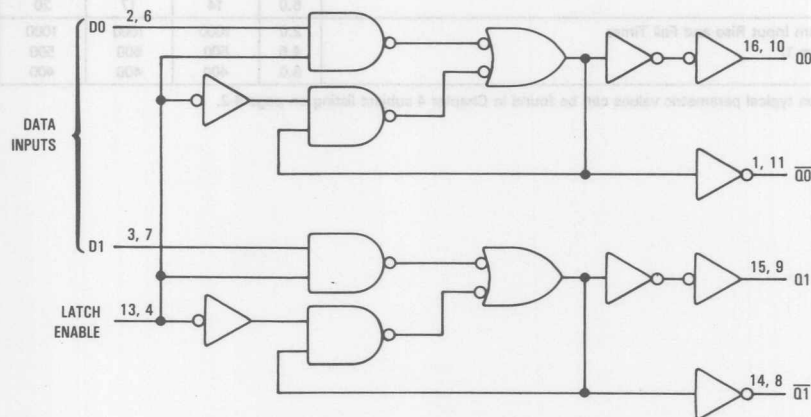
Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM



MC54/74HC76

Dual J-K Flip-Flop with Set and Reset

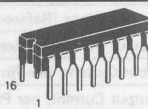
High-Performance Silicon-Gate CMOS

The MC54/74HC76 is identical in pinout to the LS76. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

The HC76 is identical in function to the HC112, but has a different pinout.

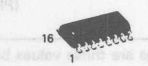
- Similar in Function to the LS76 Except When Set and Reset are Low Simultaneously
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 25 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



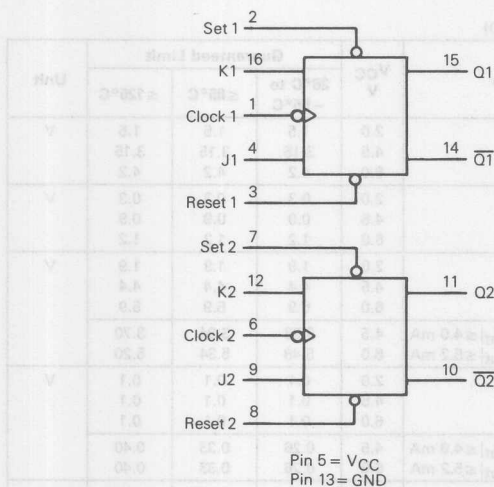
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Clock 1	1	16	K1
Set 1	2	15	Q1
Reset 1	3	14	Q1-bar
J1	4	13	GND
VCC	5	12	K2
Clock 2	6	11	Q2
Set 2	7	10	Q2-bar
Reset 2	8	9	J2

FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	Q-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	—	L	L	No Change	
H	H	—	L	H	L	H
H	H	—	H	L	H	L
H	H	—	H	H	Toggle	
H	H	L	X	X	No Change	
H	H	X	X	X	No Change	
H	H	—	X	X	No Change	

*Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC76

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Reset to Q or \bar{Q} (Figures 2 and 4)	2.0 4.5 6.0	155 31 26	195 39 33	235 47 40	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set to Q or \bar{Q} (Figures 2 and 4)	2.0 4.5 6.0	165 33 28	205 41 35	250 50 43	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

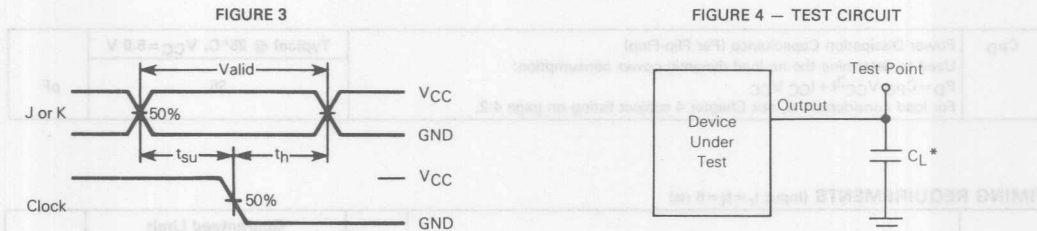
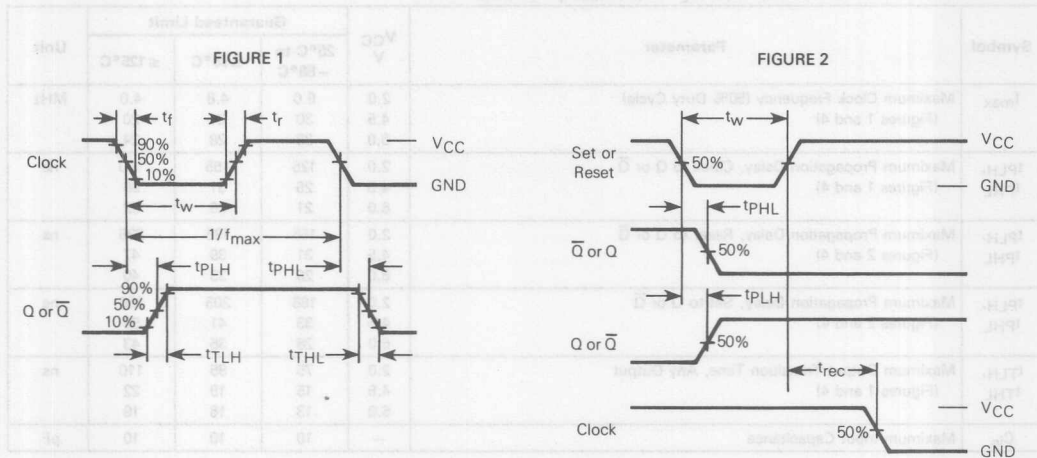
TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

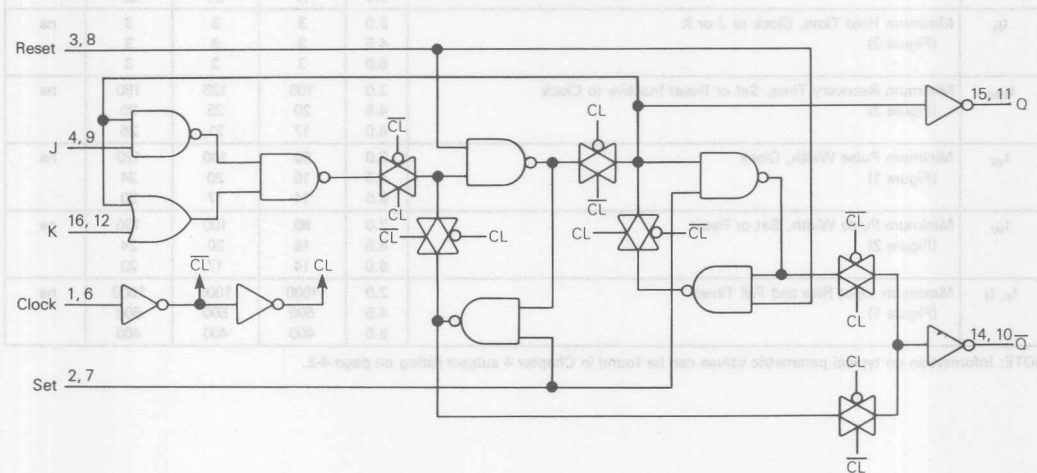
MC54/74HC76

SWITCHING WAVEFORMS



*Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM



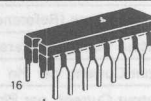
MC54/74HC85

4-Bit Magnitude Comparator High-Performance Silicon-Gate CMOS

The MC54/74HC85 is identical in pinout and function to the LS85. This device is similar in function to the MM74C85 and L85, but has a different pinout. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This 4-Bit Magnitude Comparator compares two 4-bit nibbles and gives a high voltage level on either the $A > B_{out}$, $A = B_{out}$, or $A < B_{out}$ output, leaving the other two at a low voltage level. This device also has $A > B_{in}$, $A = B_{in}$, and $A < B_{in}$ inputs, eliminating the need for external gates when cascading.

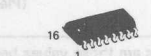
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 248 FETs or 62 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 620**



**N SUFFIX
PLASTIC
CASE 648**



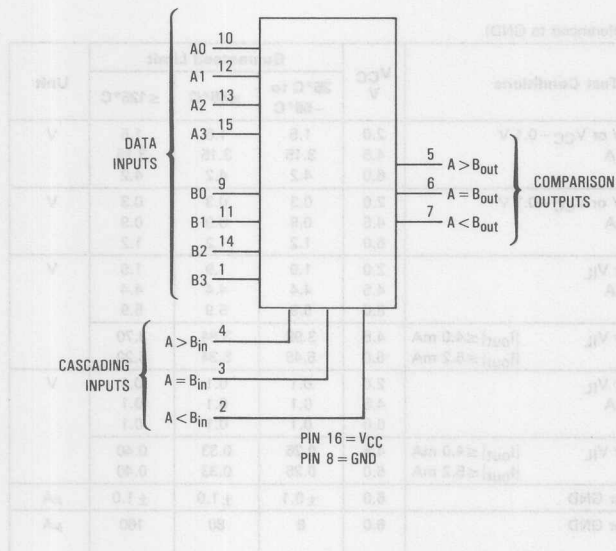
**D SUFFIX
SOIC
CASE 751**

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

B3	1	16	V _{CC}
A < B _{in}	2	15	A3
A = B _{in}	3	14	B2
A > B _{in}	4	13	A2
A > B _{out}	5	12	A1
A = B _{out}	6	11	B1
A < B _{out}	7	10	A0
GND	8	9	B0

5

V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C

Ceramic DIP: −10 mW/°C from 100° to 125°C

SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} =0.1 V or V _{CC} −0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} =0.1 V or V _{CC} −0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} =V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} =V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} =V _{CC} or GND I _{out} =0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC85

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Inputs A or B to Outputs A > B or A < B (Figures 1 and 2)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Inputs A or B to Output A = B (Figures 1 and 2)	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Inputs A < B or A = B to Output A > B (Figures 1 and 2)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Inputs A > B or A = B to Output A < B (Figures 1 and 2)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A = B to Output A = B (Figures 1 and 2)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		50	pF

FIGURE 1 — SWITCHING WAVEFORMS

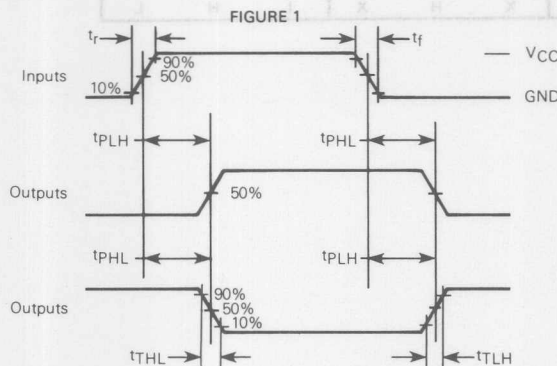
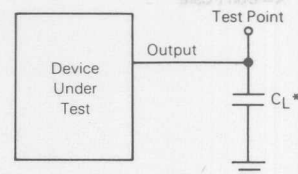


FIGURE 2 — TEST CIRCUIT



* Includes all probe and jig capacitance.

MC54/74HC85

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (Pins 10, 12, 13, 15) — Data Nibble A Inputs. The data nibble present at these inputs is compared to Data Nibble B. A3 is the most significant bit and A0 is the least significant bit.

B0, B1, B2, B3 (Pins 9, 11, 14, 1) — Data Nibble B Inputs. The data nibble present at these inputs is compared to Data Nibble A. B3 is the most significant bit and B0 is the least significant bit.

CONTROLS

A > B_{in}, A = B_{in}, A < B_{in} (Pins 4, 3, 2) — Cascading Inputs. These inputs determine the states of the outputs only when Data Nibble A equals Data Nibble B. The A = B_{in} input overrides both the A > B_{in} and A < B_{in} inputs.

For single stage operation or for the least significant stage in cascaded operation, the A < B_{in} and A > B_{in} inputs should be tied to ground and the A = B_{in} input tied to V_{CC}. Between cascaded comparators, the A < B_{out}, A = B_{out}, and A > B_{out}

outputs should be tied to A < B_{in}, A = B_{in}, and A > B_{in}, respectively, of the succeeding stage.

OUTPUTS

A > B_{out} (Pin 5) — A-Greater-Than-B Output. This output is at a high voltage level when Nibble A is greater than Nibble B, regardless of the data present at the cascading inputs. This output is also high when Nibble A equals Nibble B and the A > B_{in} input is high (A < B_{in} and A = B_{in} are at a low voltage level).

A = B_{out} (Pin 6) — A-Equals-B Output. This output is high when Nibble A equals Nibble B and the A = B_{in} input is high. A < B_{in} and A > B_{in} have no effect when the comparator is in this condition and A = B_{in} is at a high voltage level.

A < B_{out} (Pin 7) — A-Less-Than-B Output. This output is at a high voltage level when Nibble A is less than Nibble B, regardless of data present at the cascading inputs. This output is also high when Nibble A equals Nibble B and the A < B_{in} input is high (A > B_{in} and A = B_{in} are at a low voltage level).

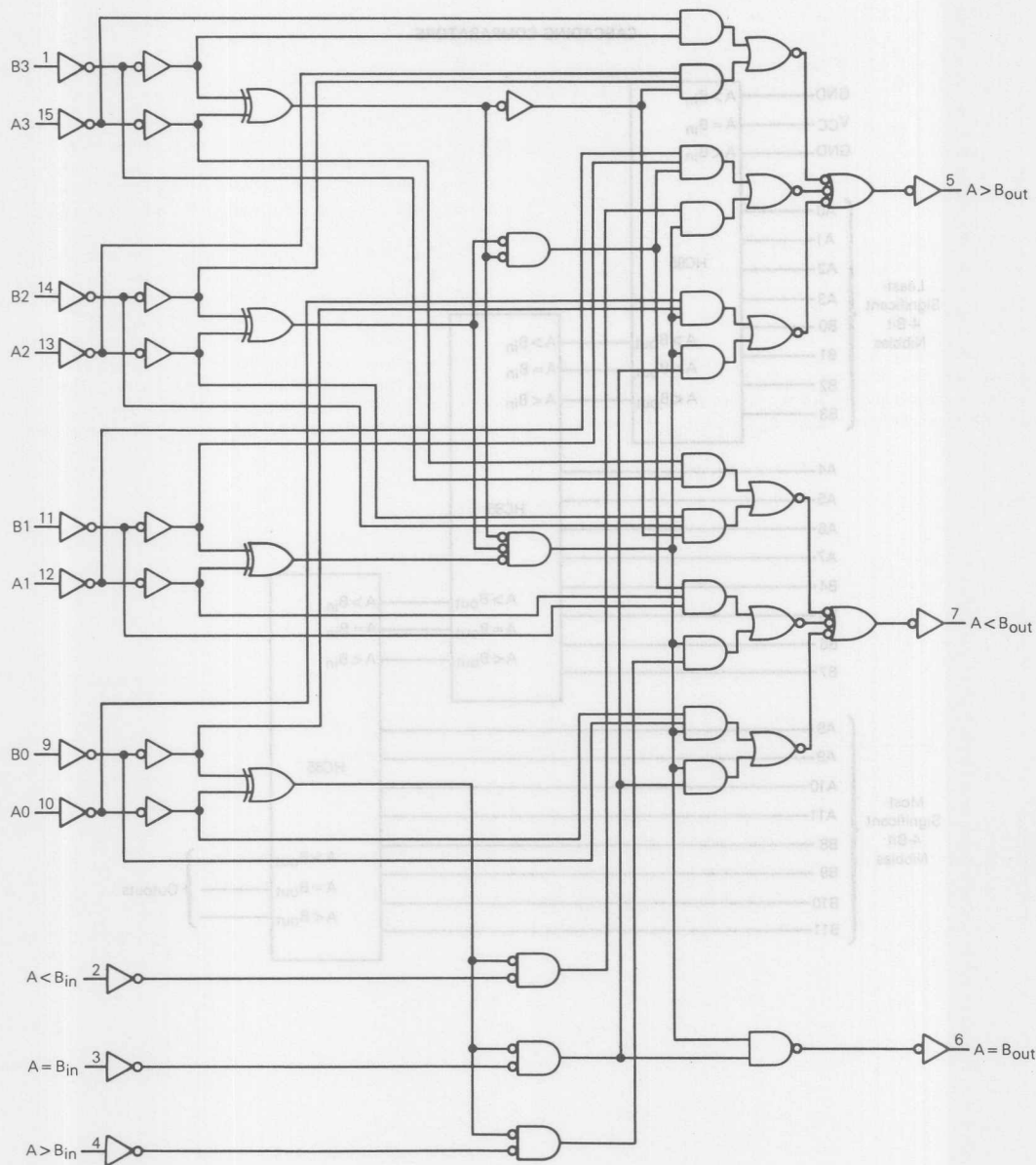
FUNCTION TABLE

Data Inputs				Cascading Inputs			Output		
A3, B3	A2, B2	A1, B1	A0, B0	A>B _{in}	A=B _{in}	A<B _{in}	A>B _{out}	A=B _{out}	A<B _{out}
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	L	H
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	L	H
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	L	H
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	L	H
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	H	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	X	H	X	L	H	L

X = Don't Care

MC54/74HC85

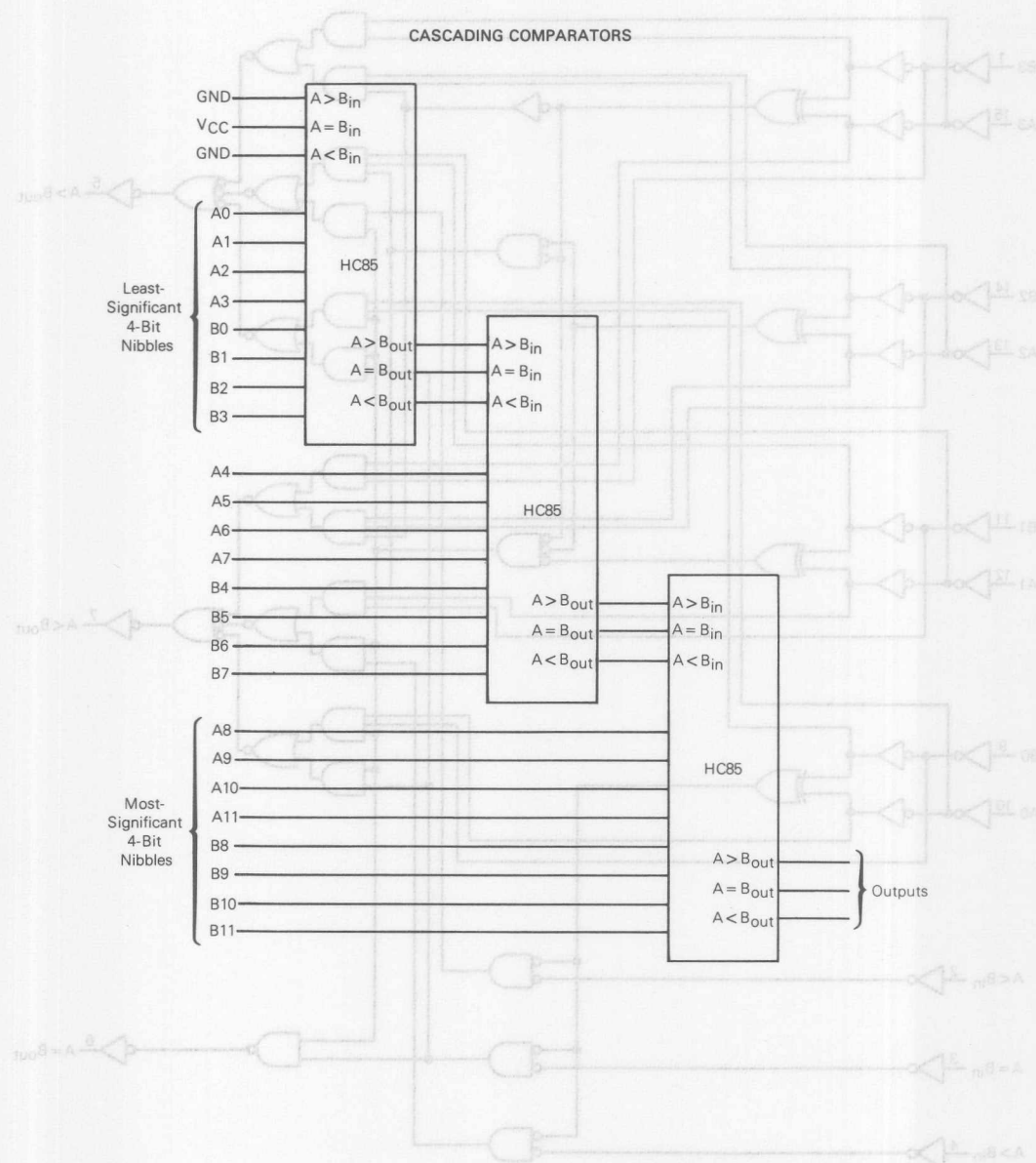
EXPANDED LOGIC DIAGRAM



5

MC54/74HC85

TYPICAL APPLICATION



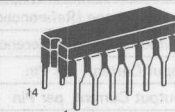
5

MC54/74HC86

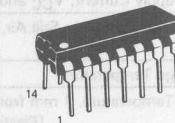
Quad 2-Input Exclusive OR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC86 is identical in pinout to the LS86; this device is similar in function to the MM74C86 and L86, but has a different pinout. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 632**



**N SUFFIX
PLASTIC
CASE 646**



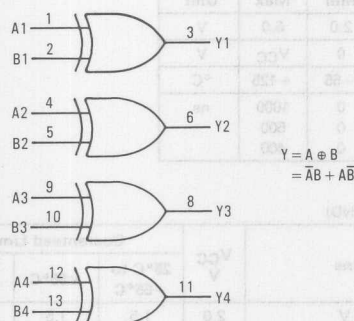
**D SUFFIX
SOIC
CASE 751A**

ORDERING INFORMATION

MC74HCXXN Plastic
MC54HCXXJ Ceramic
MC74HCXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

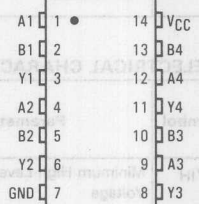
LOGIC DIAGRAM



$$Y = A \oplus B \\ = AB + \bar{A}\bar{B}$$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		33	

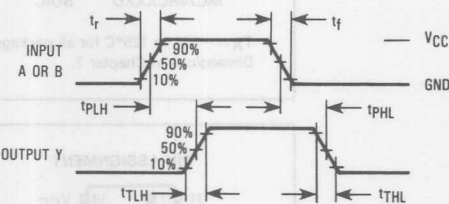
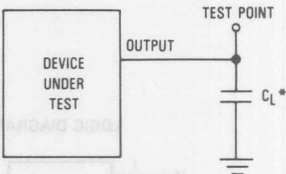


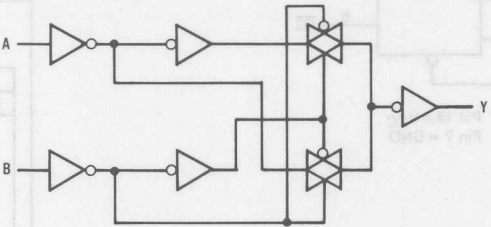
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(% of Device)



FUNCTION TABLE

Inputs	Output
A B	Y
L L	L
L H	L
H L	L
H H	L
L L	L
L H	L
H L	L
H H	L
L L	L
L H	L
H L	L
H H	L

MC54/74HC107

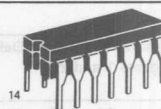
Dual J-K Flip-Flop with Reset High-Performance Silicon-Gate CMOS

The MC54/74HC107 is identical in pinout to the LS107. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

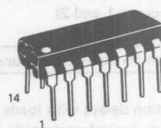
Each flip-flop is negative-edge clocked and has an active-low asynchronous reset.

The HC107 is identical in function to the HC73, but has a different pinout.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



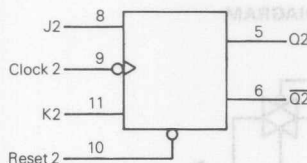
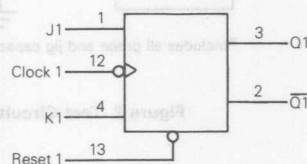
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



Pin 14 = V_{CC}
 Pin 7 = GND

PIN ASSIGNMENT

J1	1	14	V_{CC}
$\overline{Q1}$	2	13	Reset 1
Q1	3	12	Clock 1
K1	4	11	K2
Q2	5	10	Reset 2
$\overline{Q2}$	6	9	Clock 2
GND	7	8	J2

FUNCTION TABLE

Inputs				Outputs	
Reset	Clock	J	K	Q	\overline{Q}
L	X	X	X	L	H
H		L	L	No Change	H
H		L	H	L	H
H		H	L	H	L
H		H	H	Toggle	
H	L	X	X	No Change	
H	H	X	X	No Change	
H		X	X	No Change	

MC54/74HC107

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC107

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Reset to Q or \bar{Q} (Figures 2 and 4)	2.0 4.5 6.0	155 31 26	195 39 33	235 47 40	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC107

SWITCHING WAVEFORMS

FIGURE 1

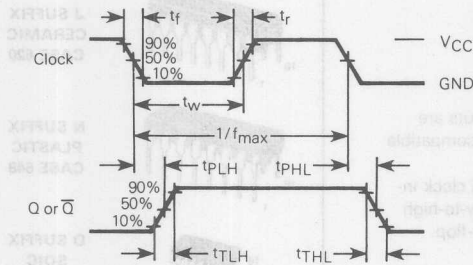


FIGURE 2

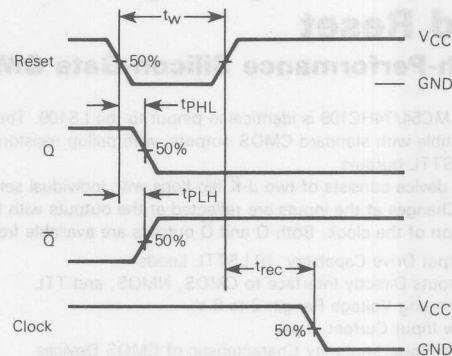


FIGURE 3

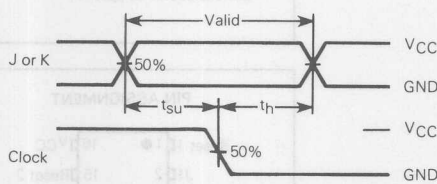
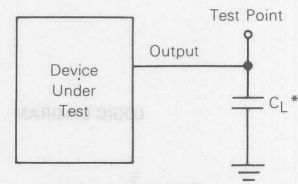
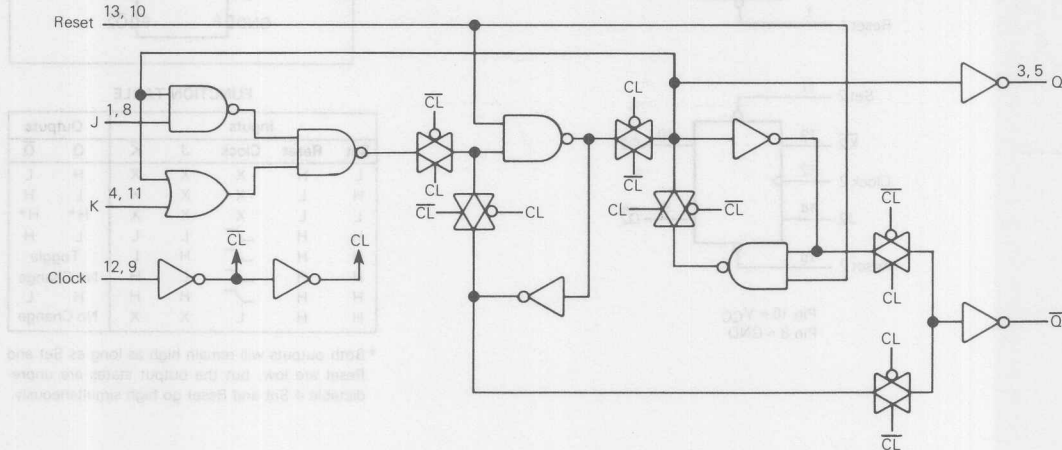


FIGURE 4 - TEST CIRCUIT



*Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM



Dual J- \bar{K} Flip-Flop with Set and Reset

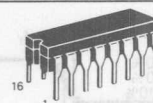
High-Performance Silicon-Gate CMOS

The MC54/74HC109 is identical in pinout to the LS109. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

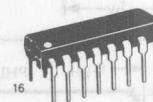
This device consists of two J- \bar{K} flip-flops with individual set, reset, and clock inputs. Changes at the inputs are reflected at the outputs with the next low-to-high transition of the clock. Both Q and \bar{Q} outputs are available from each flip-flop.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 148 FETs or 37 Equivalent Gates

MC54/74HC109



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



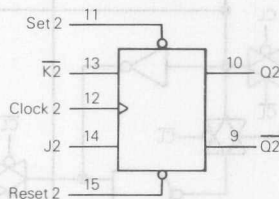
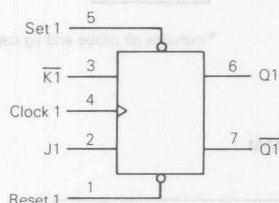
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

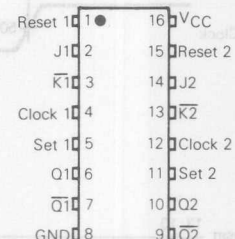
$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



Pin 16 = V_{CC}
Pin 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H		L	L	L	H
H	H		H	L	Toggle	
H	H		L	H	No Change	
H	H		H	H	No Change	
H	H	L	X	X	No Change	

* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MC54/74HC109

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	6.0	5.9	5.9	5.9	
			4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	6.0	0.1	0.1	0.1	
			4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC109

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set or Reset to Q or \bar{Q} (Figures 2 and 4)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, J or \bar{K} to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to J or \bar{K} (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

SWITCHING WAVEFORMS

FIGURE 1

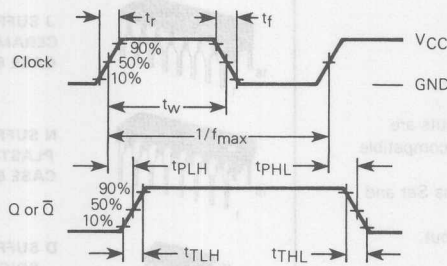


FIGURE 2

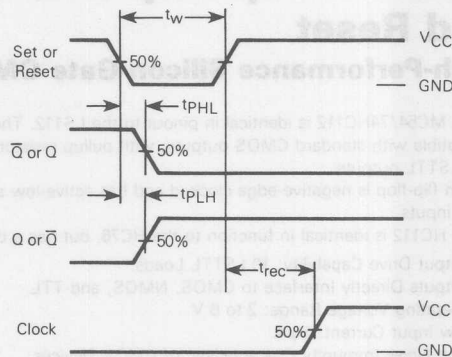


FIGURE 3

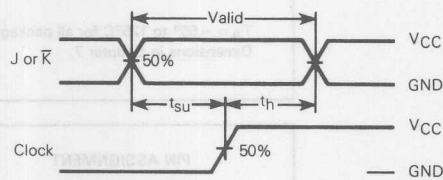
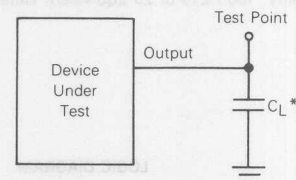
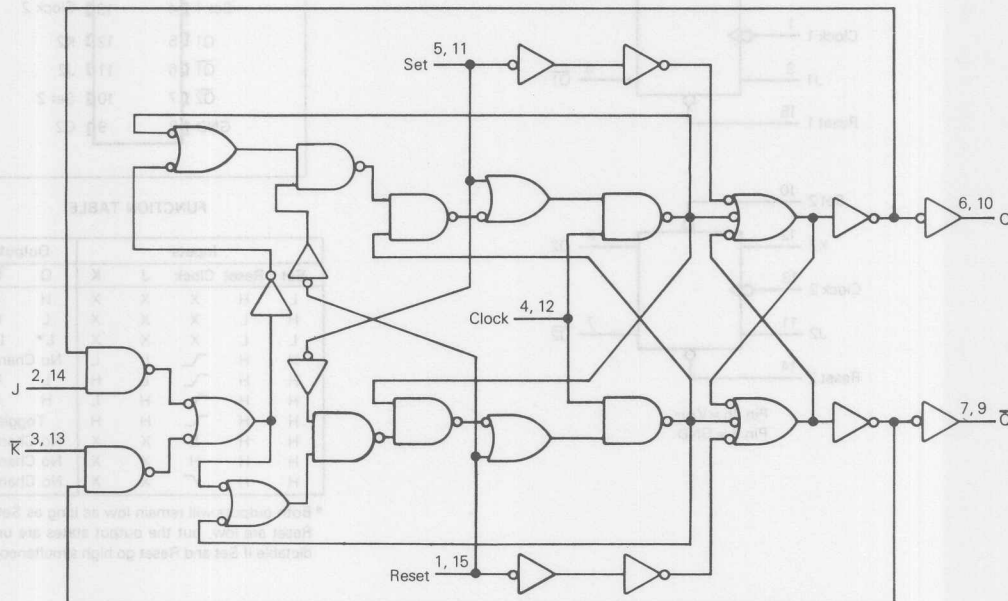


FIGURE 4 — TEST CIRCUIT



*Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM



Dual J-K Flip-Flop with Set and Reset

High-Performance Silicon-Gate CMOS

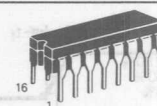
The MC54/74HC112 is identical in pinout to the LS112. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

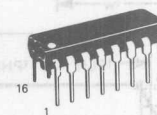
The HC112 is identical in function to the HC76, but has a different pinout.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Similar in Function to the LS112 Except When Set and Reset are Low Simultaneously
- Chip Complexity: 100 FETs or 25 Equivalent Gates

MC54/74HC112



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



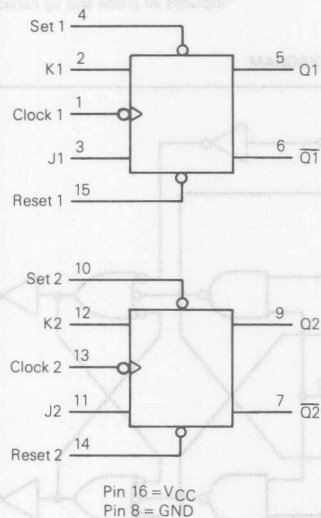
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Clock 1	1	16	VCC
K1	2	15	Reset 1
J1	3	14	Reset 2
Set 1	4	13	Clock 2
Q1	5	12	K2
Q1-bar	6	11	J2
Q2	7	10	Set 2
GND	8	9	Q2

FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	Q-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	~	L	L	No Change	
H	H	~	L	H	L	H
H	H	~	H	L	H	L
H	H	~	H	H	Toggle	
H	H	L	X	X	No Change	
H	H	X	X	X	No Change	
H	H	~	X	X	No Change	

*Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MC54/74HC112

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC112

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Reset to Q or \bar{Q} (Figures 2 and 4)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set to Q or \bar{Q} (Figures 2 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

SWITCHING WAVEFORMS

FIGURE 1

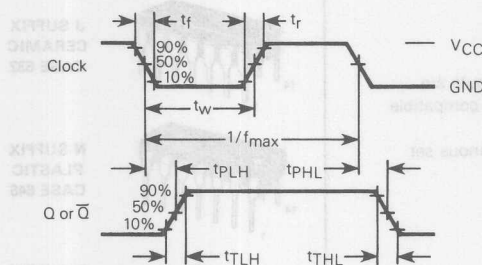


FIGURE 2

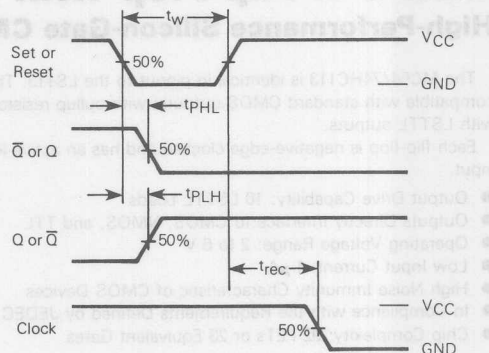


FIGURE 3

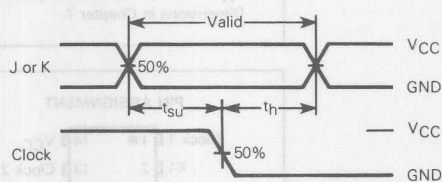
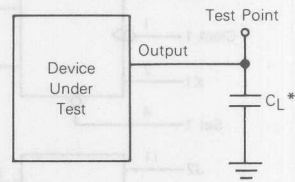
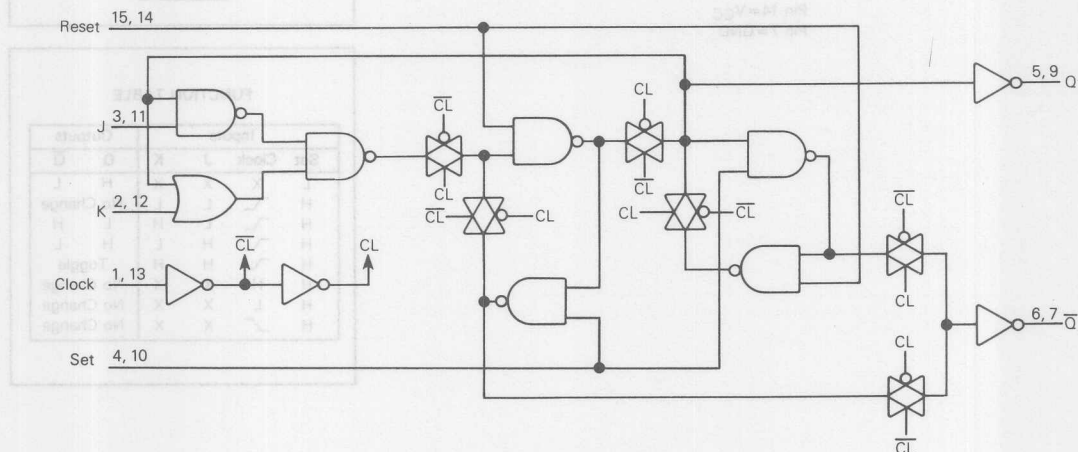


FIGURE 4 — TEST CIRCUIT



*Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM



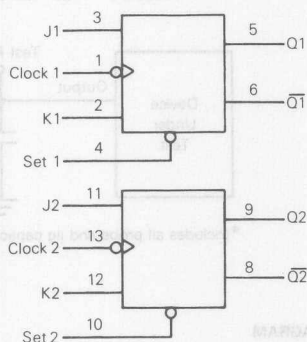
Dual J-K Flip-Flop with Set High-Performance Silicon-Gate CMOS

The MC54/74HC113 is identical in pinout to the LS113. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has an active-low asynchronous set input.

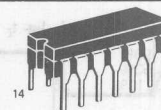
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates

LOGIC DIAGRAM

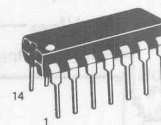


Pin 14 = V_{CC}
Pin 7 = GND

MC54/74HC113



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



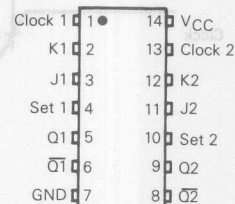
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN Plastic
MC54HCXXJ Ceramic
MC74HCXXD SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
Set	Clock	J	K	Q	Q̄
L	X	X	X	H	L
H	⌊	L	L	No Change	
H	⌊	L	H	L	H
H	⌊	H	L	H	L
H	⌊	H	H	Toggle	
H	H	X	X	No Change	
H	L	X	X	No Change	
H	⌊	X	X	No Change	

MC54/74HC113

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu A$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu A$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC113

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set to Q or \bar{Q} (Figures 2 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	
		35	pF

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, J or K to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to J or K (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _{rec}	Minimum Recovery Time, Set Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Set (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

SWITCHING WAVEFORMS

FIGURE 1

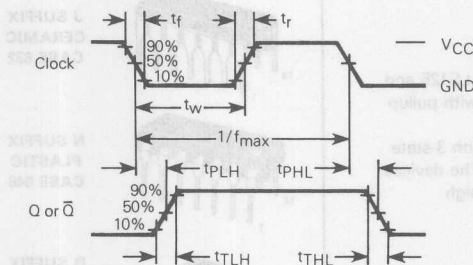


FIGURE 2

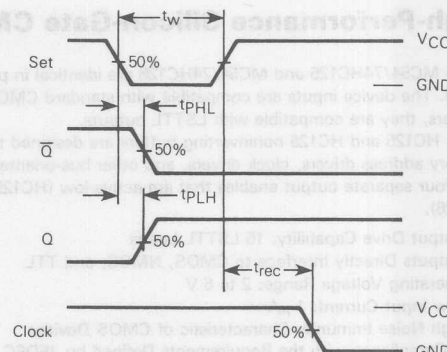


FIGURE 3

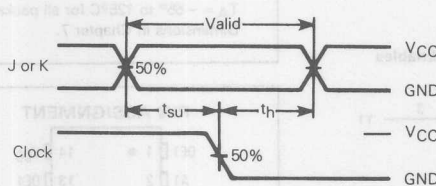
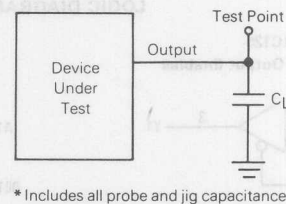
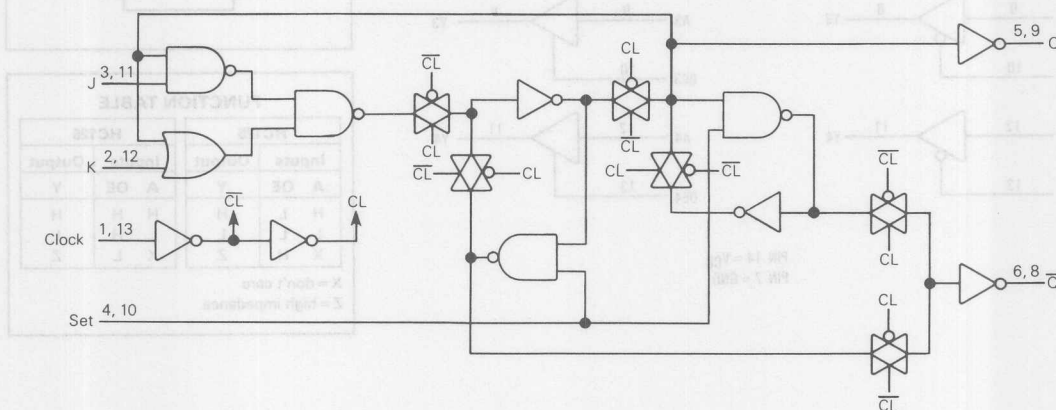


FIGURE 4 — TEST CIRCUIT



* Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM



Quad 3-State Noninverting Buffers

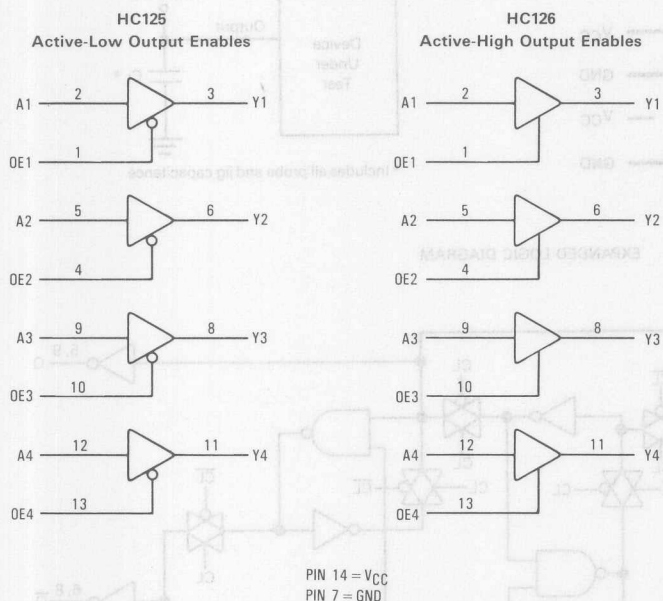
High-Performance Silicon-Gate CMOS

The MC54/74HC125 and MC54/74HC126 are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

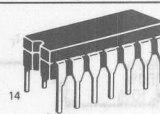
The HC125 and HC126 noninverting buffers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low (HC125) or active-high (HC126).

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

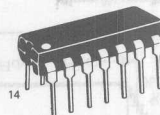
LOGIC DIAGRAM



MC54/74HC125 MC54/74HC126



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

OE1	1	14	V_{CC}
A1	2	13	OE4
Y1	3	12	A4
OE2	4	11	Y4
A2	5	10	OE3
Y2	6	9	A3
GND	7	8	Y3

FUNCTION TABLE

HC125			HC126		
Inputs		Output	Inputs		Output
A	OE	Y	A	OE	Y
H	L	H	H	H	H
L	L	L	L	H	L
X	H	Z	X	L	Z

X = don't care
Z = high impedance

MC54/74HC125•MC54/74HC126

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400 ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC125•MC54/74HC126

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		45	

SWITCHING WAVEFORMS

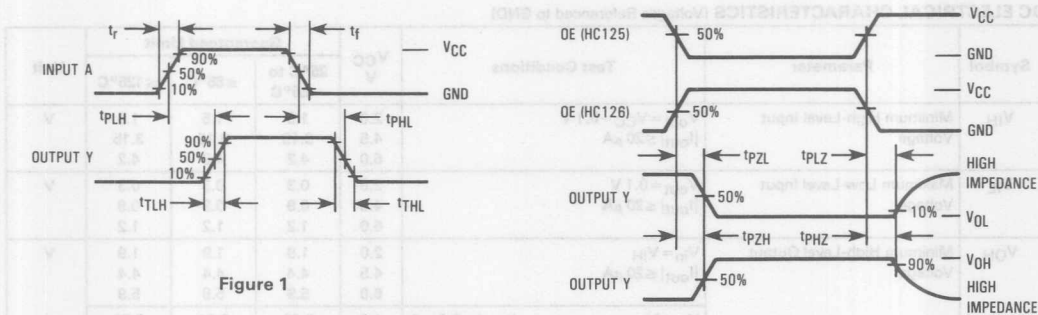
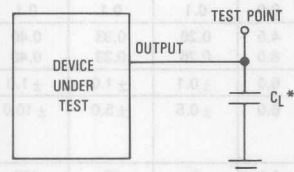


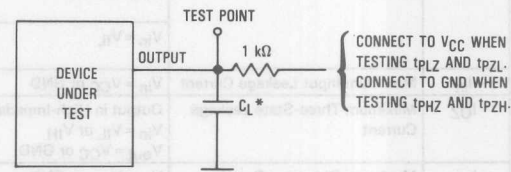
Figure 1

Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit

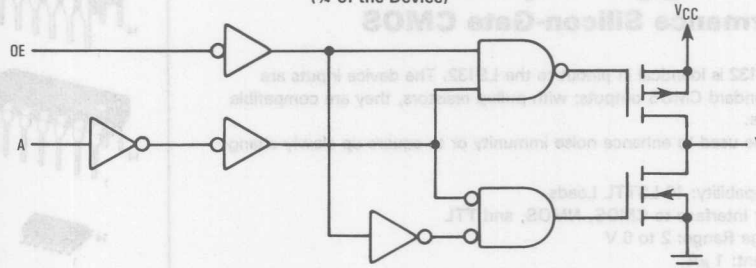


*Includes all probe and jig capacitance.

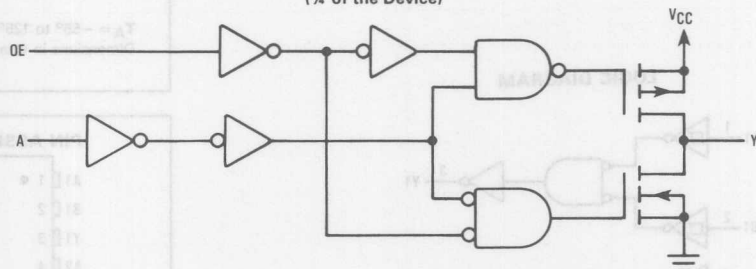
Figure 4. Test Circuit

LOGIC DETAILS

HC125
(% of the Device)



HC126
(% of the Device)



MC54/74HC125

1 SURF
DIP16

1 SURF
PLASTIC
DIP16

0 SURF
SOIC
DIP16

ORDERING INFORMATION

MC54HC125 Plastic
MC54HC125 Ceramic
MC54HC125 SOIC

TA = -55 to 125°C for all packages
X = 100% test at 125°C

FUNCTION TABLE

Input	Output
A	B
L	L
L	H
H	L
H	H

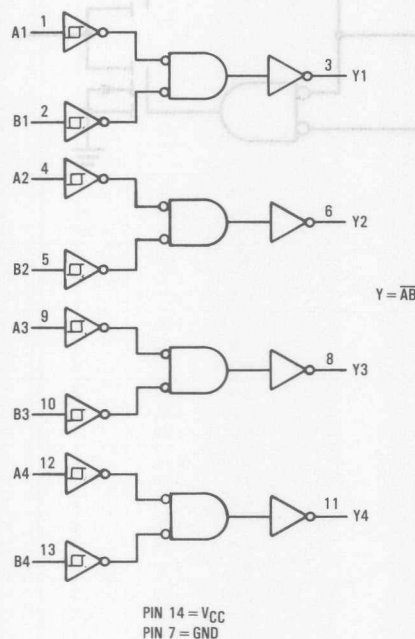
Quad 2-Input NAND Gate with Schmitt-Trigger Inputs High-Performance Silicon-Gate CMOS

The MC54/74HC132 is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

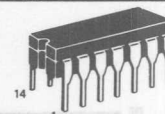
The HC132 can be used to enhance noise immunity or to square up slowly changing waveforms.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

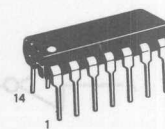
LOGIC DIAGRAM



MC54/74HC132



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	B4
Y1	3	12	A4
A2	4	11	Y4
B2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MC54/74HC132

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	no limit*	ns

*When $V_{in} \sim 0.5 V_{CC}$, $I_{CC} > \text{quiescent current}$.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C	-40°C to +85°C	-55°C to +125°C	
V_{T+max}	Maximum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V_{T+min}	Minimum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.00 2.30 3.00	0.95 2.25 2.95	0.95 2.25 2.95	V
V_{T-max}	Maximum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.90 2.00 2.60	0.95 2.05 2.65	0.95 2.05 2.65	V
V_{T-min}	Minimum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.30 0.90 1.20	0.30 0.90 1.20	0.30 0.90 1.20	V
V_{Hmax} Note 2	Maximum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.20 2.25 3.00	1.20 2.25 3.00	1.20 2.25 3.00	V
V_{Hmin} Note 2	Minimum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.20 0.40 0.50	0.20 0.40 0.50	0.20 0.40 0.50	V

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- $V_{Hmin} > (V_{T+min}) - (V_{T-max})$; $V_{Hmax} = (V_{T+max}) + (V_{T-min})$.

MC54/74HC132

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V _{OH}	Minimum High-Level Output Voltage	V _{in} ≤ V _{T- min} or V _{T+ max} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} ≤ V _{T- min} or V _{T+ max} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} ≥ V _{T+ max} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} ≥ V _{T+ max} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		24	

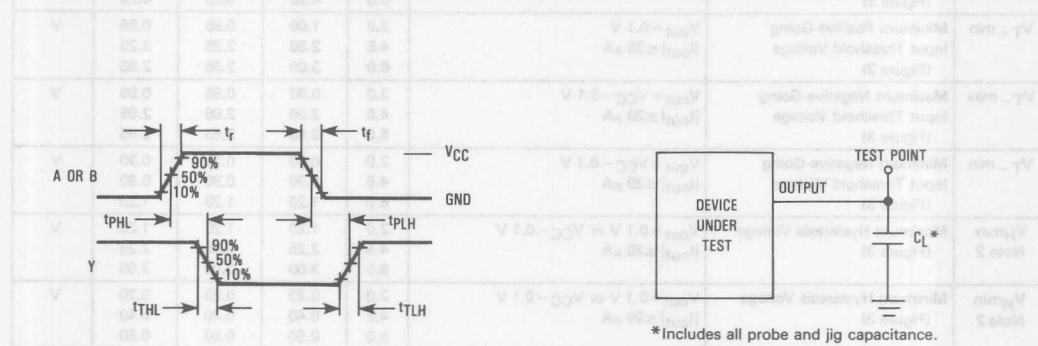


Figure 1. Switching Waveforms

Figure 2. Test Circuit

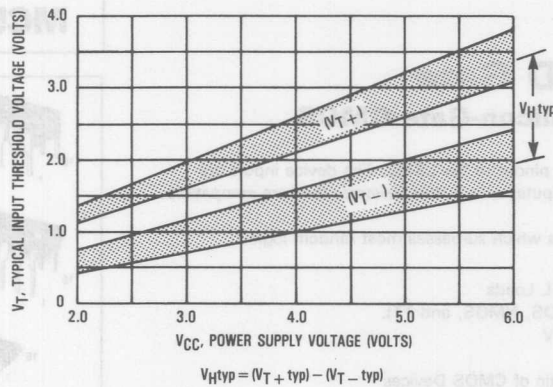


Figure 3. Typical Input Threshold, V_{T+} , V_{T-} , Versus Power Supply Voltage

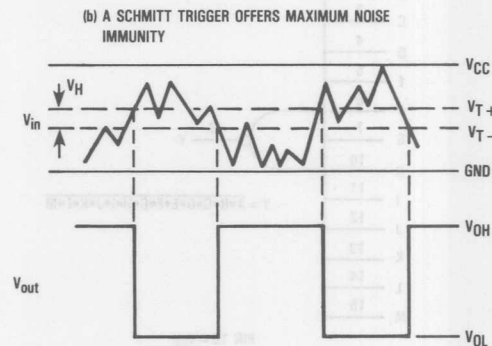
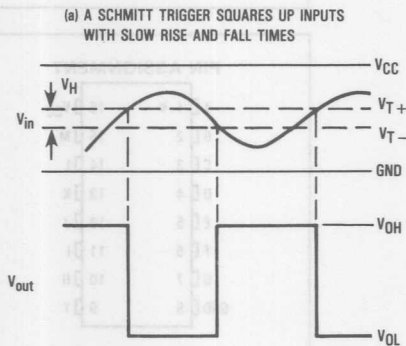
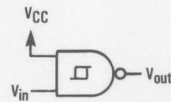


Figure 4. Typical Schmitt-Trigger Applications

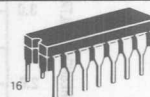
MC54/74HC133

13-Input NAND Gate High-Performance Silicon-Gate CMOS

The MC54/74HC133 is identical in pinout to the LS133. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This NAND gate features 13 inputs which surpasses most random logic requirements.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 68 FETs or 17 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



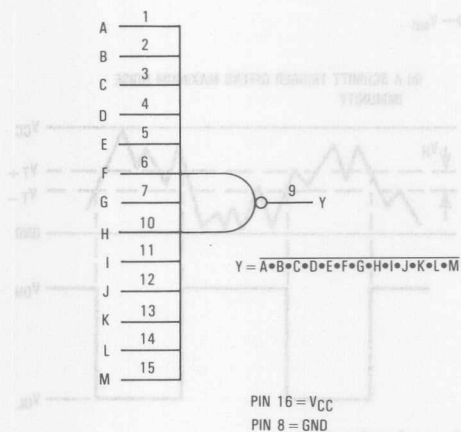
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

A	1	16	V_{CC}
B	2	15	M
C	3	14	L
D	4	13	K
E	5	12	J
F	6	11	I
G	7	10	H
GND	8	9	Y

FUNCTION TABLE

Inputs A through M	Output Y
All inputs H	L
All other combinations	H

MC54/74HC133

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC}+1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC}+0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC}=2.0\text{ V}$ $V_{CC}=4.5\text{ V}$ $V_{CC}=6.0\text{ V}$	0 0 0	1000 500 400 ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out}=0.1\text{ V}$ or $V_{CC}-0.1\text{ V}$ $ I_{out} \leq 20\text{ }\mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out}=0.1\text{ V}$ or $V_{CC}-0.1\text{ V}$ $ I_{out} \leq 20\text{ }\mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 20\text{ }\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 4.0\text{ mA}$ $ I_{out} \leq 5.2\text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 20\text{ }\mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 4.0\text{ mA}$ $ I_{out} \leq 5.2\text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in}=V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in}=V_{CC}$ or GND $I_{out}=0\text{ }\mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC133

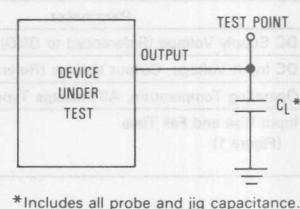
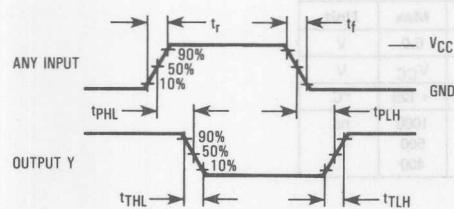
AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		27	

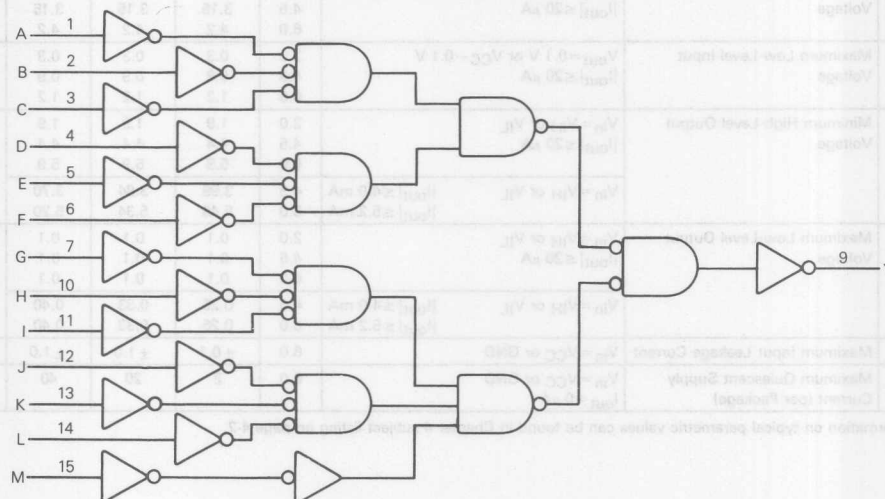


*Includes all probe and jig capacitance.

Figure 1. Switching Waveforms

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM



1-of-8 Decoder/Demultiplexer with Address Latch

High-Performance Silicon-Gate CMOS

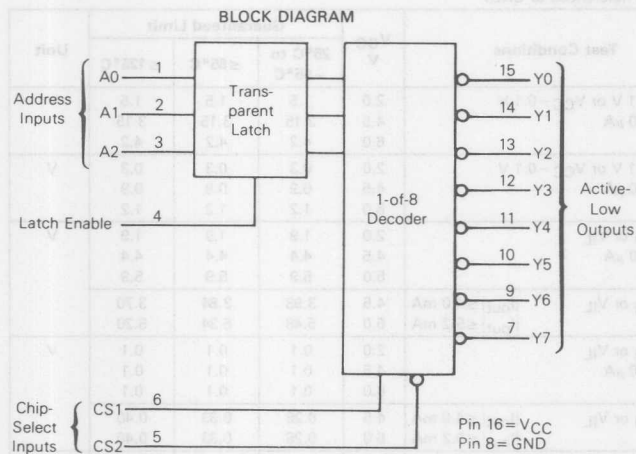
The MC54/74HC137 is identical in pinout to the LS137. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC137 decodes a three-bit Address to one-of-eight active-low outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

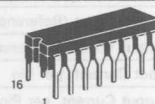
The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC137 is the inverting version of the HC237.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 152 FETs or 38 Equivalent Gates



MC54/74HC137



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

A0	1	16	VCC
A1	2	15	Y0
A2	3	14	Y1
Latch Enable	4	13	Y2
CS2	5	12	Y3
CS1	6	11	Y4
Y7	7	10	Y5
GND	8	9	Y6

FUNCTION TABLE

Inputs				Outputs							
LE	CS1	CS2	A2 A1 A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X X X	H	H	H	H	H	H	H	H
X	L	X	X X X	H	H	H	H	H	H	H	H
L	H	L	L L L	L	L	H	H	H	H	H	H
L	H	L	L L H	H	L	H	H	H	H	H	H
L	H	L	L H L	H	H	L	H	H	H	H	H
L	H	L	L H H	H	H	H	L	H	H	H	H
L	H	L	H L L	H	H	H	H	L	H	H	H
L	H	L	H L H	H	H	H	H	H	L	H	H
L	H	L	H H L	H	H	H	H	H	H	L	H
L	H	L	H H H	H	H	H	H	H	H	H	L
H	H	L	X X X	*	*	*	*	*	*	*	*

* = Depends upon the Address previously applied while LE was at a low level.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 2)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC137

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 6)	2.0	170	215	255	ns
		4.5	34	43	51	
		6.0	29	37	43	
t _{PHL}		2.0	240	300	360	
		4.5	48	60	72	
		6.0	41	51	61	
t _{PLH}	Maximum Propagation Delay, CS1 or CS2 to Output Y (Figures 2, 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PHL}		2.0	195	245	295	
		4.5	39	49	59	
		6.0	33	42	50	
t _{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 4 and 6)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PHL}		2.0	250	315	375	
		4.5	50	63	75	
		6.0	43	54	64	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	pF
		100	

TIMING REQUIREMENTS (Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input A to Latch Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Enable to Input A (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _w	Minimum Pulse Width, Latch Enable (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 2)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

ADDRESS INPUTS

A0, A1, A2 (PINS 1, 2, 3) — Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

CONTROL INPUTS

CS1, CS2 (PINS 6, 5) — Chip-Select inputs. For CS1 at a high level and CS2 at a low level, the chip is enabled and the outputs follow the address inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs are at a high level.

LATCH ENABLE (PIN 4) — Latch-Enable input. A high level at this input latches the Address. A low level at this input allows the outputs to follow the data at the Address pins (CS1 = H and CS2 = L).

OUTPUTS

Y0-Y7 — Active-low outputs. One of these eight outputs is selected when the chip is enabled (CS1 = H and CS2 = L) and the data on the A0, A1, and A2 inputs correspond to that particular output. The selected output is at a low level while all others remain at a high level.

SWITCHING WAVEFORMS

FIGURE 1

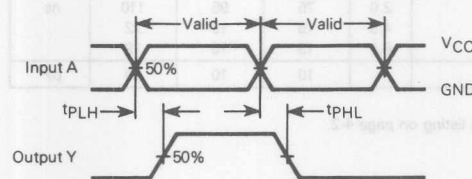


FIGURE 2

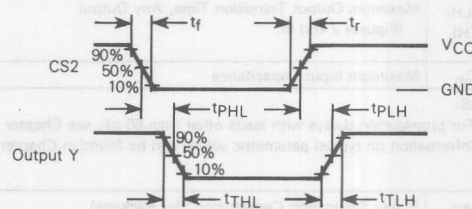


FIGURE 3

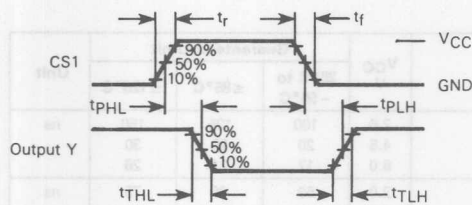


FIGURE 4

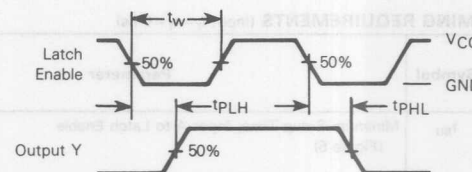


FIGURE 5

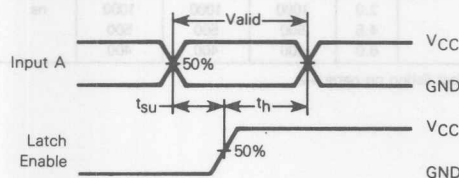
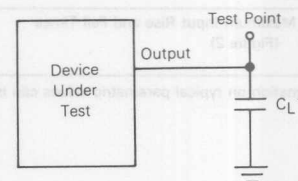


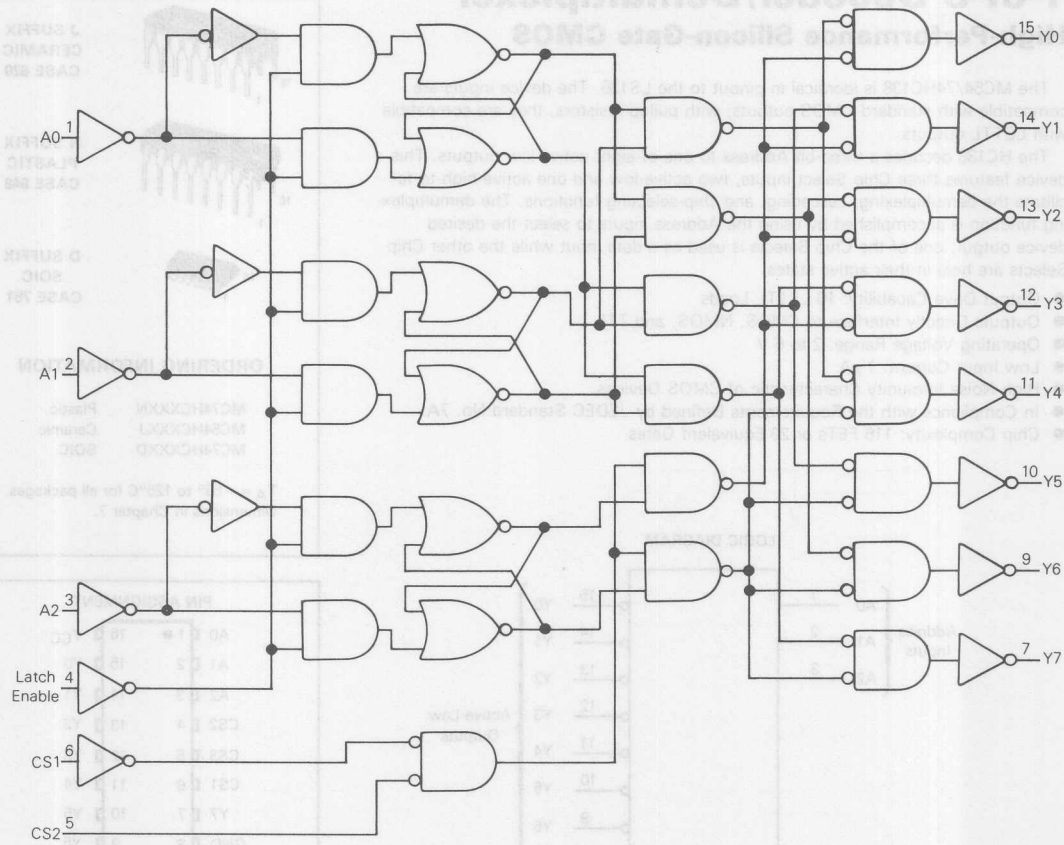
FIGURE 6 — TEST CIRCUIT



*Includes all probe and jig capacitance.

MC54/74HC137

EXPANDED LOGIC DIAGRAM



FUNCTION TABLE

Inputs	Outputs
A2 A1 A0	Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
L L L	H H H H H H H H
L L H	L H H H H H H H
L H L	L L H H H H H H
L H H	L L L H H H H H
H L L	L L L L H H H H
H L H	L L L L L H H H
H H L	L L L L L L H H
H H H	L L L L L L L H

H = high level (steady state)
L = low level (steady state)
X = don't care

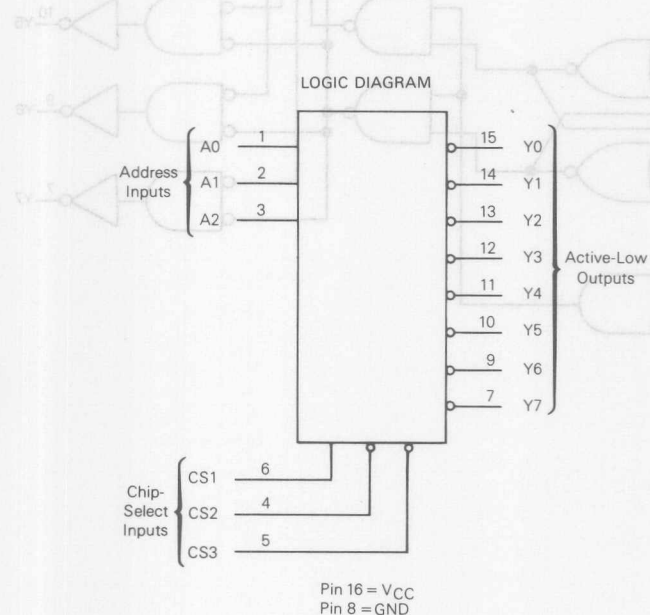
1-of-8 Decoder/Demultiplexer

High-Performance Silicon-Gate CMOS

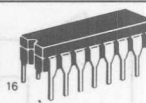
The MC54/74HC138 is identical in pinout to the LS138. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC138 decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

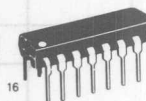
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 116 FETs or 29 Equivalent Gates



MC54/74HC138



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

A0	1	16	V _{CC}
A1	2	15	Y0
A2	3	14	Y1
CS2	4	13	Y2
CS3	5	12	Y3
CS1	6	11	Y4
Y7	7	10	Y5
GND	8	9	Y6

FUNCTION TABLE

Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	F	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	L	H	L	L	H	H	H	L	H	H	H
H	L	L	L	H	L	H	H	H	H	H	L	H	H
H	L	L	L	H	H	L	H	H	H	H	H	L	H
H	L	L	L	H	H	H	H	H	H	H	H	H	L

H = high level (steady state)
L = low level (steady state)
X = don't care

MC54/74HC138

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} ,V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 2)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC138

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PHL}		2.0	200	250	300	
		4.5	40	50	60	
		6.0	34	43	51	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, CS1 to Output Y (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PLH}	Maximum Propagation Delay, CS2 or CS3 to Output Y (Figures 3 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PHL}		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		55	

SWITCHING WAVEFORMS

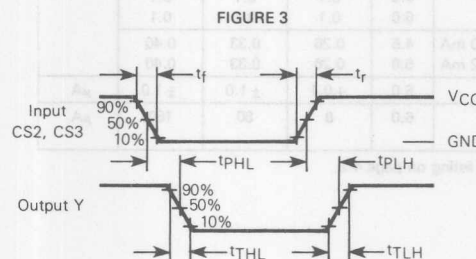
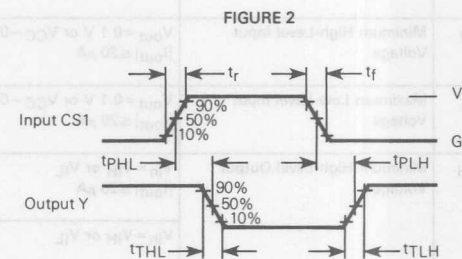
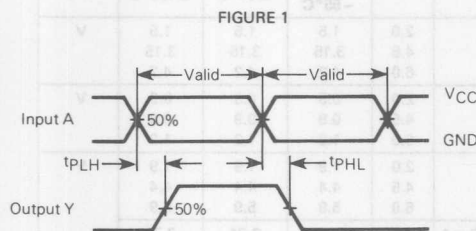
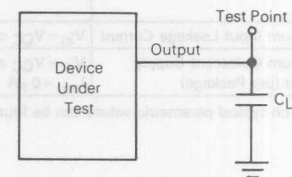


FIGURE 4 — TEST CIRCUIT



* Includes all probe and jig capacitance.

MC54/74HC138

PIN DESCRIPTIONS

ADDRESS INPUTS

A0, A1, A2 (PINS 1, 2, 3) — Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active-low.

CONTROL INPUTS

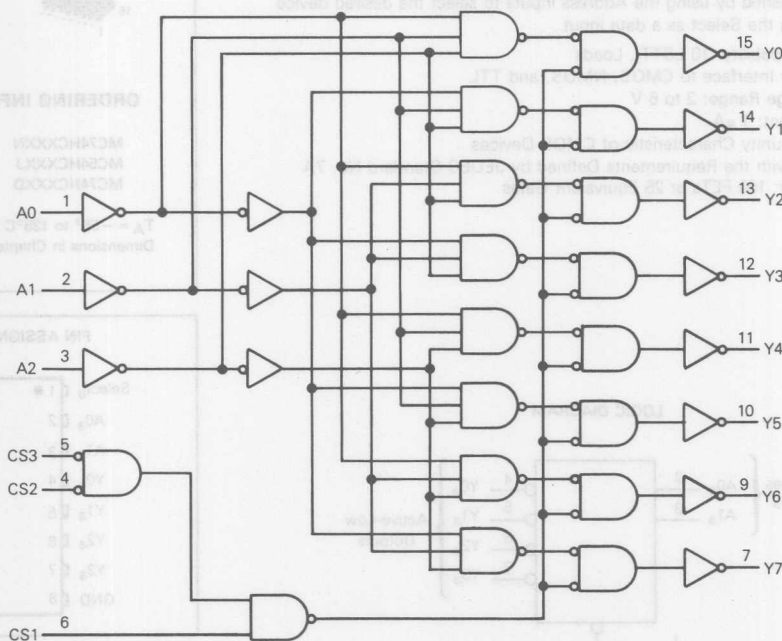
CS1, CS2, CS3 (PINS 6, 4, 5) — Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the

outputs follow the Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic high.

OUTPUTS

Y0-Y7 (PINS 15, 14, 13, 12, 11, 10, 9, 7) — Active-low Decoded outputs. These outputs assume a low level when addressed and the chip is selected. These outputs remain high when not addressed or the chip is not selected.

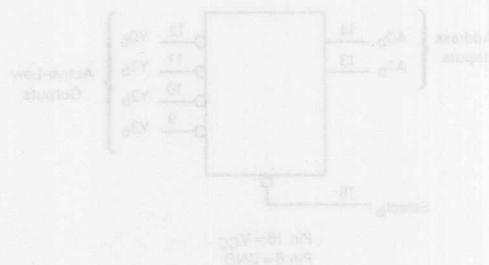
EXPANDED LOGIC DIAGRAM



FUNCTION TABLE

Outputs	A2	A1	A0
Y0	H	X	X
Y1	H	L	X
Y2	H	X	L
Y3	H	L	L
Y4	L	X	X
Y5	L	L	X
Y6	L	X	L
Y7	L	L	L

X = Don't care



Dual 1-of-4 Decoder/ Demultiplexer

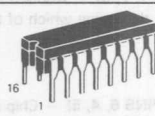
High-Performance Silicon-Gate CMOS

The MC54/74HC139 is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

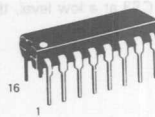
This device consists of two independent 1-of-4 decoders, each of which decodes a two-bit Address to one-of-four active-low outputs. Active-low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 25 Equivalent Gates

MC54/74HC139



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



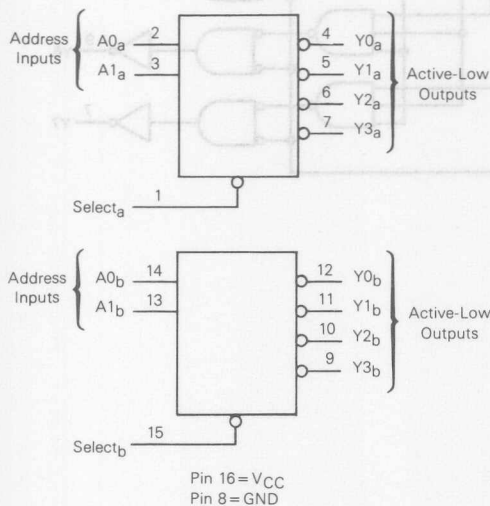
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

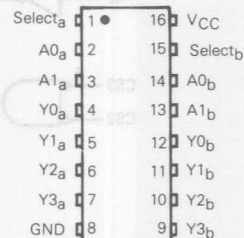
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs			
Select	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don't care

MC54/74HC139

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ 0 $V_{CC} = 4.5 \text{ V}$ 0 $V_{CC} = 6.0 \text{ V}$ 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC139

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 1 and 3)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 3)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Decoder) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		55	

SWITCHING WAVEFORMS

FIGURE 1

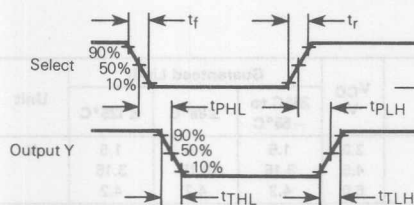


FIGURE 2

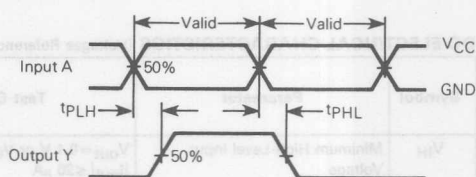
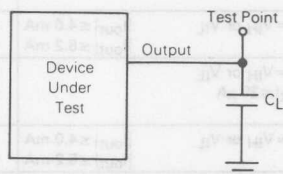


FIGURE 3 — TEST CIRCUIT



* Includes all probe and jig capacitance.

PIN DESCRIPTIONS

ADDRESS INPUTS

A0_a, A1_a, A0_b, A1_b (PINS 2, 3, 14, 13) — Address inputs. These inputs, when the respective 1-of-4 decoder is enabled, determine which of its four active-low outputs is selected.

CONTROL INPUTS

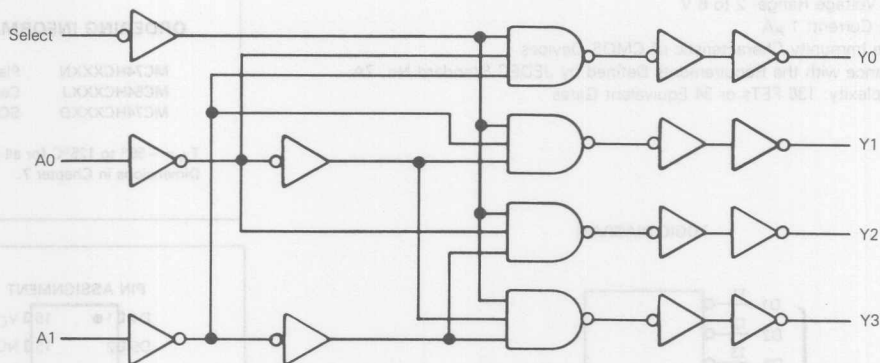
Select_a, Select_b (PINS 1, 15) — Active-low select inputs. For a low level on this input, the outputs for that particular

decoder follow the Address inputs. A high level on this input forces all outputs to a high level.

OUTPUTS

Y0_a-Y3_a, Y0_b-Y3_b (PINS 4-7, 12, 11, 10, 9) — Active-low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

EXPANDED LOGIC DIAGRAM
($\frac{1}{2}$ OF DEVICE)



FUNCTION TABLE

Inputs	Outputs
A1 A0	Y0 Y1 Y2 Y3
0 0	0 1 1 1
0 1	1 0 1 1
1 0	1 1 0 1
1 1	1 1 1 0
0 0	1 1 1 1
0 1	0 0 1 1
1 0	0 1 0 1
1 1	0 1 1 0
0 0	1 1 1 1
0 1	0 0 1 1
1 0	0 1 0 1
1 1	0 1 1 0
0 0	1 1 1 1
0 1	0 0 1 1
1 0	0 1 0 1
1 1	0 1 1 0

Advance Information

Decimal-to-BCD Encoder

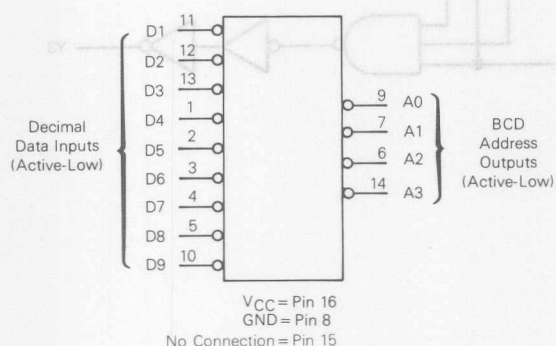
High-Performance Silicon-Gate CMOS

The MC54/74HC147 is identical in pinout to the LS147. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

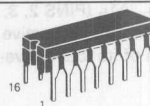
This device encodes nine active-low data inputs to four active-low BCD Address Outputs, ensuring that only the highest order active data line is encoded. The implied decimal zero condition is encoded when all nine data inputs are at a high level (inactive).

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates

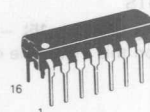
LOGIC DIAGRAM



MC54/74HC147



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

D4	1	16	VCC
D5	2	15	NC
D6	3	14	A3
D7	4	13	D3
D8	5	12	D2
A2	6	11	D1
A1	7	10	D9
GND	8	9	A0

NC = No Connection

FUNCTION TABLE

Inputs									Outputs			
D9	D8	D7	D6	D5	D4	D3	D2	D1	A3	A2	A1	A0
H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	L
H	H	H	H	H	H	H	L	X	H	H	L	H
H	H	H	H	H	H	L	X	X	H	H	L	L
H	H	H	H	L	X	X	X	X	H	L	H	H
H	H	H	L	X	X	X	X	X	H	L	L	L
H	H	L	X	X	X	X	X	X	H	L	L	L
H	L	X	X	X	X	X	X	X	L	H	H	H
L	X	X	X	X	X	X	X	X	L	H	H	L

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC147

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ 0 $V_{CC} = 4.5 \text{ V}$ 0 $V_{CC} = 6.0 \text{ V}$ 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC147

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Output A (Figures 1 and 2)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

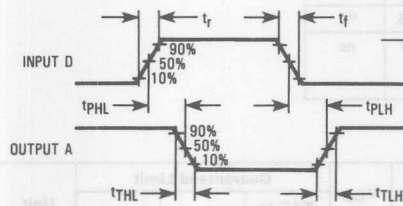
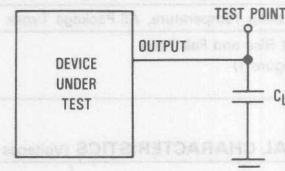
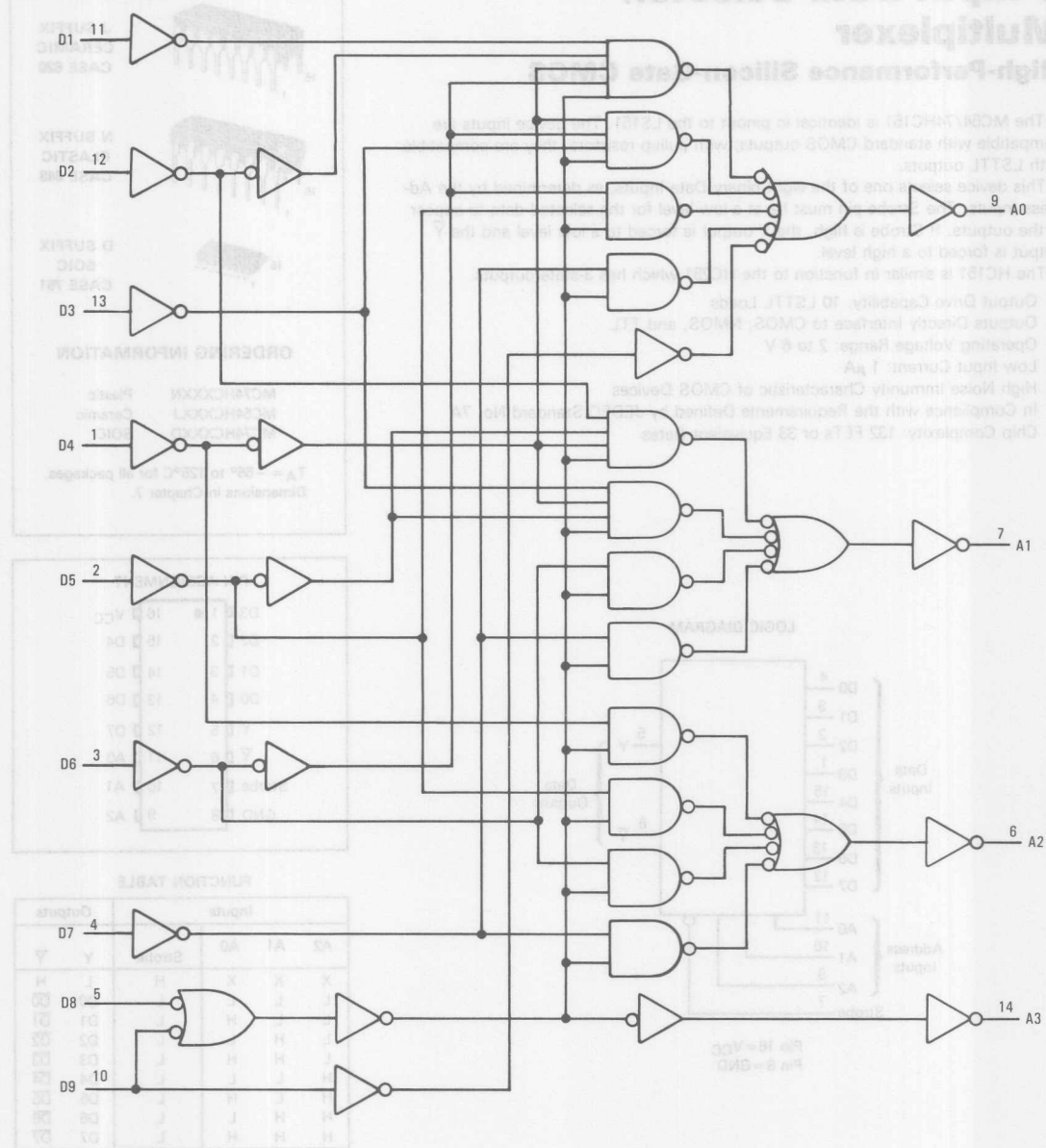


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit



8-Input Data Selector/ Multiplexer

High-Performance Silicon-Gate CMOS

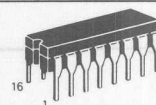
The MC54/74HC151 is identical in pinout to the LS151. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Strobe pin must be at a low level for the selected data to appear at the outputs. If Strobe is high, the Y output is forced to a low level and the \bar{Y} output is forced to a high level.

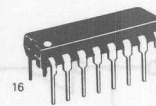
The HC151 is similar in function to the HC251 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 132 FETs or 33 Equivalent Gates

MC54/74HC151



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



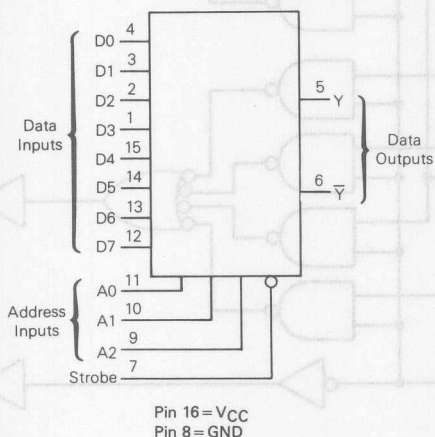
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

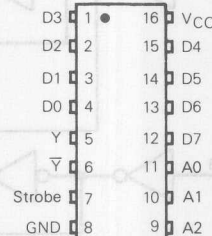
MC74HCXXXN Plastic
MC54HCXXXJ Ceramic
MC74HCXXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs	
A2	A1	A0	Strobe	Y	\bar{Y}
X	X	X	H	L	H
L	L	L	L	D0	\bar{D}_0
L	L	H	L	D1	\bar{D}_1
L	H	L	L	D2	\bar{D}_2
L	H	H	L	D3	\bar{D}_3
H	L	L	L	D4	\bar{D}_4
H	L	H	L	D5	\bar{D}_5
H	H	L	L	D6	\bar{D}_6
H	H	H	L	D7	\bar{D}_7

D0, D1, . . . D7 = the level of the respective D input

MC54/74HC151

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} ,V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC151

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input D to Output Y or \bar{Y} (Figures 1, 3 and 6)	2.0	185	230	280	ns
		4.5	37	46	56	
		6.0	31	39	48	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y or \bar{Y} (Figures 2 and 6)	2.0	205	255	310	ns
		4.5	41	51	62	
		6.0	35	43	53	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Strobe to Output Y or \bar{Y} (Figures 4, 5 and 6)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		36	pF

PIN DESCRIPTIONS

INPUTS

D0, D1, . . . , D7 (PINS 4, 3, 2, 1, 15, 14, 13, 12) — Data inputs. Data on any one of these eight binary inputs may be selected to appear on the output.

STROBE (PIN 7) — Strobe. This input pin must be at a low level for the selected data to appear at the outputs. If the Strobe pin is high, the Y output is forced to a low level and the \bar{Y} output is forced to a high level.

CONTROL INPUTS

A0, A1, A2 (PINS 11, 10, 9) — Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

OUTPUTS

Y, \bar{Y} (PINS 5, 6) — Data outputs. The selected data is presented at these pins in both true (Y output) and complemented (\bar{Y} output) forms.

5

Symbol	Parameter	Guaranteed Limit	Typical	Unit
V_{IL}	Maximum Low-Level Input Voltage	$V_{IL} \leq 0.8 V_{CC}$	0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{OH} \geq V_{CC} - 0.1 V$	4.9	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{OL} \leq V_{CC} - 0.1 V$	0.1	V
I_{IH}	Maximum Input High-Level Current	$I_{IH} \leq -1 \mu A$	0.1	μA
I_{IL}	Maximum Input Low-Level Current	$I_{IL} \leq -1 \mu A$	0.1	μA
I_{OH}	Maximum Output High-Level Current	$I_{OH} \leq -10 \mu A$	10	μA
I_{OL}	Maximum Output Low-Level Current	$I_{OL} \leq 10 \mu A$	10	μA

MC54/74HC151

SWITCHING WAVEFORMS

FIGURE 1

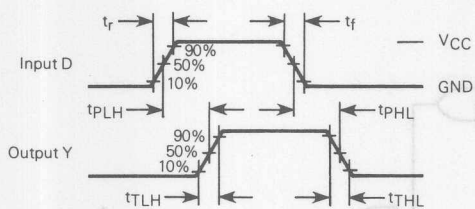


FIGURE 2

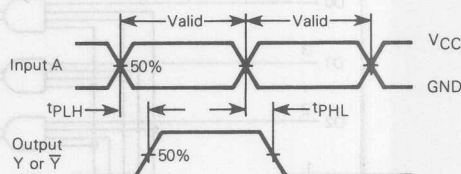


FIGURE 3

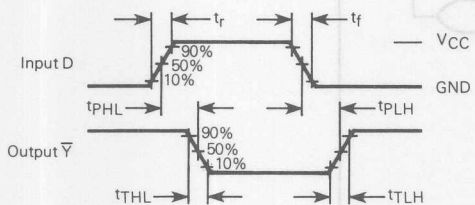


FIGURE 4

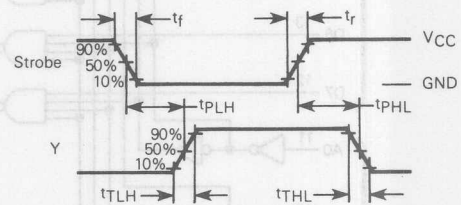


FIGURE 5

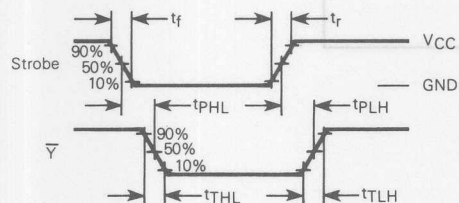
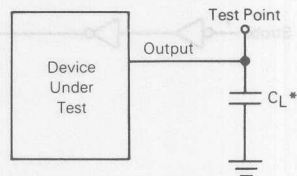
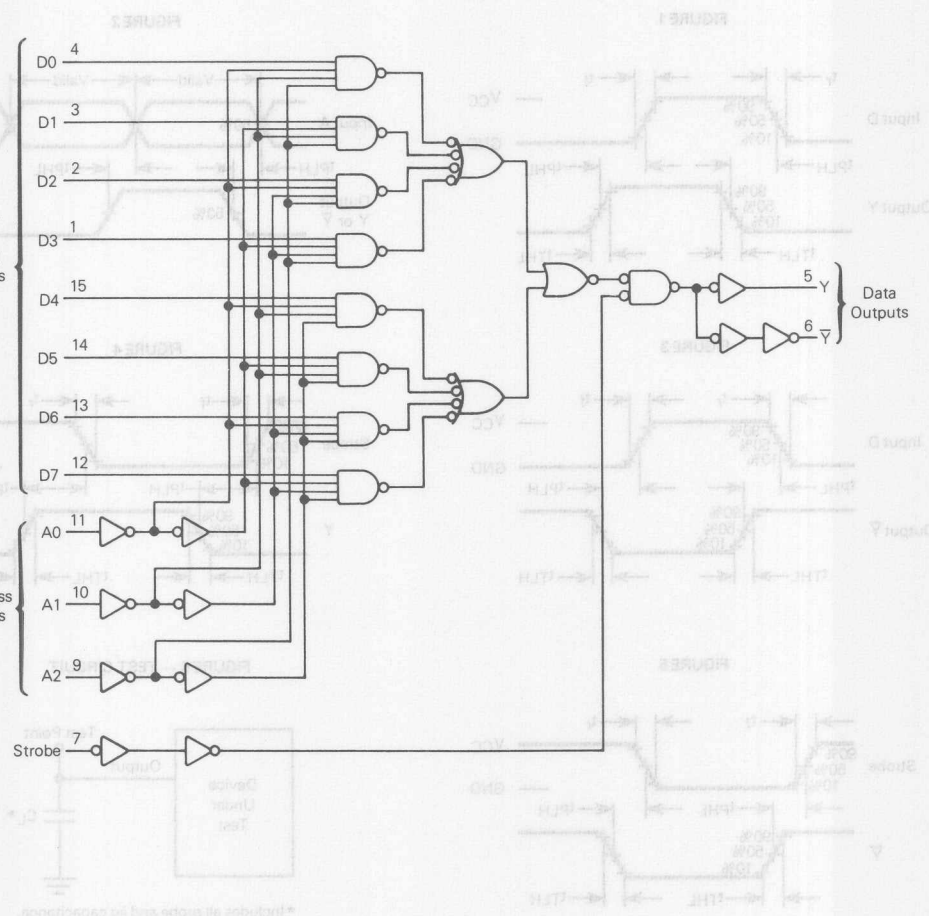


FIGURE 6 — TEST CIRCUIT



* Includes all probe and jig capacitance.



MC54/74HC153

Dual 4-Input Data Selector/ Multiplexer

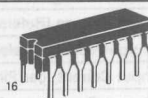
High-Performance Silicon-Gate CMOS

The MC54/74HC153 is identical in pinout to the LS153. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

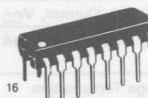
The Address Inputs select one of four Data Inputs from each multiplexer. Each multiplexer has an active-low Strobe control and a noninverting output.

The HC153 is similar in function to the HC253, which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



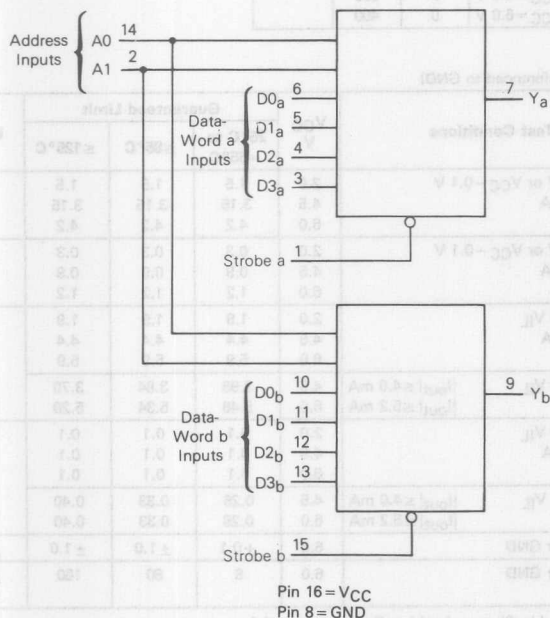
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Strobe a	1	16	VCC
A1	2	15	Strobe b
D3a	3	14	A0
D2a	4	13	D3b
D1a	5	12	D2b
D0a	6	11	D1b
Ya	7	10	D0b
GND	8	9	Yb

FUNCTION TABLE

Inputs			Output
A1	A0	Strobe	Y
X	X	H	L
L	L	L	D0
L	H	L	D1
H	L	L	D2
H	H	L	D3

D0, D1, D2, and D3 = the level of the respective Data Input

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC153

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Output Y (Figures 1 and 4)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Strobe to Output Y (Figures 3 and 4)	2.0	95	120	145	ns
		4.5	19	24	29	
		6.0	16	20	25	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Multiplexer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		31	

SWITCHING WAVEFORMS

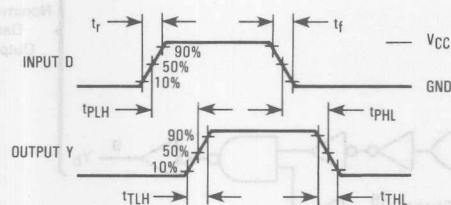


Figure 1

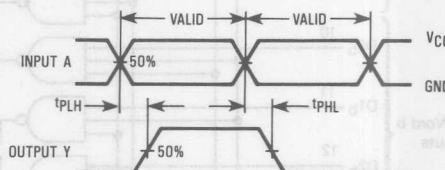


Figure 2

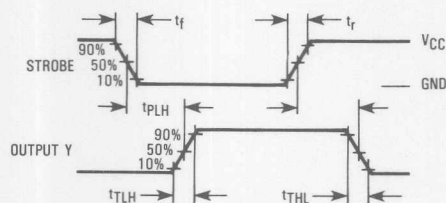
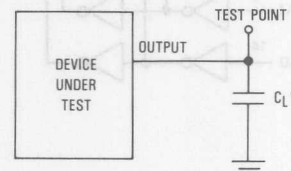


Figure 3



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

DATA INPUTS

D0_a-D3_a, D0_b-D3_b (PINS 3, 4, 5, 6, 10, 11, 12, 13) — Data Inputs. With the outputs enabled, the addressed Data Inputs appear at the Y outputs.

CONTROL INPUTS

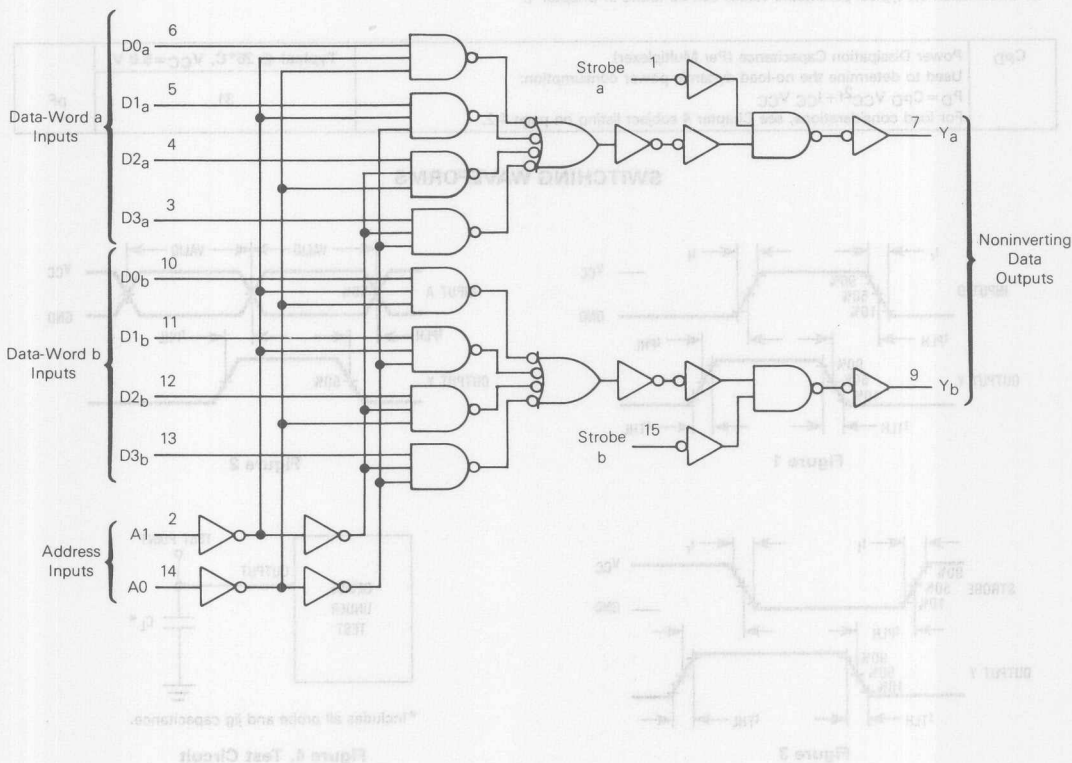
A0, A1 (PINS 2, 14) — Address Inputs. These inputs address the pair of Data Inputs which appear at the corresponding outputs.

STROBE (PINS 1, 15) — Active-low Strobe. A low level applied to these pins enables the corresponding outputs.

OUTPUTS

Y_a, Y_b (PINS 7, 9) — Noninverting data outputs.

EXPANDED LOGIC DIAGRAM



MC54/74HC154

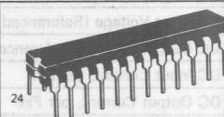
1-of-16 Decoder/Demultiplexer High-Performance Silicon-Gate CMOS

The MC54/74HC154 is identical in pinout to the LS154. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

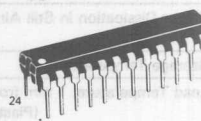
This device, when enabled, selects one of 16 active-low outputs. Two active-low Chip Selects are provided to facilitate the chip-select, demultiplexing, and cascading functions. When either Chip Select is high, all outputs are high. The demultiplexing function is accomplished by using the Address inputs to select the desired device output. Then, while holding one chip select input low, data can be applied to the other chip select input (see Application Note).

The HC154 is primarily used for memory address decoding and data routing applications.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 192 FETs or 48 Equivalent Gates



J SUFFIX
CERAMIC
CASE 758



N SUFFIX
PLASTIC
CASE 724



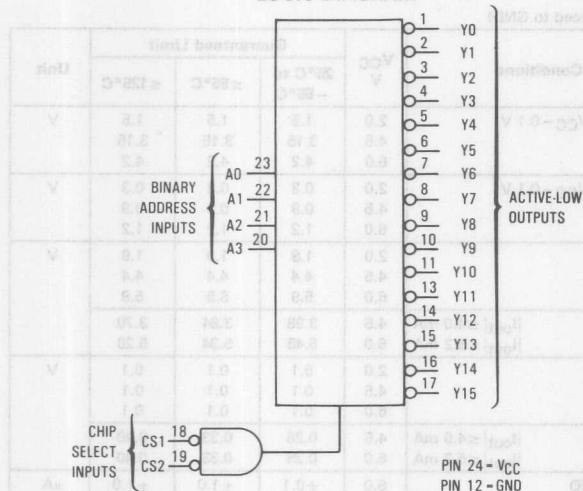
DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ\text{C}$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Y0	1	24	V _{CC}
Y1	2	23	A0
Y2	3	22	A1
Y3	4	21	A2
Y4	5	20	A3
Y5	6	19	CS2
Y6	7	18	CS1
Y7	8	17	Y15
Y8	9	16	Y14
Y9	10	15	Y13
Y10	11	14	Y12
GND	12	13	Y11

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 2)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC154

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to –55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, CS to Output Y (Figures 2 and 3)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		80	

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (PINS 23, 22, 21, 20) — Address inputs. These inputs, when the 1-of-16 decoder is enabled, determine which of its sixteen active-low outputs is selected.

select inputs are active. These outputs remain high when not addressed or a chip-select input is high.

CONTROL INPUTS

CS1, CS2 (PINS 18, 19) — Active-low chip-select inputs. With low levels on both of these inputs, the outputs of the decoder follow the Address inputs. A high level on either input forces all outputs high.

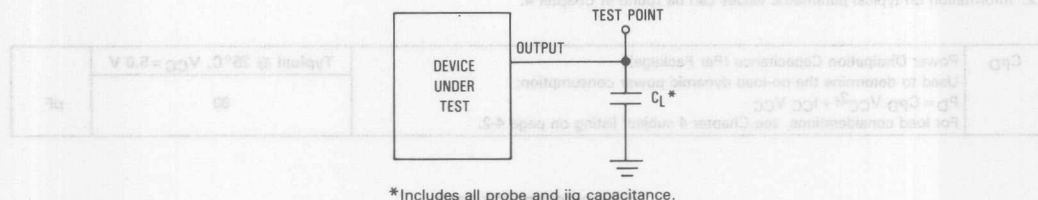
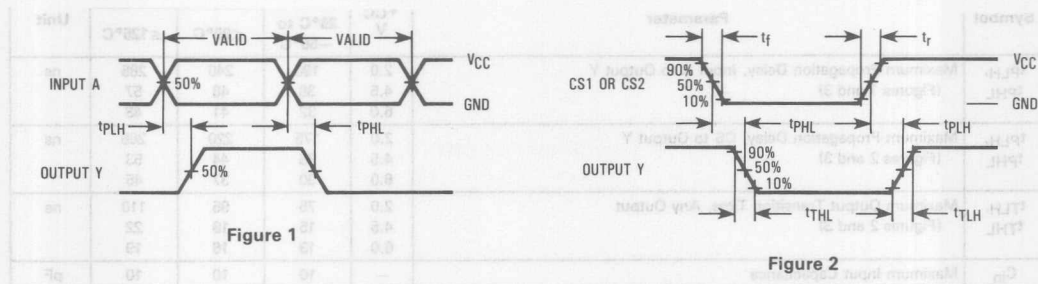
OUTPUTS

Y0-Y15 (PINS 1-11, 13-17) — Active-low outputs. These outputs assume a low level when addressed and both chip-

FUNCTION TABLE

[illegible]

H = High Level, L = Low Level, X = Don't Care

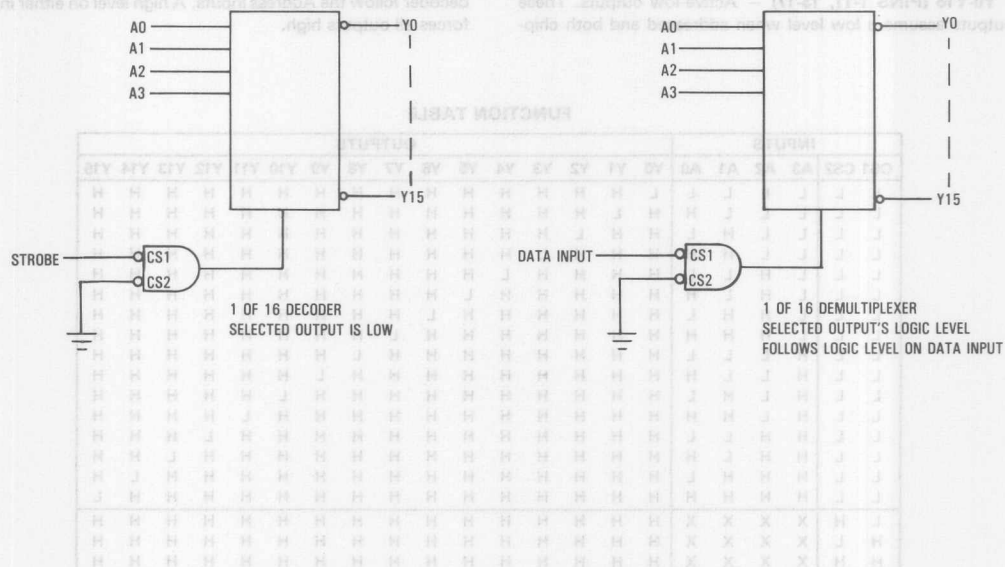


TYPICAL APPLICATIONS

With low levels on both of these inputs, the output of the decoder follows the address input. A high level on either input forces the output high.

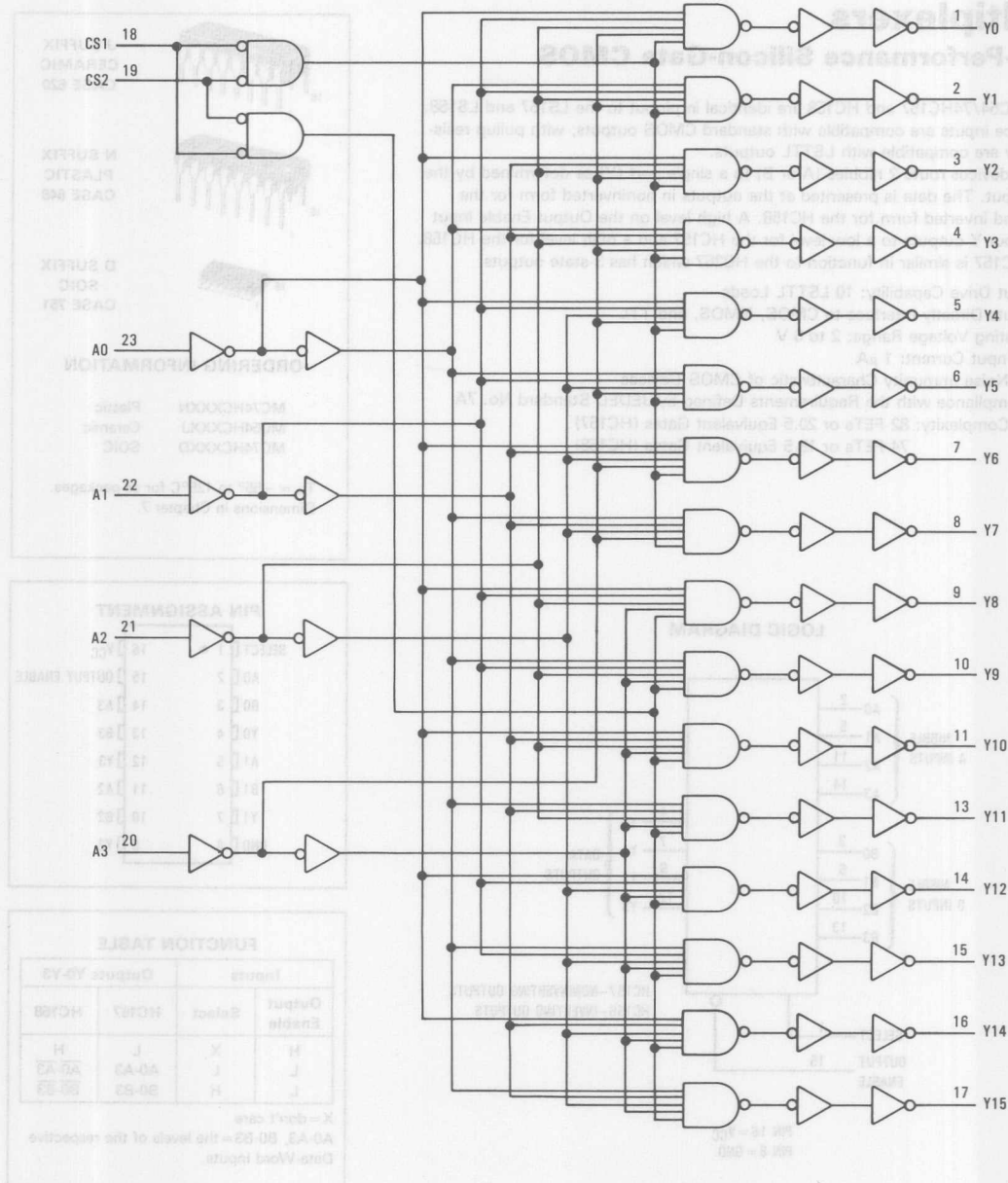
1 OF 16 DECODER
SELECTED OUTPUT IS LOW

1 OF 16 DEMULTIPLEXER
SELECTED OUTPUT'S LOGIC LEVEL
FOLLOWS LOGIC LEVEL ON DATA INPUT



MC54/74HC154

EXPANDED LOGIC DIAGRAM



Quad 2-Input Data Selectors/ Multiplexers

High-Performance Silicon-Gate CMOS

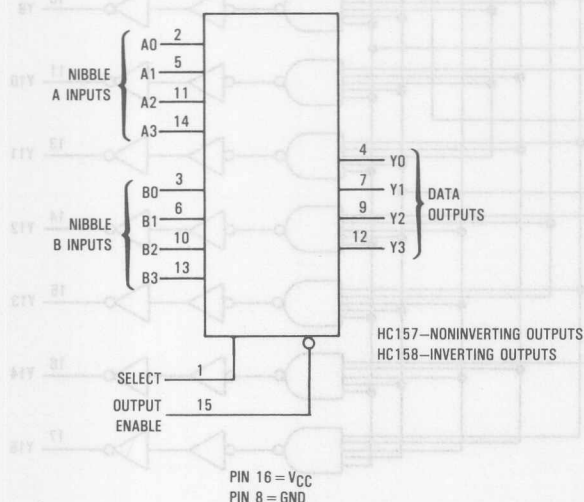
The MC54/74HC157 and HC158 are identical in pinout to the LS157 and LS158. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices route 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form for the HC157 and inverted form for the HC158. A high level on the Output Enable input sets all four Y outputs to a low level for the HC157 and a high level for the HC158.

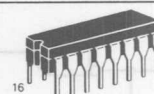
The HC157 is similar in function to the HC257 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 82 FETs or 20.5 Equivalent Gates (HC157)
 74 FETs or 18.5 Equivalent Gates (HC158)

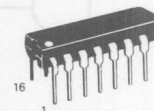
LOGIC DIAGRAM



MC54/74HC157 MC54/74HC158



J SUFFIX
 CERAMIC
 CASE 620



N SUFFIX
 PLASTIC
 CASE 648



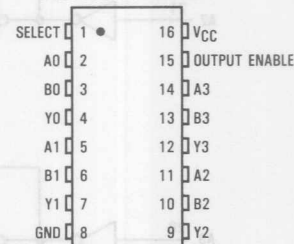
D SUFFIX
 SOIC
 CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs Y0-Y3	
Output Enable	Select	HC157	HC158
H	X	L	H
L	L	A0-A3	A0-A3
L	H	B0-B3	B0-B3

X = don't care
 A0-A3, B0-B3 = the levels of the respective Data-Word Inputs.

MC54/74HC157•MC54/74HC158

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC157•MC54/74HC158

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1, 2, and 7)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 3, 4, and 7)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Output Enable to Output Y (Figures 5, 6, and 7)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1, 2, and 7)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		33 (HC157) 35 (HC158)	

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (PINS 2, 5, 11, 14) — Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form for the HC157 and inverted form for the HC158.

B0, B1, B2, B3 (PINS 3, 6, 10, 13) — Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form for the HC157 and inverted form for the HC158.

OUTPUTS

Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12) — Data outputs. The selected input Nibble is presented at these outputs when the

Output Enable input is at a low level. The data present on these pins is in its noninverted form for the HC157 and inverted form for the HC158. For the Output Enable input at a high level, the outputs are at a low level for the HC157 and at a high level for the HC158.

CONTROL INPUTS

SELECT (PIN 1) — Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

OUTPUT ENABLE (PIN 15) — Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level for the HC157 and to a high level for the HC158.

MC54/74HC157•MC54/74HC158

SWITCHING WAVEFORMS

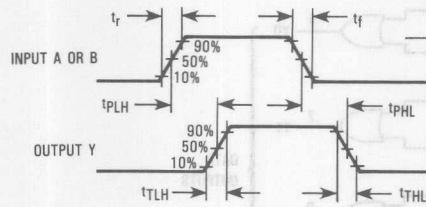


Figure 1. HC157

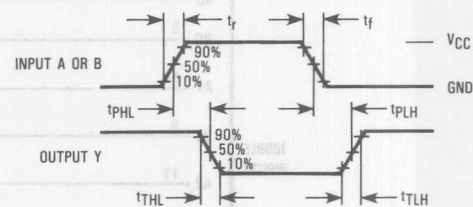


Figure 2. HC158

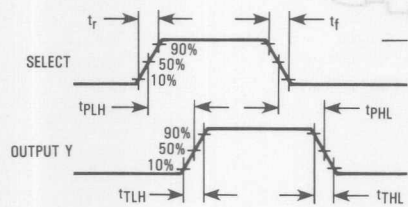


Figure 3. Y vs Select, Noninverted

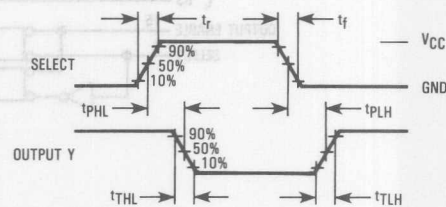


Figure 4. Y vs Select, Inverted

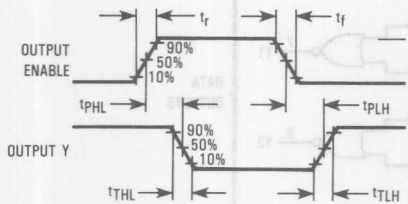


Figure 5. HC157

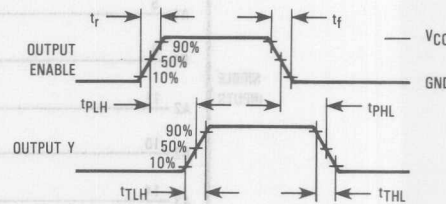
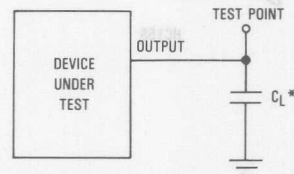
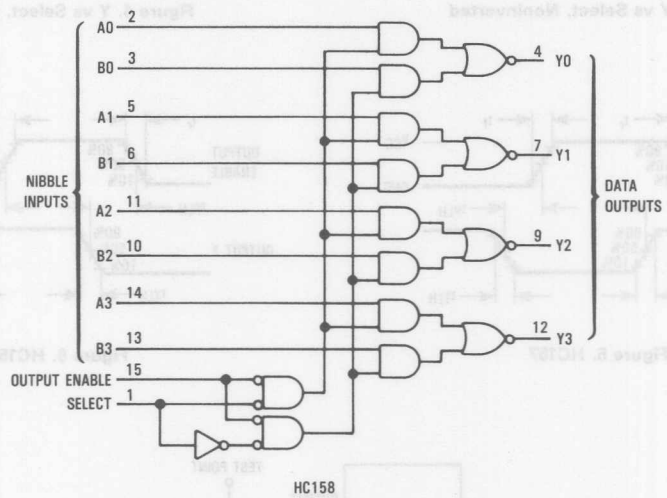
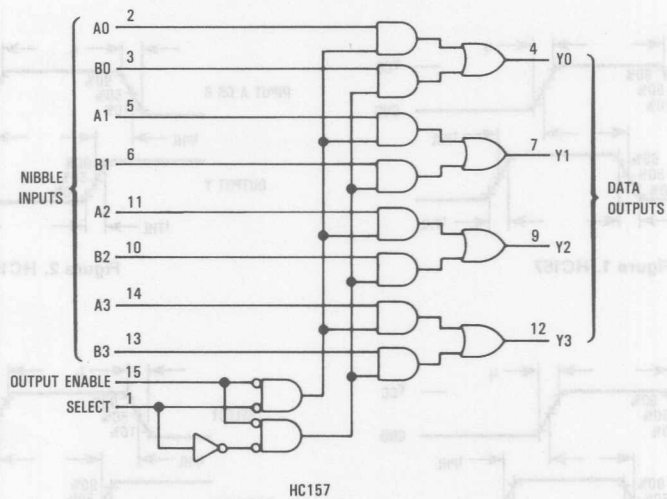


Figure 6. HC158



*Includes all probe and jig capacitance.

Figure 7. Test Circuit



Presettable Counters

High-Performance Silicon-Gate CMOS

The MC54/74HC160 through HC163 are identical in pinout to the LS160 through LS163, respectively. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC160 and HC162 are programmable BCD counters with asynchronous and synchronous Reset inputs, respectively. The HC161 and HC163 are programmable 4-bit binary counters with asynchronous and synchronous reset, respectively.

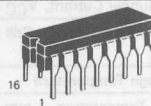
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates

MC54/74HC160

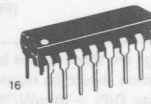
MC54/74HC161

MC54/74HC162

MC54/74HC163



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



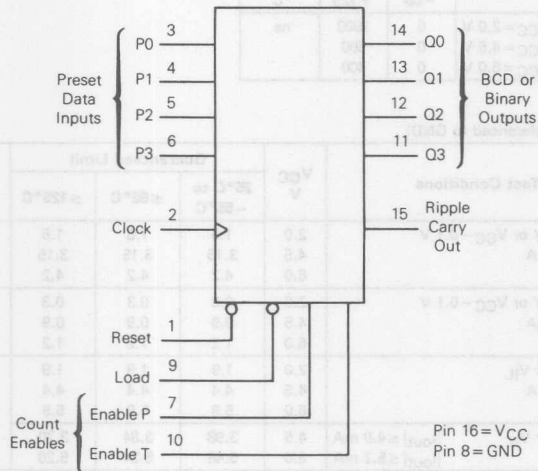
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

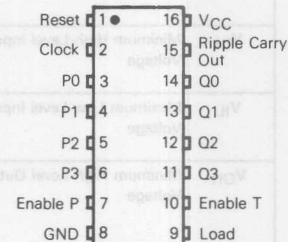
MC74HCXXXN Plastic
MC54HCXXXJ Ceramic
MC74HCXXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



Device	Count Mode	Reset Mode
HC160	BCD	Asynchronous
HC161	Binary	Asynchronous
HC162	BCD	Synchronous
HC163	Binary	Synchronous

Inputs					Output
Clock	Reset*	Load	Enable P	Enable T	Q
	L	X	X	X	Reset
	H	L	X	X	Load Preset Data
	H	H	H	H	Count
	H	H	L	X	No Count
	H	H	X	L	No Count

*HC162 and HC163 only. HC160 and HC161 are Asynchronous-Reset Devices

H = high level
L = low level
X = don't care

MC54/74HC160•MC54/74HC161•MC54/74HC162•MC54/74HC163

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC160•MC54/74HC161•MC54/74HC162•MC54/74HC163

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)* (Figures 1 and 7)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 7)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 7)	2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (HC160 and HC161 Only) (Figures 2 and 7)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t_{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 3 and 7)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t_{PHL}	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 3 and 7)	2.0 4.5 6.0	195 39 33	245 49 42	295 59 50	ns
t_{PLH}	Maximum Propagation Delay, Clock to Ripple Carry Out (Figures 1 and 7)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PHL}	Maximum Propagation Delay, Clock to Ripple Carry Out (Figures 1 and 7)	2.0 4.5 6.0	215 43 37	270 54 46	325 65 55	ns
t_{PHL}	Maximum Propagation Delay, Reset to Ripple Carry Out (HC160 and HC161 Only) (Figures 2 and 7)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
$t_{TLH},$ t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 7)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

*Applies to noncascaded/nonsynchronously clocked configurations only. With synchronously cascaded counters, (1) Clock to Ripple Carry Out propagation delays, (2) Enable T or Enable P to Clock setup times, and (3) Clock to Enable T or Enable P hold times determine f_{max} . However, if Ripple Carry Out of each stage is tied to the Clock of the next stage (nonsynchronously clocked), the f_{max} in the table above is applicable. See Applications Information in this data sheet.

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		60	

MC54/74HC160•MC54/74HC161•MC54/74HC162•MC54/74HC163

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock (Figure 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{su}	Minimum Setup Time, Load to Clock (Figure 5)	2.0	135	170	205	ns
		4.5	27	34	41	
		6.0	23	29	35	
t_{su}	Minimum Setup Time, Reset to Clock (HC162 and HC163 only) (Figure 4)	2.0	160	200	240	ns
		4.5	32	40	48	
		6.0	27	34	41	
t_{su}	Minimum Setup Time, Enable T or Enable P to Clock (Figure 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t_h	Minimum Hold Time, Clock to Preset Data Inputs (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_h	Minimum Hold Time, Clock to Load (Figure 5)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t_h	Minimum Hold Time, Clock to Reset (HC162 and HC163 only) (Figure 4)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t_h	Minimum Hold Time, Clock to Enable T or Enable P (Figure 6)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (HC160 and HC161 only) (Figure 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t_{rec}	Minimum Recovery Time, Load Inactive to Clock (Figure 5)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Reset (HC160 and HC161 only) (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

FUNCTION DESCRIPTION

The HC160/161/162/163 are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count-enable controls.

The HC160 and HC162 are BCD counters with asynchronous Reset, and synchronous Reset, respectively. The HC161 and HC163 are binary counters with asynchronous Reset and synchronous Reset, respectively.

INPUTS

Clock (Pin 2) — The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting (HC162 and HC163) and loading occur with the rising edge of the Clock input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6) — These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (pin 3) is the least-significant bit and P3 (pin 6) is the most-significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11) — These are the counter outputs (BCD or binary). Q0 (pin 14) is the least-significant bit and Q3 (pin 11) is the most-significant bit.

Ripple Carry Out (Pin 15) — When the counter is in its maximum state (1001 for the BCD counters or 1111 for the binary counters), this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equations for this output are:

Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3
for BCD counters HC160 and HC162

Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3
for binary counters HC161 and HC163

CONTROL FUNCTIONS

Resetting — A low level on the Reset pin (pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to a low level. The HC160 and HC161 reset asynchronously, and the HC162 and HC163 reset with the rising edge of the Clock input (synchronous reset).

Loading — With the rising edge of the Clock, a low level on Load (pin 9) loads the data from the Preset Data Input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Although the HC160 and HC162 are BCD counters, they may be programmed to any state. If they are loaded with a state disallowed in BCD code, they will return to their normal count sequence within two clock pulses (see the Output State Diagram).

Count Enable/Disable — These devices have two count-enable control pins: Enable P (pin 7) and Enable T (pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \cdot \text{Enable T} \cdot \text{Load}$$

The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control; Enable T is both a count-enable and a Ripple-Carry Output control.

TABLE 1. COUNT ENABLE/DISABLE

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0-Q3	Ripple Carry Out
H	H	H	Count	High when Q0-Q3 are maximum*
L	H	H	No Count	High when Q0-Q3 are maximum*
X	L	H	No Count	High when Q0-Q3 are maximum*
X	X	L	No Count	L

*Q0 through Q3 are maximum for the HC160 and HC162 when Q3 Q2 Q1 Q0 = 1001.

Q0 through Q3 are maximum for the HC161 and HC163 when Q3 Q2 Q1 Q0 = 1111.

OUTPUT STATE DIAGRAMS

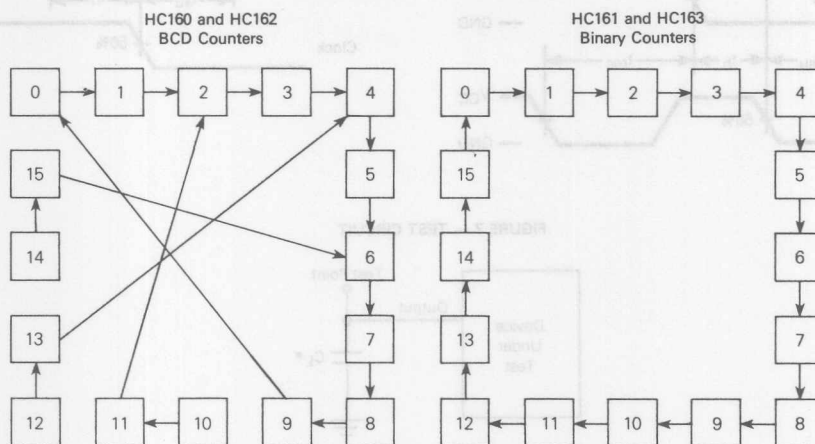


FIGURE 1

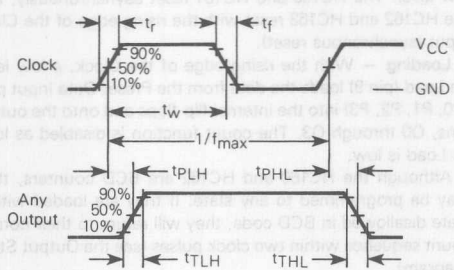


FIGURE 3

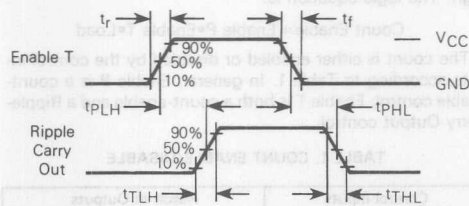


FIGURE 5

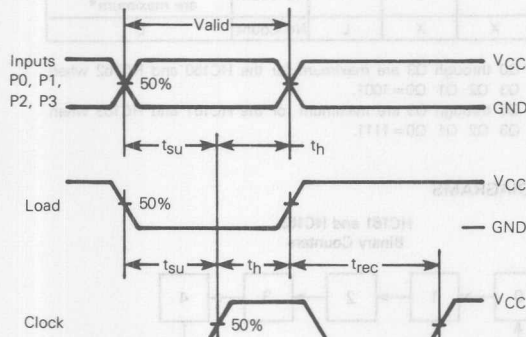
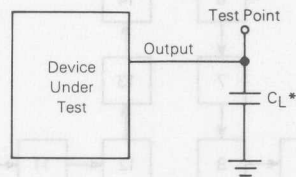


FIGURE 7 — TEST CIRCUIT



* Includes all probe and jig capacitance.

FIGURE 2

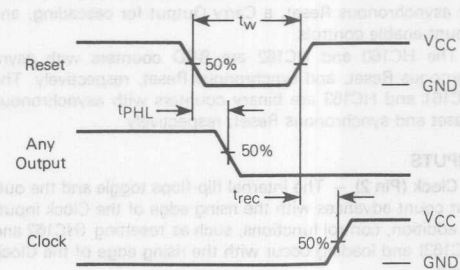


FIGURE 4 — HC162 AND HC163 ONLY

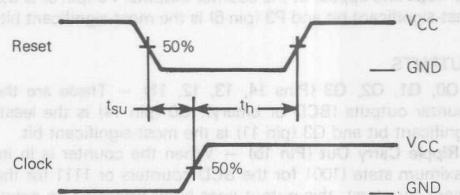
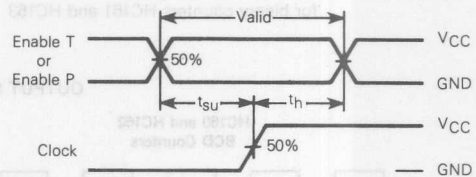
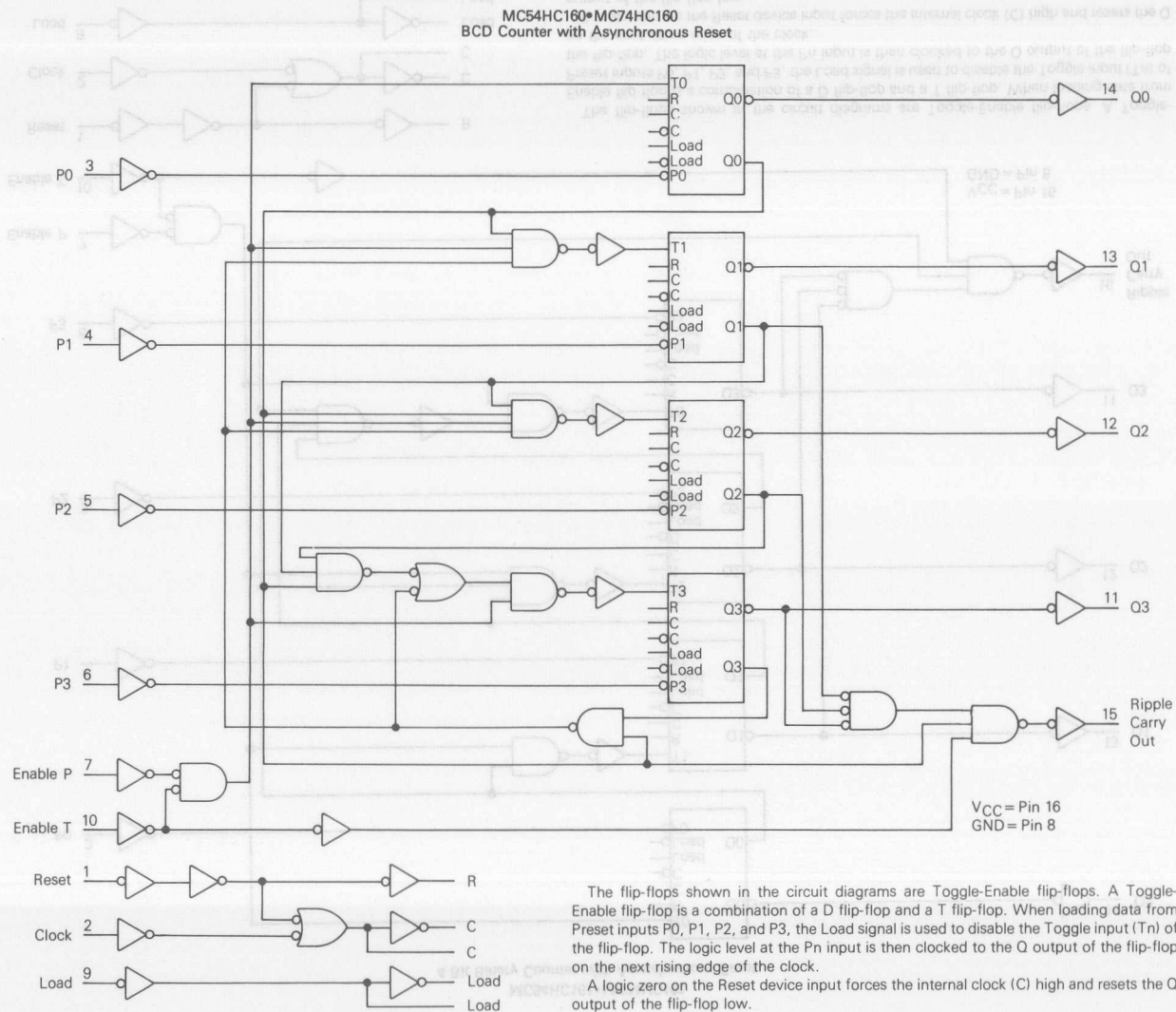


FIGURE 6



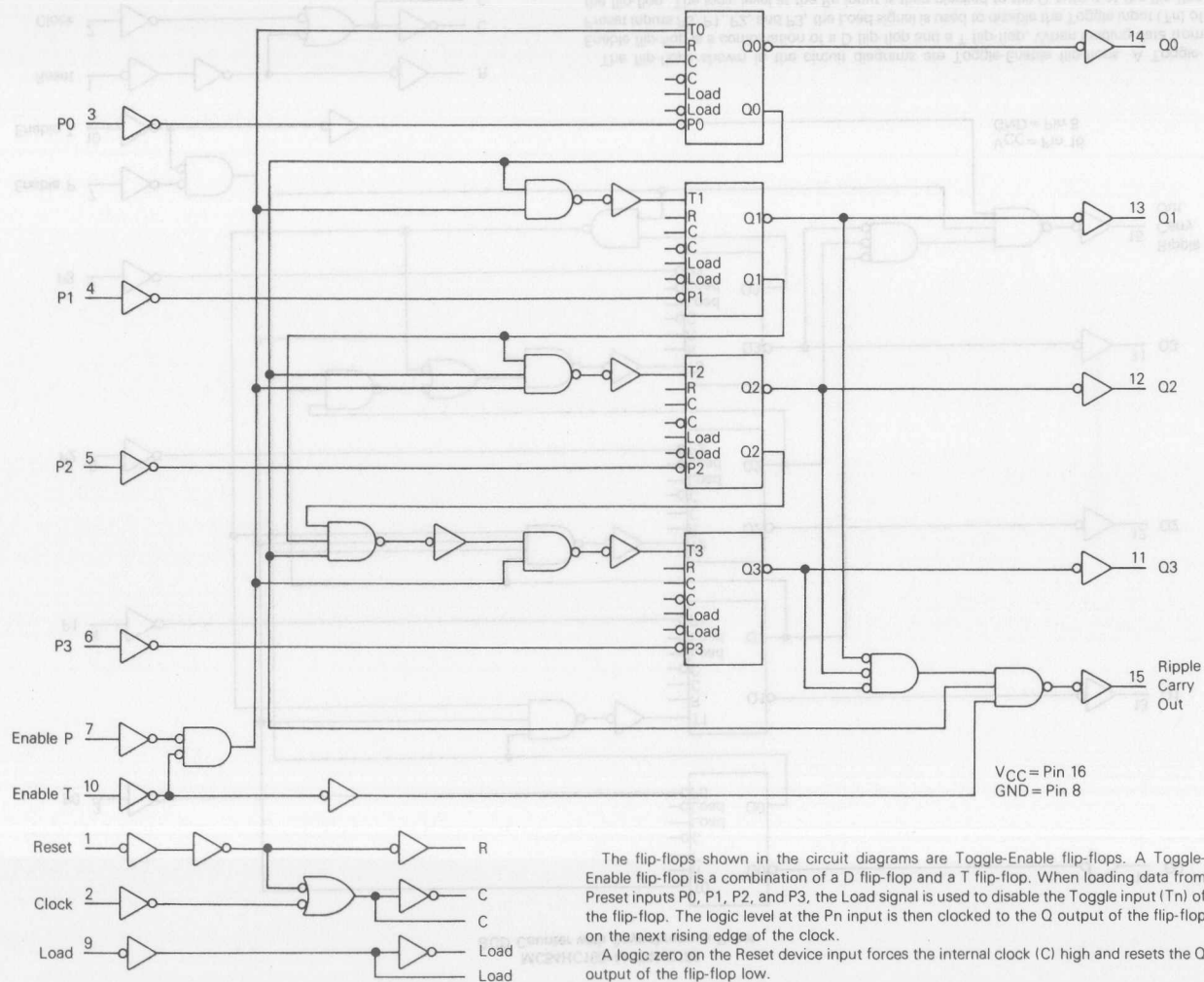
MC54HC160•MC74HC160
BCD Counter with Asynchronous Reset



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

MC54HC161•MC74HC161
4-Bit Binary Counter with Asynchronous Reset



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

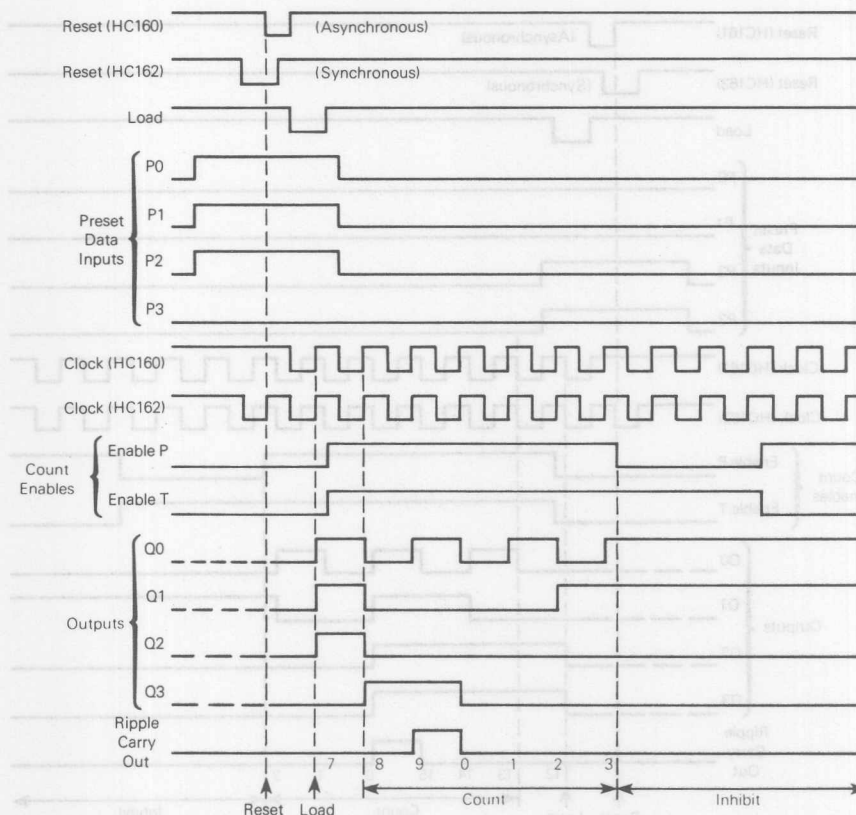
A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

MC54/74HC160•MC54/74HC161•MC54/74HC162•MC54/74HC163

HC160, HC162 TIMING DIAGRAM

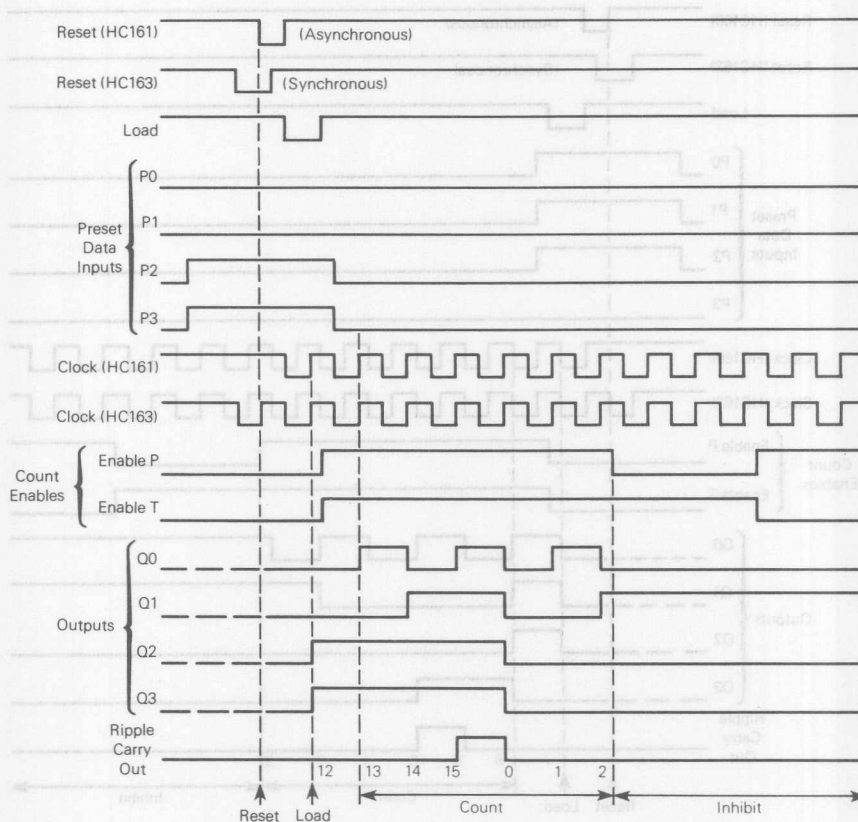
Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.



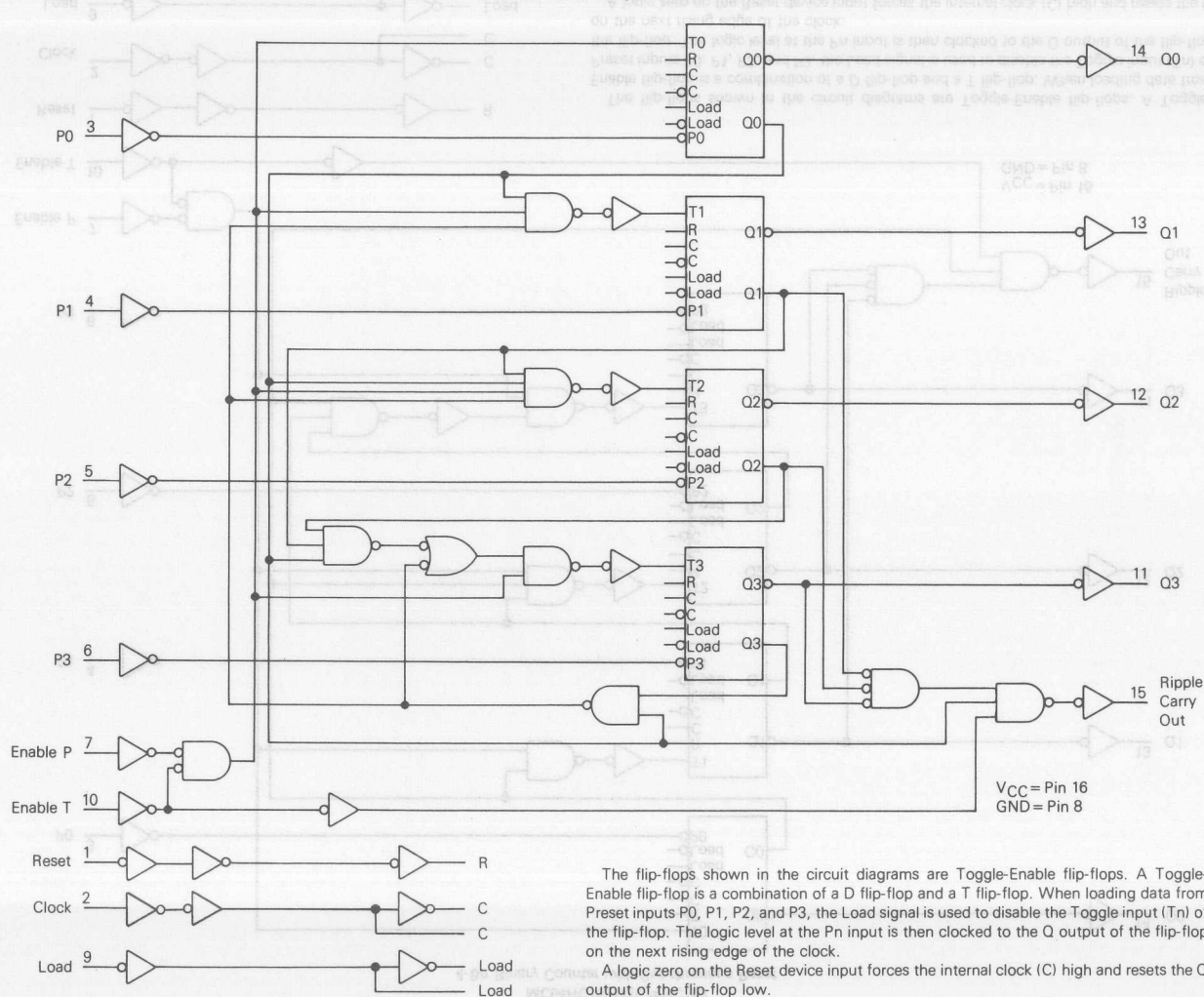
Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

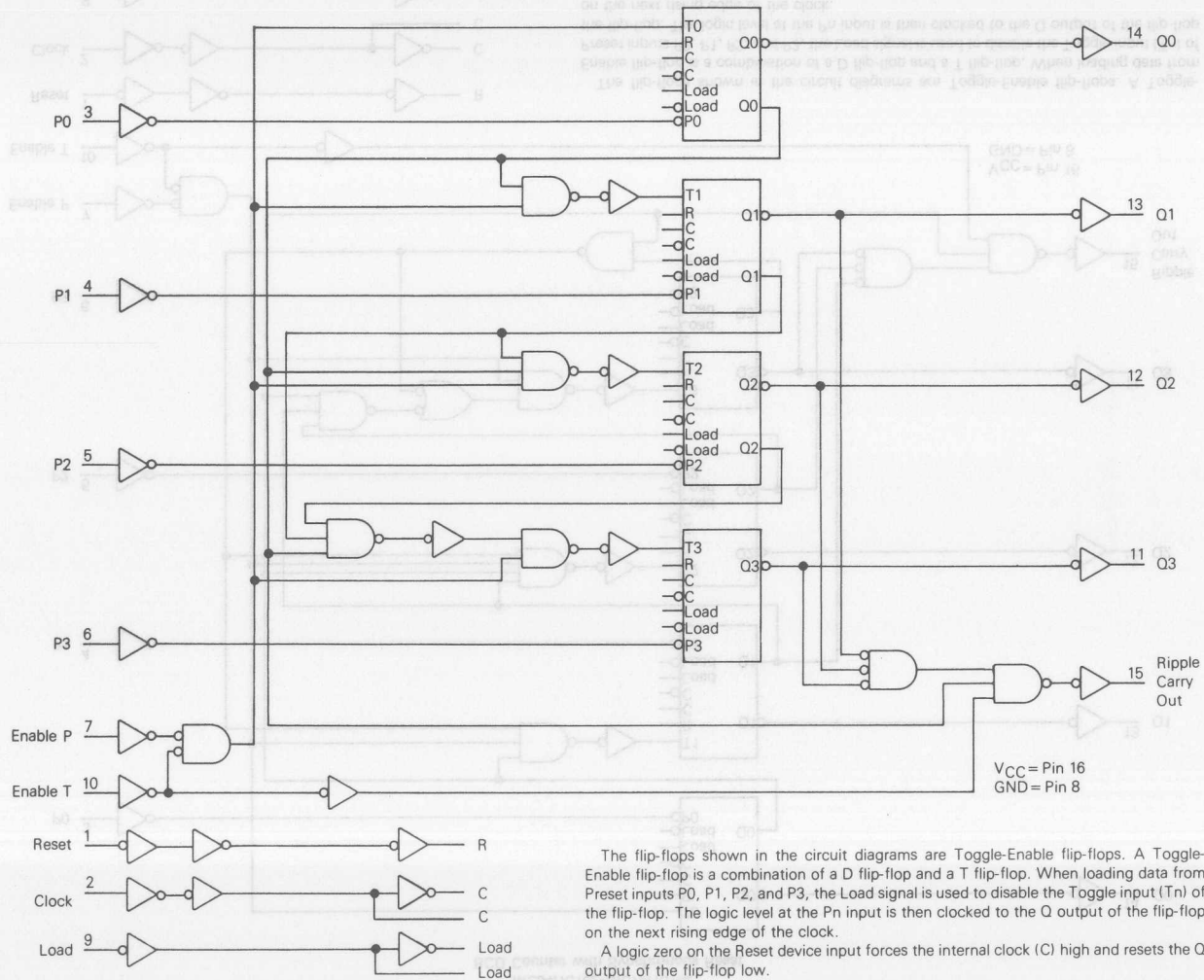


5

MC54HC162•MC74HC162
BCD Counter with Synchronous Reset



MC54HC163•MC74HC163
4-Bit Binary Counter with Synchronous Reset

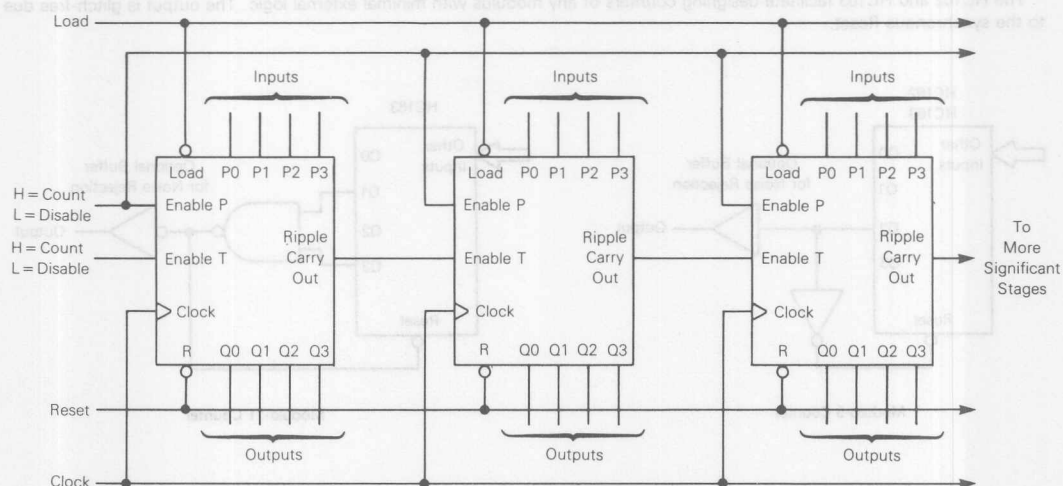


The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

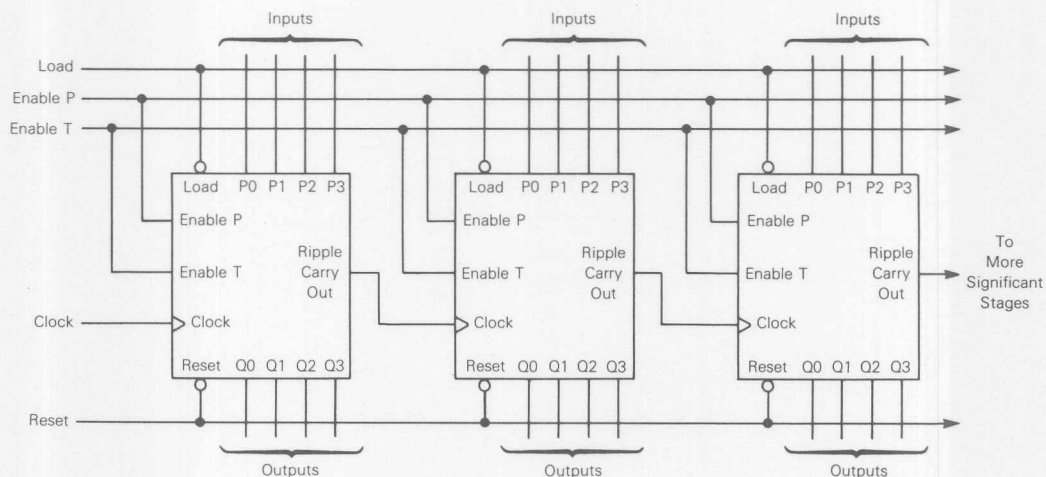
TYPICAL APPLICATIONS
CASCADING

N-Bit Synchronous Counters



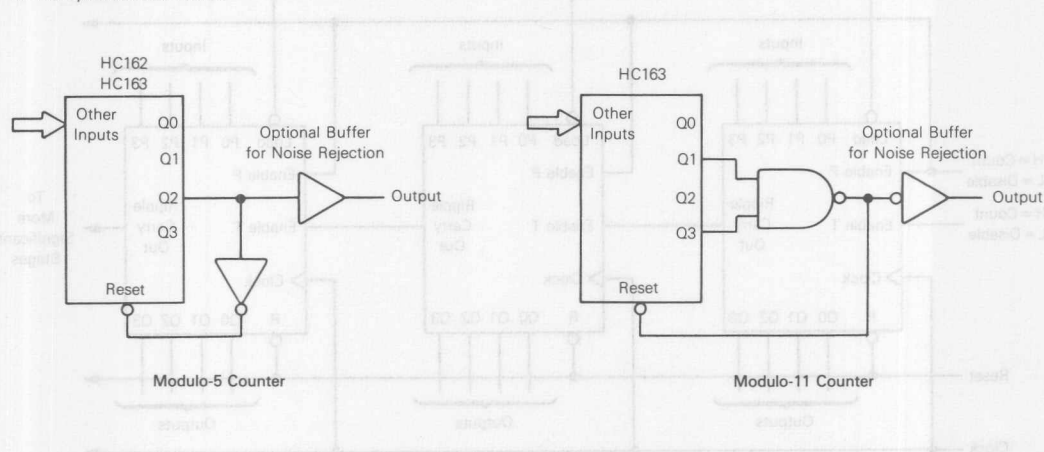
NOTE: When used in these cascaded configurations the clock f_{max} guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.

Nibble Ripple Counter



TYPICAL APPLICATIONS
VARYING THE MODULUS

The HC162 and HC163 facilitate designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous Reset.



MC54/74HC164

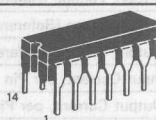
8-Bit Serial-Input/Parallel-Output Shift Register

High-Performance Silicon-Gate CMOS

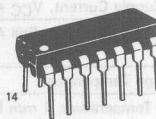
The MC54/74HC164 is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC54/74HC164 is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



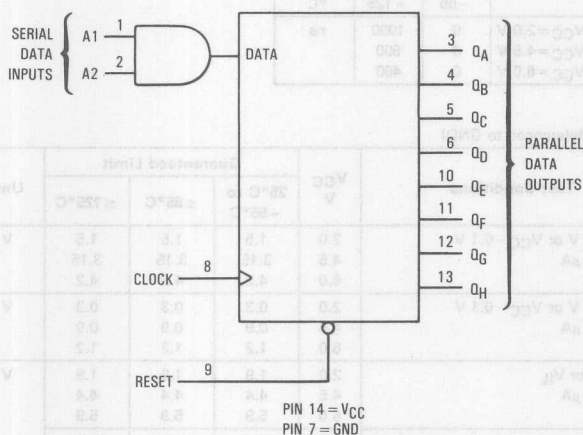
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

A1	1	14	V _{CC}
A2	2	13	Q _H
Q _A	3	12	Q _G
Q _B	4	11	Q _F
Q _C	5	10	Q _E
Q _D	6	9	RESET
GND	7	8	CLOCK

FUNCTION TABLE

Inputs				Outputs			
Reset	Clock	A1	A2	Q _A	Q _B	...	Q _H
L	X	X	X	L	L	...	L
H		X	X	no change			
H		H	D	D	Q _{An} ...	Q _{Gn}	
H		D	H	D	Q _{An} ...	Q _{Gn}	

D = data input
Q_{An} - Q_{Gn} = data shifted from the previous stage on a rising edge at the clock input.

V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C

Ceramic DIP: −10 mW/°C from 100° to 125°C

SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} − 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} − 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC164

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		140	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t _h	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC164

PIN DESCRIPTIONS

INPUTS

A1, A2 (PINS 1, 2) — Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data-enable input. When only one serial input is used, the other must be connected to V_{CC} .

CLOCK (PIN 8) — Shift Register Clock. A positive-going transition on this pin shifts the data at each stage to the next stage. The shift register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

OUTPUTS

$Q_A - Q_H$ (PINS 3, 4, 5, 6, 10, 11, 12, 13) — Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

CONTROL INPUT

RESET (PIN 9) — Active-Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip-flops and sets outputs $Q_A - Q_H$ to the low level state.

SWITCHING WAVEFORMS

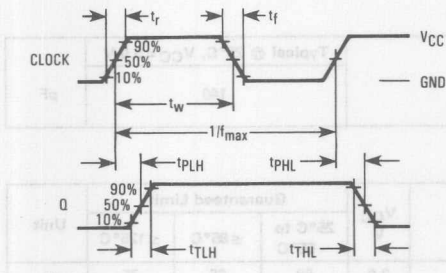


Figure 1

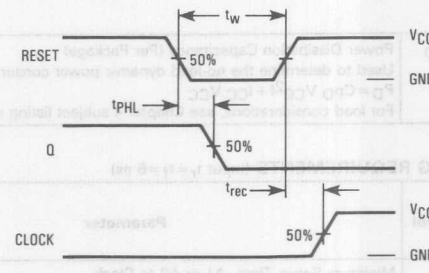


Figure 2

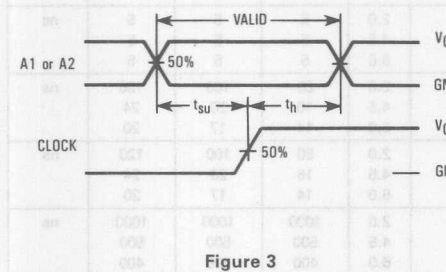
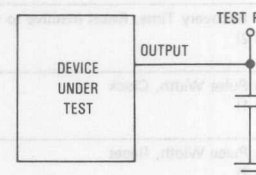


Figure 3

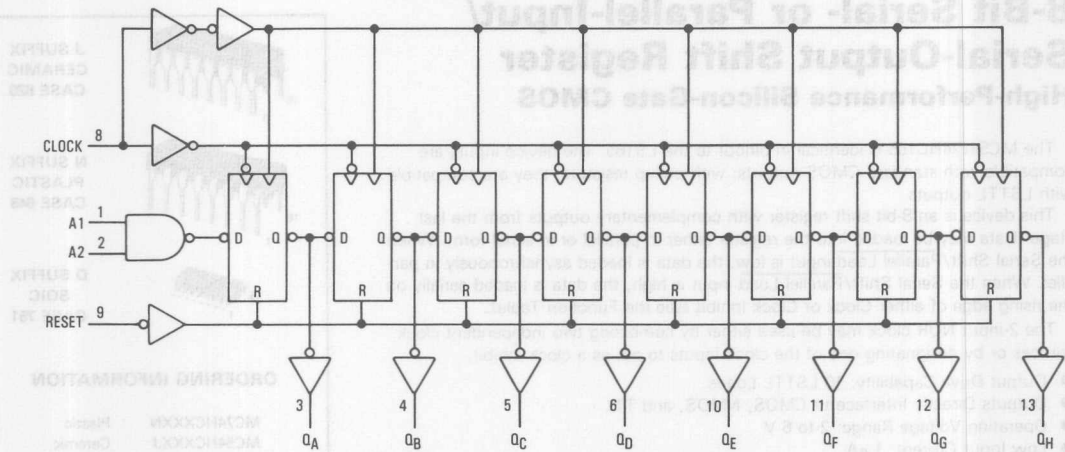


*Includes all probe and jig capacitance.

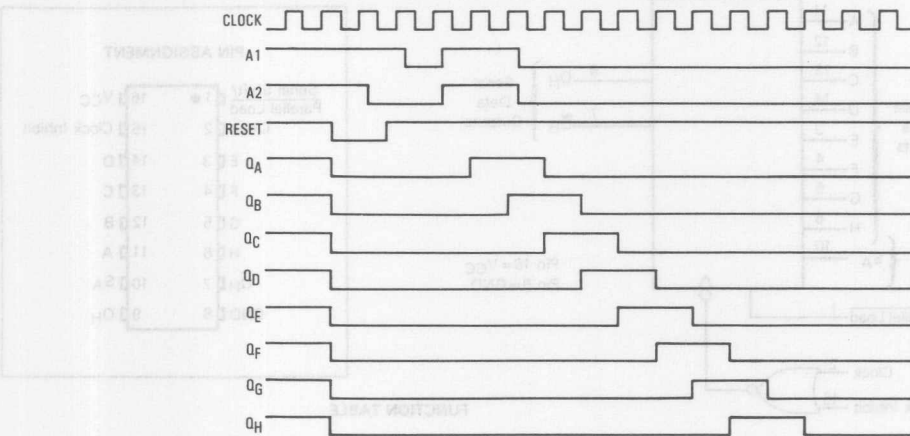
Figure 4. Test Circuit

MC54/74HC164

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



Operation	Initial State	Q _A	Q _B	Q _C	Q _D	Q _E	Q _F	Q _G	Q _H
Asynchronous Reset (Active Low)	X	X	X	X	X	X	X	X	X
Serial Shift via Clock	X	X	X	X	X	X	X	X	X
Serial Shift via Clock (Active Low)	X	X	X	X	X	X	X	X	X
Invalid Clock	X	X	X	X	X	X	X	X	X
No Clock	X	X	X	X	X	X	X	X	X

MOTOROLA

8-Bit Serial- or Parallel-Input/ Serial-Output Shift Register

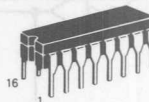
High-Performance Silicon-Gate CMOS

The MC54/74HC165 is identical in pinout to the LS165. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

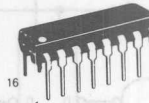
This device is an 8-bit shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Serial Shift/Parallel Load input is low, the data is loaded asynchronously in parallel. When the Serial Shift/Parallel Load input is high, the data is loaded serially on the rising edge of either Clock or Clock Inhibit (see the Function Table).

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.


- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 286 FETs or 71.5 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 620**



**N SUFFIX
PLASTIC
CASE 648**



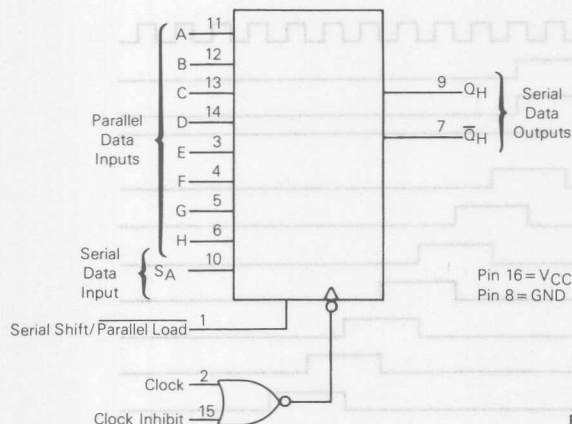
**D SUFFIX
SOIC
CASE 751**

ORDERING INFORMATION

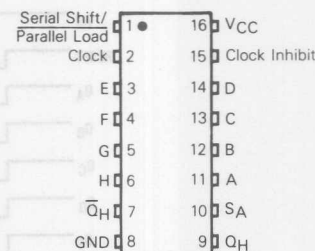
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Serial Shift/ Parallel Load	Inputs				Internal Stages		Output Q _H	Operation
	Clock	Clock Inhibit	S _A	A-H	Q _A	Q _B		
L	X	X	X	a...h	a	b	h	Asynchronous Parallel Load
H		L	L	X	L	Q _{An}	Q _{Gn}	Serial Shift via Clock
H		L	H	X	H	Q _{An}	Q _{Gn}	
H	L		L	X	L	Q _{An}	Q _{Gn}	Serial Shift via Clock Inhibit
H	L		H	X	H	Q _{An}	Q _{Gn}	
H	X	H	X	X	no change			Inhibited Clock
H	H	X	X	X	no change			No Clock
H	L	L	X	X	no change			

X = don't care

Q_{An}-Q_{Gn} = Data shifted from the preceding stage

MC54/74HC165

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC165

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 8)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock (or Clock Inhibit) to Q_H or \bar{Q}_H (Figures 1 and 8)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q_H or \bar{Q}_H (Figures 2 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input H to Q_H or \bar{Q}_H (Figures 3 and 8)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		85	pF

5

Symbol	Parameter	Test Conditions	Guaranteed Limit		
			25°C to -55°C	≤85°C	≤125°C
V_{IH}	Minimum High-Level Input Voltage	$V_{IH} = 0.1 V$ to $V_{CC} - 0.1 V$ $I_{IH} \leq 50 \mu A$	0.0 0.0 0.0	0.0 0.0 0.0	0.0 0.0 0.0
V_{IL}	Maximum Low-Level Input Voltage	$V_{IL} = 0.1 V$ to $V_{CC} - 0.1 V$ $I_{IL} \leq 50 \mu A$	0.0 0.0 0.0	0.0 0.0 0.0	0.0 0.0 0.0
V_{OH}	Minimum High-Level Output Voltage	$V_{OH} = V_{IH}$ or V_{IL} $I_{OH} \leq 50 \mu A$	0.0 0.0 0.0	0.0 0.0 0.0	0.0 0.0 0.0
V_{OL}	Maximum Low-Level Output Voltage	$V_{OL} = V_{IH}$ or V_{IL} $I_{OL} \leq 50 \mu A$	0.0 0.0 0.0	0.0 0.0 0.0	0.0 0.0 0.0
I_{IH}	Maximum Input Leakage Current	$V_{IH} = V_{CC}$ or V_{IL} $I_{IH} \leq 50 \mu A$	0.0 0.0 0.0	0.0 0.0 0.0	0.0 0.0 0.0
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{CC} = V_{CC}$ or V_{IL} $I_{CC} \leq 50 \mu A$	0.0 0.0 0.0	0.0 0.0 0.0	0.0 0.0 0.0

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC165

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Parallel Data Inputs to Serial Shift/Parallel Load (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Input S_A to Clock (or Clock Inhibit) (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Clock (or Clock Inhibit) (Figure 6)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Clock to Clock Inhibit (Figure 7)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Serial Shift/Parallel Load to Parallel Data Inputs (Figure 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Input S_A (Figure 5)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_h	Minimum Hold Time, Clock (or Clock Inhibit) to Serial Shift/Parallel Load (Figure 6)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Clock to Clock Inhibit (Figure 7)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_w	Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

5

PIN DESCRIPTIONS

INPUTS

A, B, C, D, E, F, G, H (PINS 11, 12, 13, 14, 3, 4, 5, 6) — Parallel Data inputs. Data on these inputs are asynchronously entered in parallel into the internal flip-flops when the Serial Shift/Parallel Load input is low.

S_A (PIN 10) — Serial Data input. When the Serial Shift/Parallel Load input is high, data on this pin is serially entered into the first stage of the shift register with the rising edge of the Clock.

CONTROL INPUTS

SERIAL SHIFT/PARALLEL LOAD (PIN 1) — Data-entry control input. When a high level is applied to this pin, data at the Serial Data input (S_A) are shifted into the register with the rising edge of the Clock. When a low level is applied to

this pin, data at the Parallel Data inputs are asynchronously loaded into each of the eight internal stages.

CLOCK, CLOCK INHIBIT (PINS 2, 15) — Clock inputs. These two clock inputs function identically. Either may be used as an active-high clock inhibit. However, to avoid double clocking, the inhibit input should go high only while the clock input is high.

The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

OUTPUTS

Q_H, \bar{Q}_H (PINS 9, 7) — Complementary Shift Register outputs. These pins are the noninverted and inverted outputs of the eighth stage of the shift register.

FIGURE 1 — SERIAL-SHIFT MODE

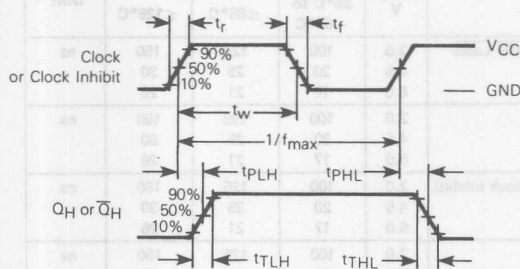


FIGURE 2 — PARALLEL-LOAD MODE

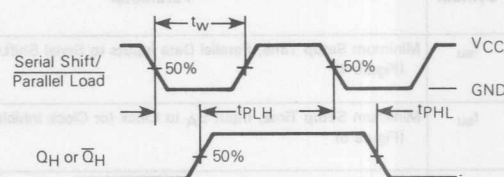


FIGURE 3 — PARALLEL-LOAD MODE

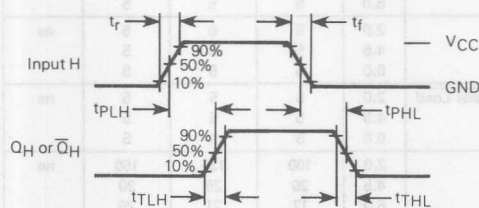


FIGURE 4 — PARALLEL-LOAD MODE

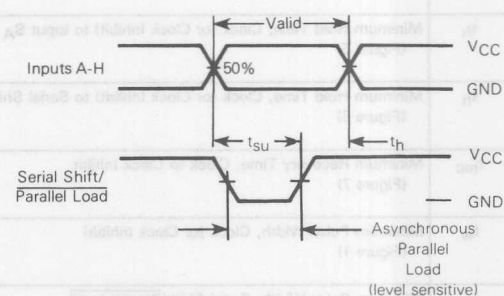


FIGURE 5 — SERIAL-SHIFT MODE

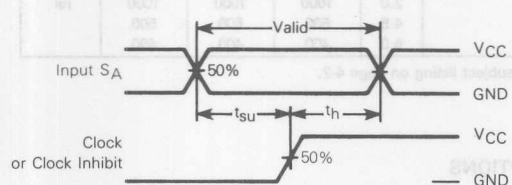


FIGURE 6 — SERIAL-SHIFT MODE

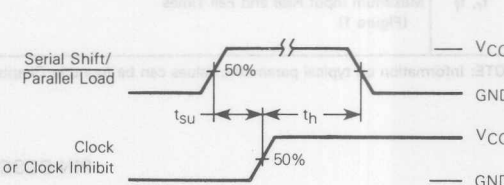


FIGURE 7 — SERIAL-SHIFT, CLOCK-INHIBIT MODE

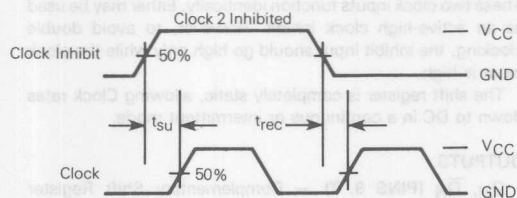
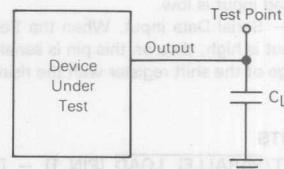


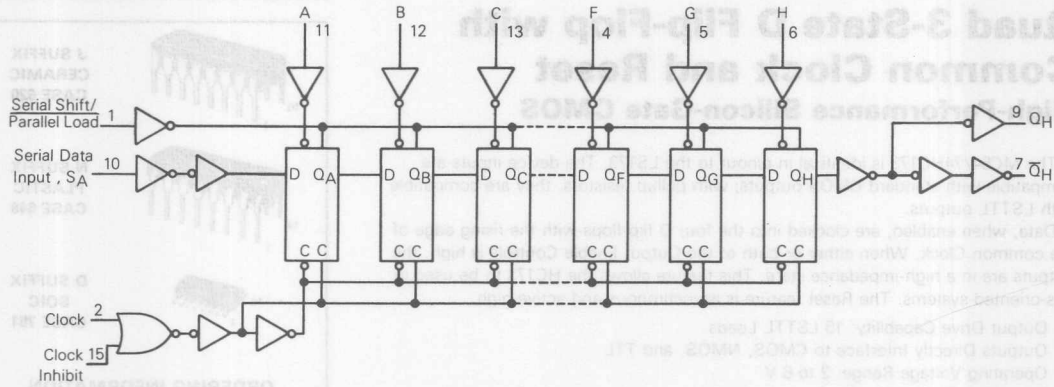
FIGURE 8 — TEST CIRCUIT



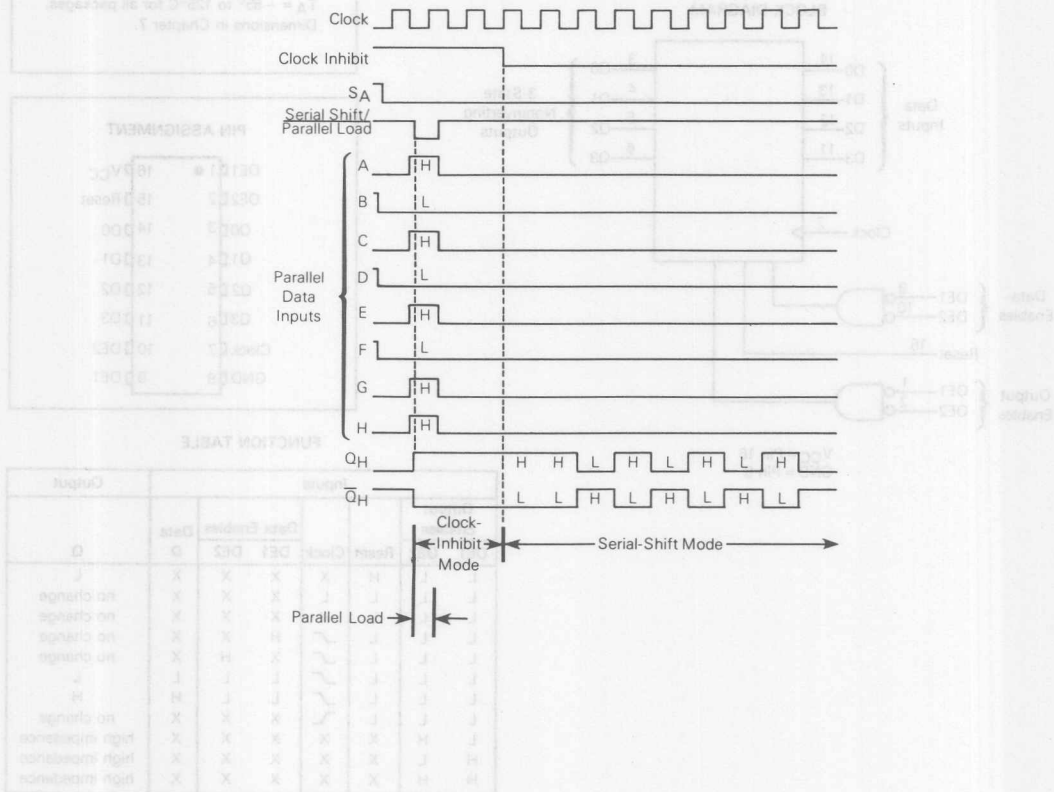
*Includes all probe and jig capacitance.

MC54/74HC165

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



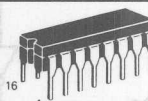
MC54/74HC173

Quad 3-State D Flip-Flop with Common Clock and Reset High-Performance Silicon-Gate CMOS

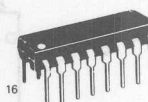
The MC54/74HC173 is identical in pinout to the LS173. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data, when enabled, are clocked into the four D flip-flops with the rising edge of the common Clock. When either or both of the Output Enable Controls is high, the outputs are in a high-impedance state. This feature allows the HC173 to be used in bus-oriented systems. The Reset feature is asynchronous and active-high.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: $1 \mu\text{A}$
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 208 FETs or 52 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 620**



**N SUFFIX
PLASTIC
CASE 648**



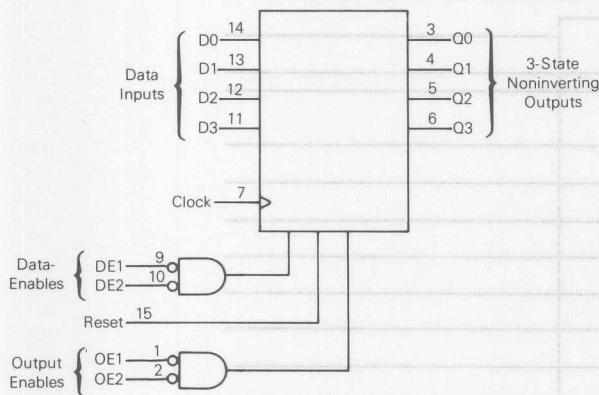
**D SUFFIX
SOIC
CASE 751**

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

BLOCK DIAGRAM



V_{CC} = Pin 16
 GND = Pin 8

PIN ASSIGNMENT

OE1	1	16	V_{CC}
OE2	2	15	Reset
Q0	3	14	D0
Q1	4	13	D1
Q2	5	12	D2
Q3	6	11	D3
Clock	7	10	DE2
GND	8	9	DE1

FUNCTION TABLE

Output Enables		Inputs					Output
OE1	OE2	Reset	Clock	Data Enables		Data D	Q
L	L	H	X	X	X	X	L
L	L	L	L	X	X	X	no change
L	L	L	H	X	X	X	no change
L	L	L	\nearrow	H	X	X	no change
L	L	L	\nearrow	X	H	X	no change
L	L	L	\nearrow	L	L	L	L
L	L	L	\nearrow	L	L	H	H
L	L	L	\searrow	X	X	X	no change
L	H	X	X	X	X	X	high impedance
H	L	X	X	X	X	X	high impedance
H	H	X	X	X	X	X	high impedance

MC54/74HC173

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	– 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PLZ} t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input D or DE to Clock (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Clock to Input D or DE (Figure 4)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	90 18 15	115 23 20	135 27 23	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC173

PIN DESCRIPTIONS

INPUTS

D0, D1, D2, D3 (PINS 14, 13, 12, 11) — 4-bit data inputs. Data on these pins, when enabled by the Data-Enable Controls, are entered into the flip-flops on the rising edge of the clock.

CLOCK (PIN 7) — Clock input.

OUTPUTS

Q0, Q1, Q2, Q3 (PINS 3, 4, 5, 6) — 3-state register outputs. During normal operation of the device, the outputs of the D flip-flops appear at these pins. During 3-state operation, these outputs assume a high-impedance state.

CONTROL INPUTS

RESET (PIN 15) — Asynchronous reset input. A high level

on this pin resets all flip-flops and forces the Q outputs low, if they are not already in high-impedance state.

DE1, DE2 (Pins 9, 10) — Active-low Data Enable Control inputs. When both Data Enable Controls are low, data at the D inputs are loaded into the flip-flops with the rising edge of the Clock input. When either or both of these controls are high, there is no change in the state of the flip-flops, regardless of any changes at the D or Clock inputs.

OE1, OE2 (Pins 1, 2) — Output Enable Control inputs. When either or both of the Output Enable Controls are high, the Q outputs of the device are in the high-impedance state. When both controls are low, the device outputs display the data in the flip-flops.

SWITCHING WAVEFORMS

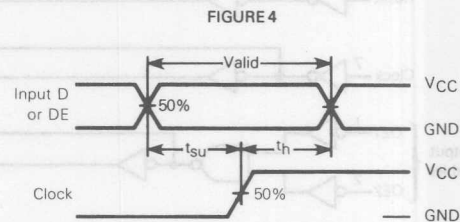
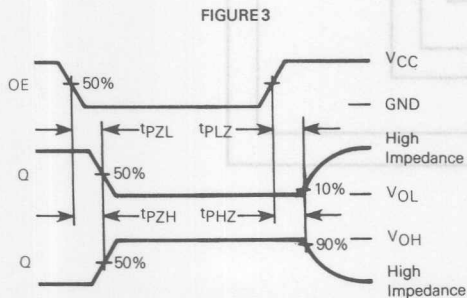
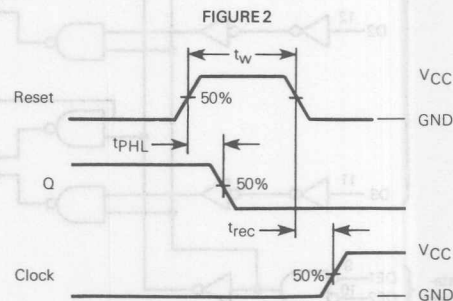
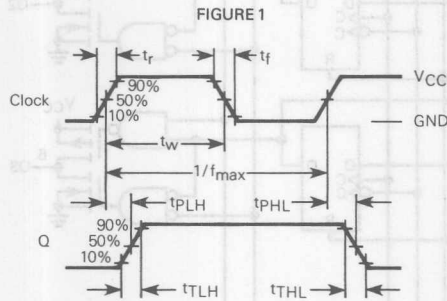
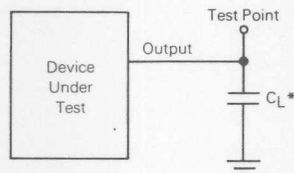
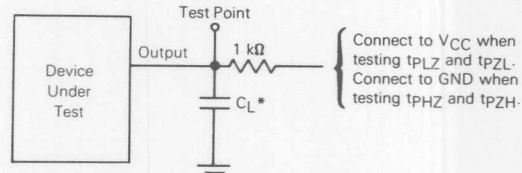


FIGURE 5 — TEST CIRCUIT



* Includes all probe and jig capacitance.

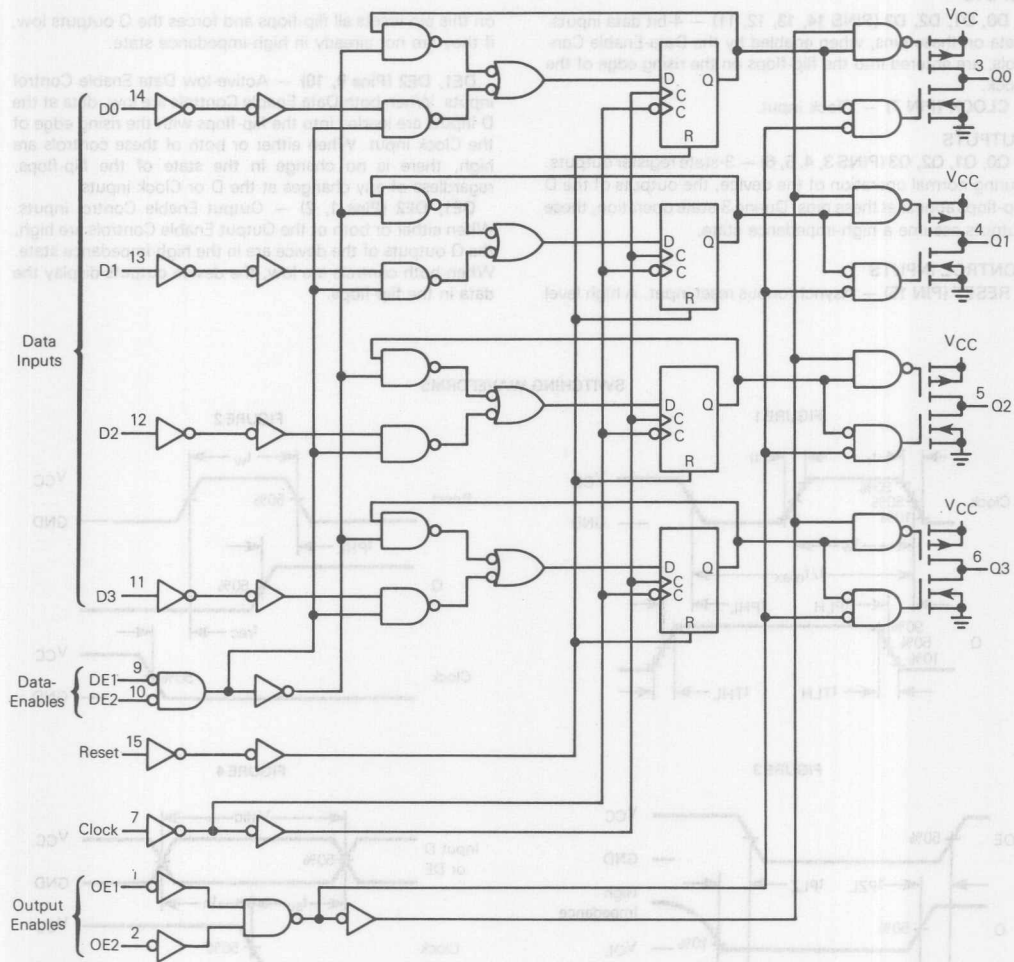
FIGURE 6 — TEST CIRCUIT



* Includes all probe and jig capacitance.

MC54/74HC173

LOGIC DETAIL



MC54/74HC174

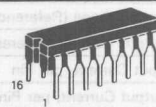
Hex D Flip-Flop with Common Clock and Reset

High-Performance Silicon-Gate CMOS

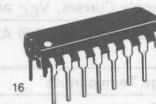
The MC54/74HC174 is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

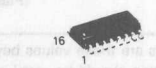
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 162 FETs or 40.5 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 620**



**N SUFFIX
PLASTIC
CASE 648**



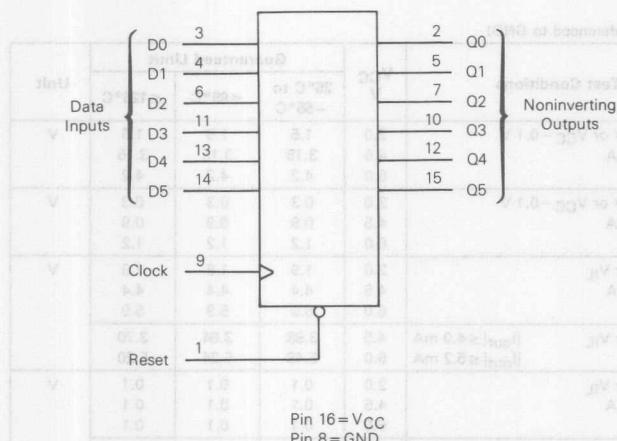
**D SUFFIX
SOIC
CASE 751**

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Reset	1	16	V_{CC}
Q0	2	15	Q5
D0	3	14	D5
D1	4	13	D4
Q1	5	12	Q4
D2	6	11	D3
Q2	7	10	Q3
GND	8	9	Clock

FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

5

MC54/74HC174

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	
		35	pF

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC174

SWITCHING WAVEFORMS

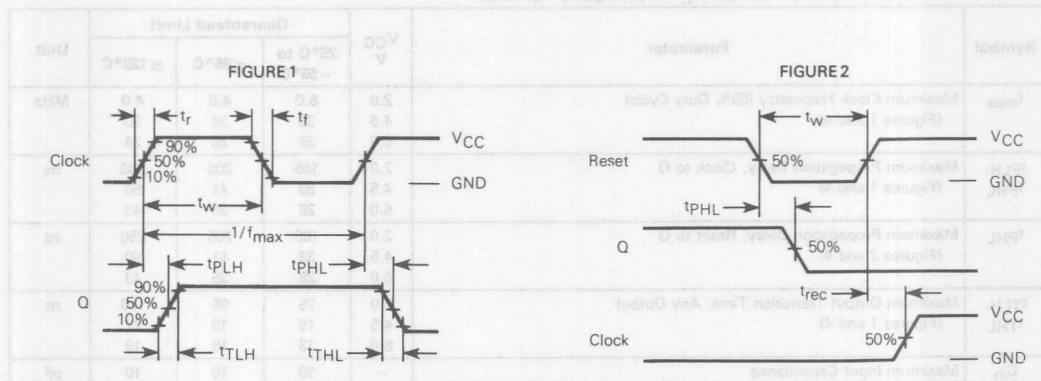


FIGURE 3

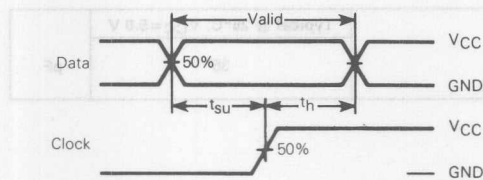
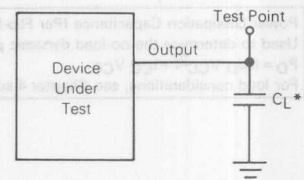
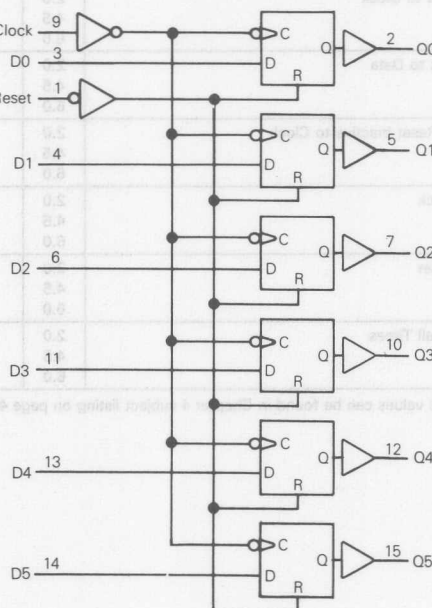


FIGURE 4 — TEST CIRCUIT



* Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM



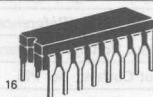
MC54/74HC175

Quad D Flip-Flop with Common Clock and Reset High-Performance Silicon-Gate CMOS

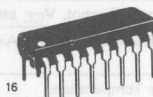
The MC54/74HC175 is identical in pinout to the LS175. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of four D flip-flops with common Reset and Clock inputs, and separate D inputs. Reset (active-low) is asynchronous and occurs when a low level is applied to the Reset input. Information at a D input is transferred to the corresponding Q output on the next positive-going edge of the Clock input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 166 FETs or 41.5 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 620**



**N SUFFIX
PLASTIC
CASE 648**



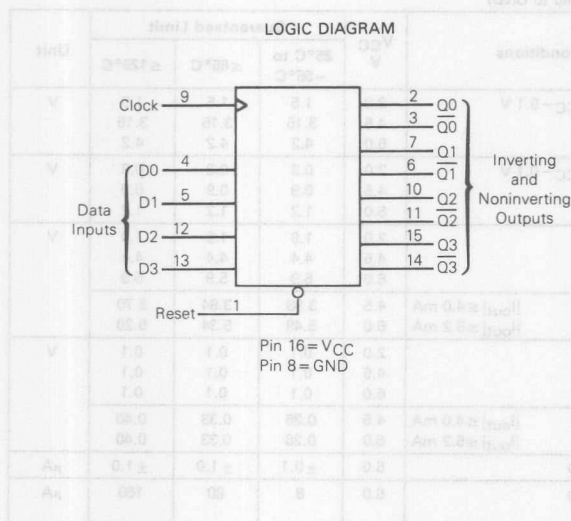
**D SUFFIX
SOIC
CASE 751**

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

Unit	Max	Min
V	5.0	2.0
V	5.0	0
$^\circ\text{C}$	125	-55
ns	100	0



PIN ASSIGNMENT

Reset	1	16	VCC
Q0	2	15	Q3
Q0	3	14	Q3
D0	4	13	D3
D1	5	12	D2
Q1	6	11	Q2
Q1	7	10	Q2
GND	8	9	Clock

FUNCTION TABLE

Inputs			Outputs	
Reset	Clock	D	Q	\bar{Q}
L	X	X	L	H
H		H	H	L
H		L	L	H
H	L	X	no change	

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

5

MC54/74HC175

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q or \bar{Q} (Figures 2 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

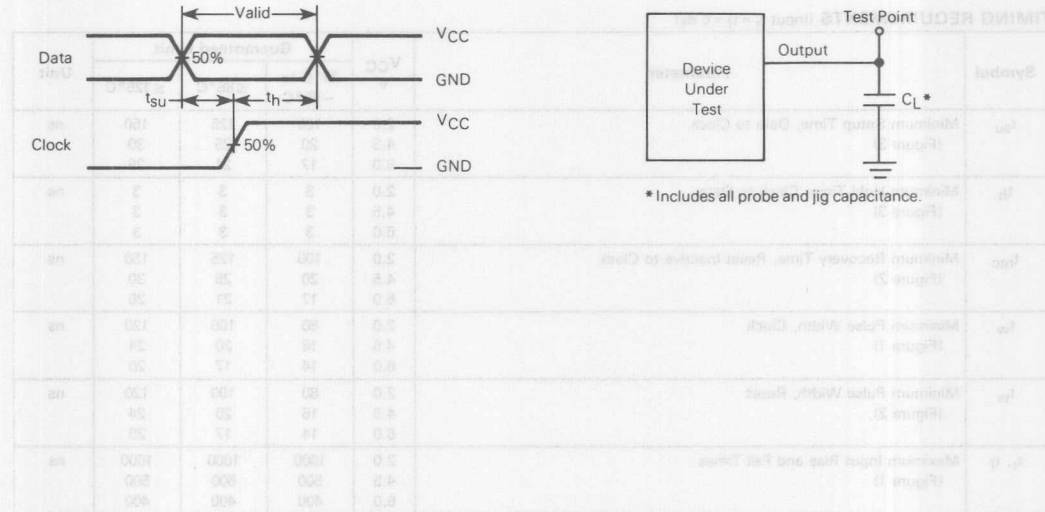
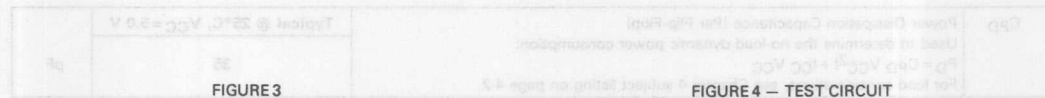
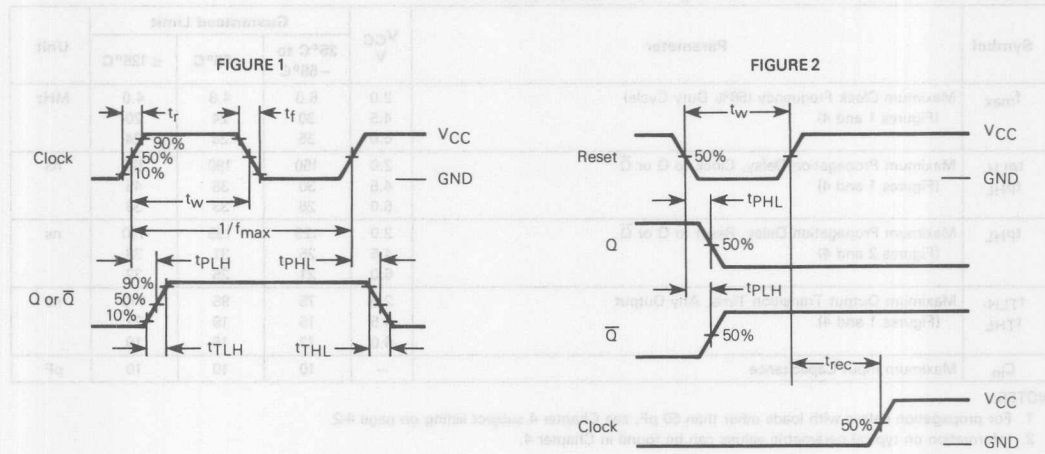
TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

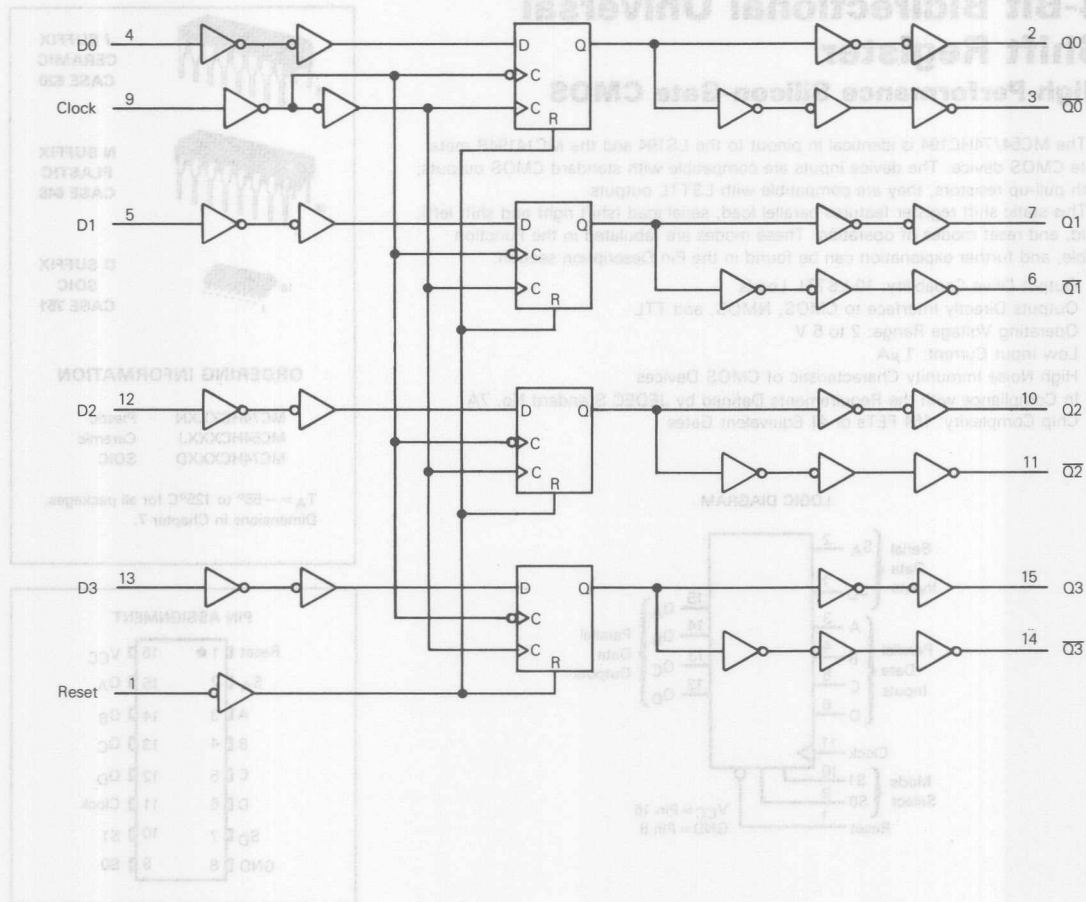
NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC175

SWITCHING WAVEFORMS



EXPANDED LOGIC DIAGRAM



FUNCTION TABLE

Mode Select	Shift Data	Parallel Data	Outputs				Operating Mode
			A	B	C	D	
0	0	0	X	X	X	X	Hold
0	0	1	X	X	X	X	Hold
0	1	0	X	X	X	X	Shift Left
0	1	1	X	X	X	X	Shift Right
1	0	0	X	X	X	X	Shift Left
1	0	1	X	X	X	X	Shift Right
1	1	0	X	X	X	X	Shift Left
1	1	1	X	X	X	X	Shift Right

H = high-level steady state
L = low-level steady state
X = don't care
— = transition from low to high level
Q₀, Q₁, Q₂, Q₃ = the level of Q₀, Q₁, Q₂, Q₃ respectively, before the next
clock transition of the clock
no change = no change

4-Bit Bidirectional Universal Shift Register

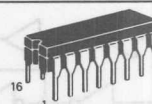
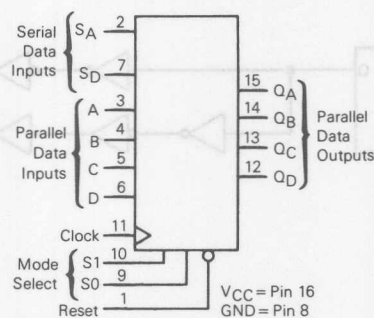
High-Performance Silicon-Gate CMOS

The MC54/74HC194 is identical in pinout to the LS194 and the MC14194B metal gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

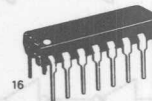
This static shift register features parallel load, serial load (shift right and shift left), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 164 FETs or 41 Equivalent Gates

LOGIC DIAGRAM



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

Reset	1	16	VCC
SA	2	15	QA
A	3	14	QB
B	4	13	QC
C	5	12	QD
D	6	11	Clock
SD	7	10	S1
GND	8	9	S0

FUNCTION TABLE

Reset	Inputs				Outputs				Operating Mode
	Mode Select	Serial Data		Parallel Data	QA	QB	QC	QD	
	S1 S0	SD	SA	A B C D					
L	X X	X	X	X X X X	L	L	L	L	Reset
H	H H	X	X	a b c d	a	b	c	d	Parallel Load
H	L H	X	H	X X X X	H	QA _n	QB _n	QC _n	Shift Right
H	L H	X	L	X X X X	L	QA _n	QB _n	QC _n	Shift Right
H	H L	X	H	X X X X	QB _n	QC _n	QD _n	H	Shift Left
H	H L	X	L	X X X X	QB _n	QC _n	QD _n	L	Shift Left
H	L L	X	X	X X X X	no change				Hold
H	X X	L	X	X X X X	no change				Hold
H	X X	H	X	X X X X	no change				Hold

H = high level (steady state)
L = low level (steady state)
X = don't care
/ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
QA_n, QB_n, QC_n, QD_n = the level of QA, QB, QC, or QD, respectively, before the most-recent / transition of the clock.

MC54/74HC194

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC194

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	
		90	pF

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Parallel Data Inputs to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, S1 to S0 to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, SA or SD to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Clock to any Input (except Reset) (Figure 3)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC194

PIN DESCRIPTIONS

DATA INPUTS

- A, B, C, D (PINS 3, 4, 5, 6)** — Parallel data inputs.
S_A (PIN 2) — Serial-data input when using shift-right mode.
S_D (PIN 7) — Serial-data input when using shift-left mode.

OUTPUTS

- Q_A, Q_B, Q_C, Q_D (PINS 15, 14, 13, 12)** — Parallel data outputs.

CONTROL INPUTS

- CLOCK (PIN 11)** — Clock Input. The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

- RESET (PIN 1)** — A low level applied to this pin resets all stages and forces all outputs low.

- S₀, S₁ (PINS 9, 10)** — Mode-select inputs. These inputs control the mode of operation as described in the function table and below.

- Parallel Load Mode (S₁=H, S₀=H)** — Data is loaded into the device with a positive transition of the Clock input.

- Shift Right Mode (S₁=L, S₀=H)** — With a positive transition of the Clock input, each bit is shifted right (in the direction Q_A toward Q_D) one stage and data on the S_A Serial Data Input is shifted into stage A.

- Shift Left Mode (S₁=H, S₀=L)** — With a positive transition of the Clock input, each bit is shifted left (in the direction Q_D toward Q_A) one stage and data on the S_D Serial Data Input is shifted into stage D.

- Hold Mode (S₁=L, S₀=L)** — Outputs are held.

SWITCHING WAVEFORMS

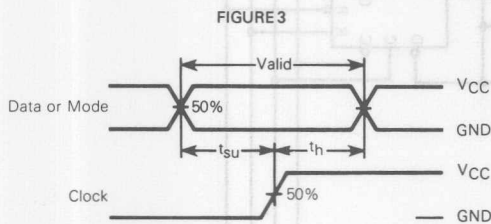
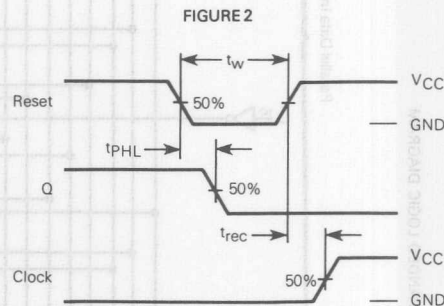
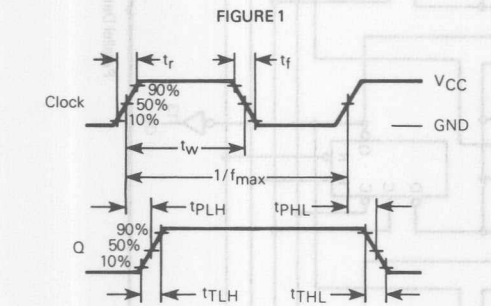
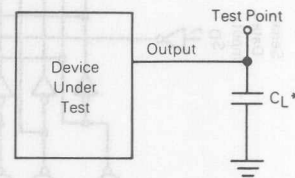


FIGURE 4 — TEST CIRCUIT

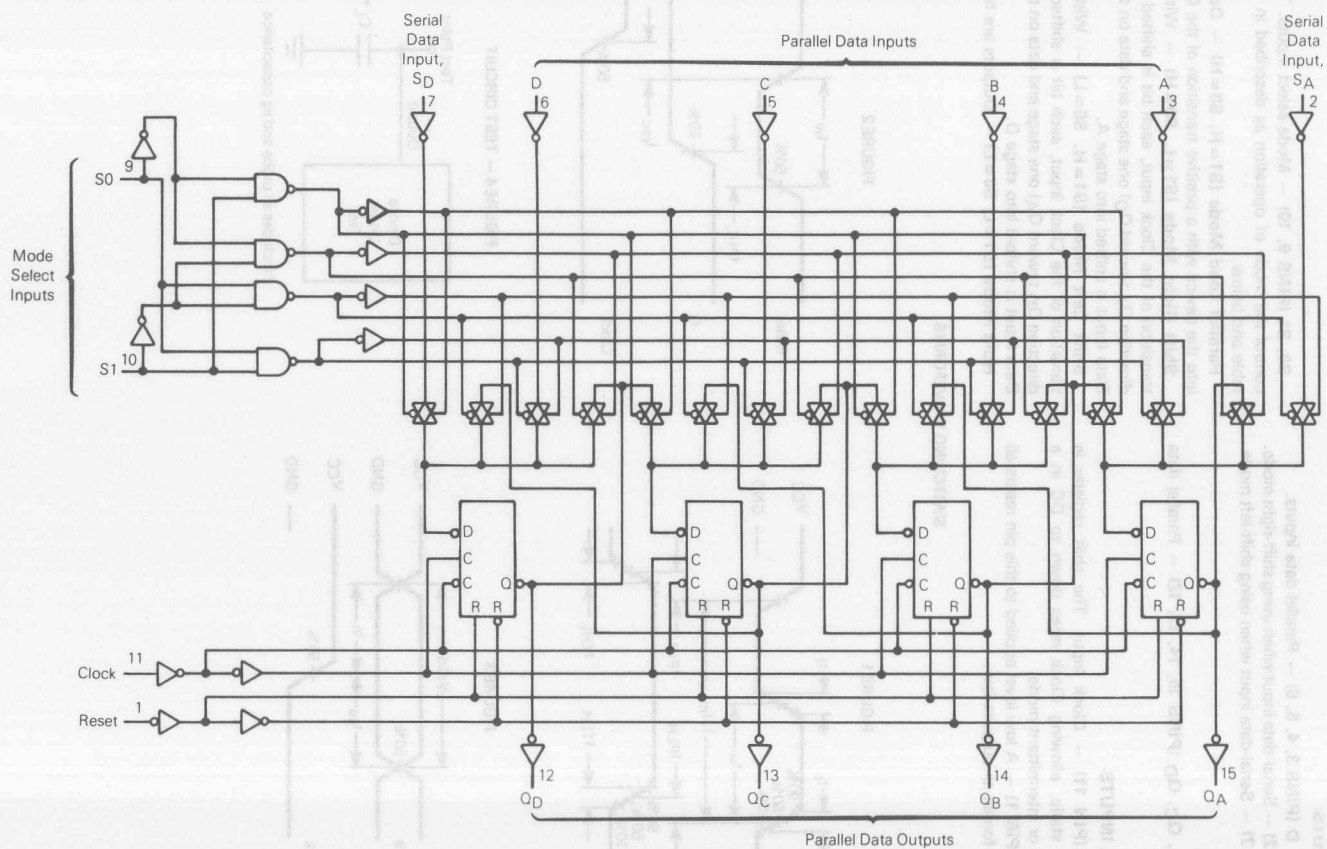


* Includes all probe and jig capacitance.

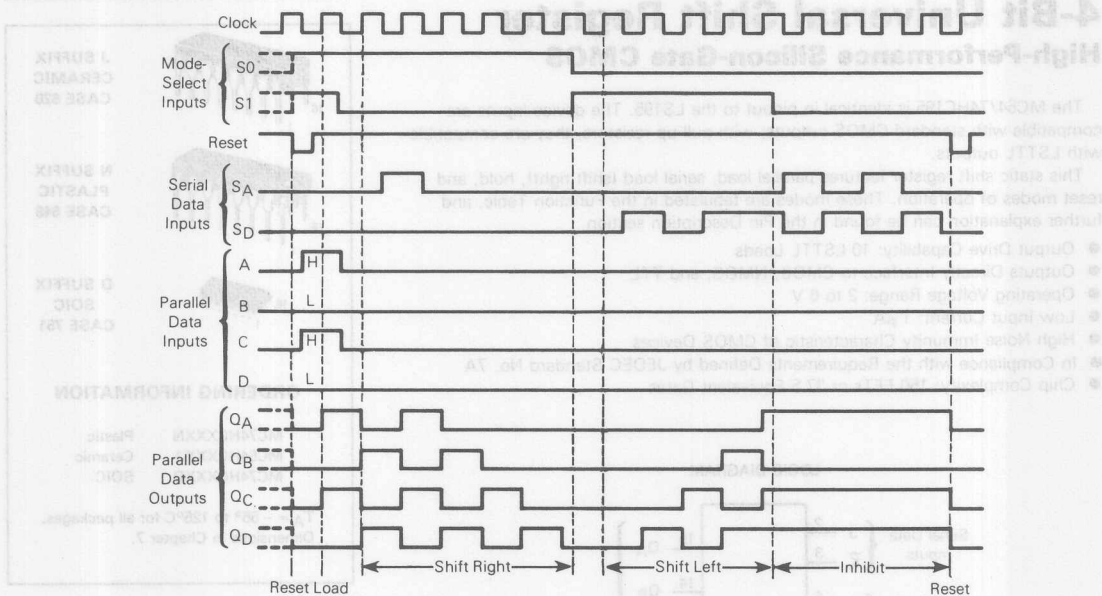
MOTOROLA HIGH-SPEED CMOS LOGIC DATA

5-206

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



FUNCTION TABLE

Operating Mode	Serial Load	Clock	Serial Inputs				Parallel Inputs				Outputs			
			A	B	C	D	QA	QB	QC	QD	QA	QB	QC	QD
Shift Right	0	1	X	X	X	X	X	X	X	X	0	0	0	0
Shift Left	0	1	X	X	X	X	X	X	X	X	0	0	0	0
Parallel Load	1	1	X	X	X	X	X	X	X	X	A	B	C	D
Inhibit	1	0	X	X	X	X	X	X	X	X	0	0	0	0
Shift Right	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Shift Left	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Parallel Load	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Inhibit	1	0	0	0	0	0	0	0	0	0	0	0	0	0

0 = low level (steady state)
1 = high level (steady state)
X = don't care
Transition from low to high level
A, B, C, D = the level of steady-state
input at inputs A, B, C, or D,
respectively.

QA = the level of QA before the
indicated steady-state input condi-
tion was established
QA, QB, QC = the level of QA,
QB, or QC, respectively, before the
most recent transition of the
clock

MC54/74HC195

4-Bit Universal Shift Register High-Performance Silicon-Gate CMOS

The MC54/74HC195 is identical in pinout to the LS195. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This static shift register features parallel load, serial load (shift right), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 150 FETs or 37.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



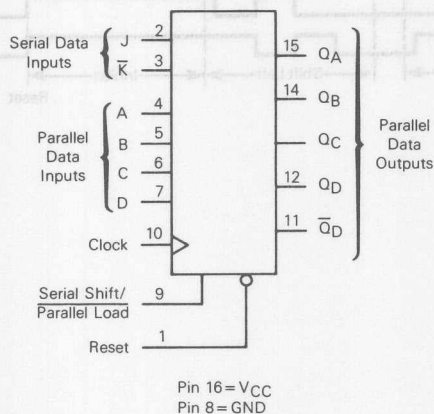
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

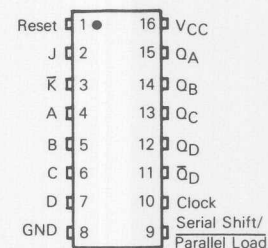
MC74HCXXN Plastic
MC54HCXXJ Ceramic
MC74HCXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs						Operating Mode
Reset	Shift/Load	Clock	Serial J K	Parallel A B C D	QA	QB	QC	QD	QD-bar	
L	X	X	X X	X X X X	L	L	L	L	H	Reset
H	L	\nearrow	X X	a b c d	a	b	c	d	d-bar	Parallel Load
H	H	L	X X	X X X X	no change					Hold
H	H	\nearrow	L	H X X X X	QA0	QBn	QCn	QDn	QDn-bar	Retain First Stage
H	H	\nearrow	L	L X X X X	L	QA0	QBn	QCn	QDn-bar	Reset First Stage
H	H	\nearrow	H	H X X X X	H	QA0	QBn	QCn	QDn-bar	Set First Stage
H	H	\nearrow	H	L X X X X	QA0	QA0	QBn	QCn	QDn-bar	Toggle First Stage

H = high level (steady state)
L = low level (steady state)
X = don't care
 \nearrow = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

QA0 = the level of QA before the indicated steady-state input conditions were established.
QA0, QBn, QCn = the level of QA, QB, or QC, respectively, before the most-recent \nearrow transition of the clock.

MC54/74HC195

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V	25°C to -55°C	≤85°C	≤125°C	Unit
f_{\max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to any Q or \bar{Q}_D (Figures 1 and 5)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Reset to any Q or \bar{Q}_D (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		95	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, A, B, C, D, J, or \bar{K} to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Clock (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_h	Minimum Hold Time, Clock to A, B, C, D, J, or \bar{K} (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t_h	Minimum Hold Time, Clock to Serial Shift/Parallel Load (Figure 4)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC195

PIN DESCRIPTION

DATA INPUTS

A, B, C, D (PINS 4, 5, 6, 7) — Parallel data inputs.

OUTPUTS

Q_A , Q_B , Q_C , Q_D , \bar{Q}_D (PINS 15, 14, 13, 12, 11) — Parallel data outputs.

CONTROL INPUTS

CLOCK (PIN 10) — Clock input. The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

SERIAL SHIFT/PARALLEL LOAD (PIN 9) — Shift or load control. A low level applied to this pin allows data to be loaded from the parallel inputs. Data is loaded with the positive transition of the Clock input. A high level allows data to be shifted in the manner dictated by the J and \bar{K} control inputs.

RESET (PIN 1) — A low level applied to this pin resets all stages and forces all outputs low.

J, \bar{K} (PINS 2, 3) — Shift Control. With Serial Shift/Parallel Load high, J and \bar{K} control the mode of operation, as illustrated in the Function Table.

J = L, \bar{K} = H — With a positive transition of the Clock input, each bit is shifted to the right (in the direction Q_A toward Q_D) one stage and stage A maintains its previous state.

J = H, \bar{K} = L — With a positive transition of the Clock input, each bit is shifted right (in the direction of Q_A toward Q_D) one stage and the Q_A output is inverted.

J = \bar{K} = L — With a positive transition of the Clock input, each bit is shifted right (in the direction Q_A toward Q_D) one stage and a low is loaded into stage A.

J = \bar{K} = H — With a positive transition of the Clock input, each bit is shifted right (in the direction Q_A toward Q_D) one stage and a high is loaded into stage A.

SWITCHING WAVEFORMS

FIGURE 1

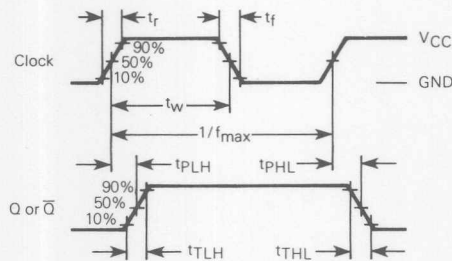


FIGURE 2

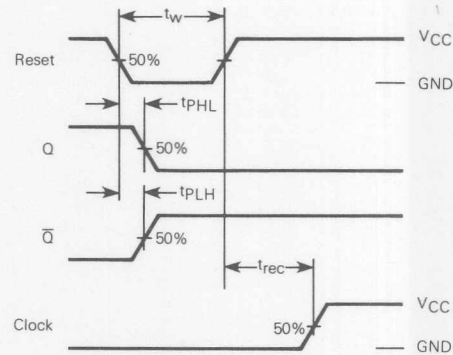


FIGURE 3

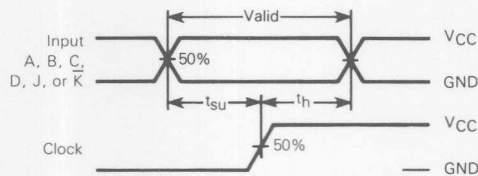


FIGURE 4

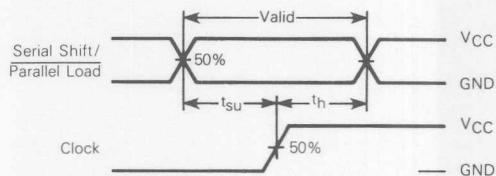
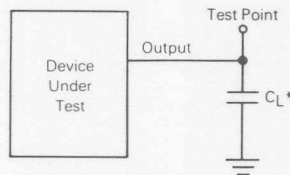


FIGURE 5 — TEST CIRCUIT



* Includes all probe and jig capacitance.

MC54/74HC195

TIMING DIAGRAM

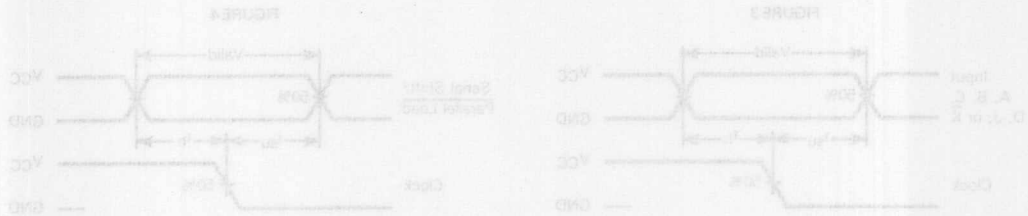
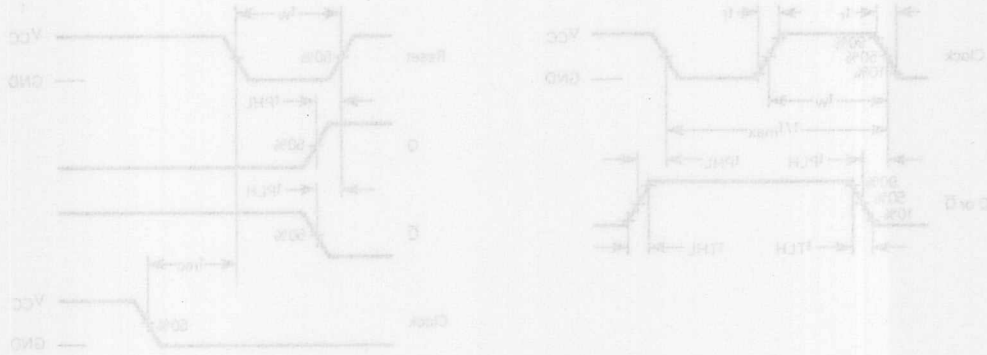
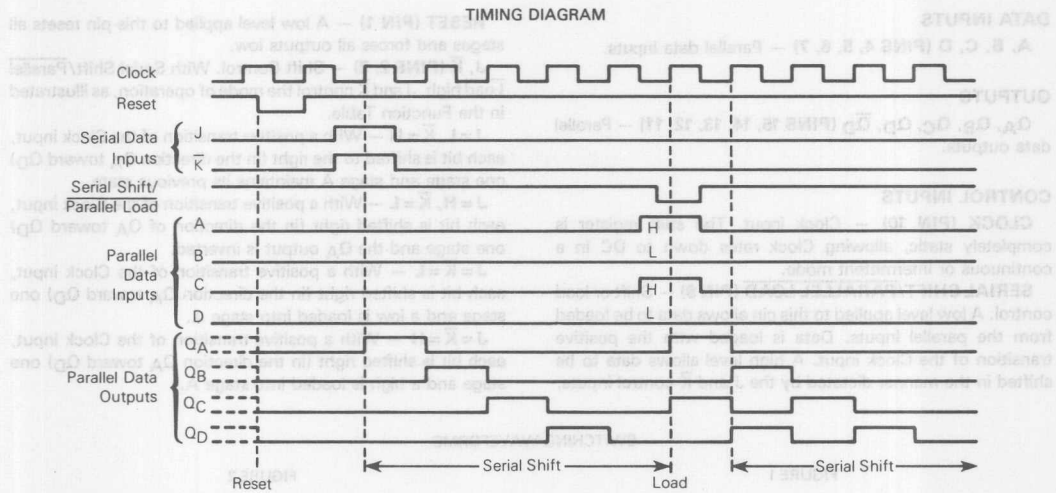
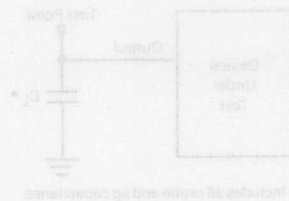
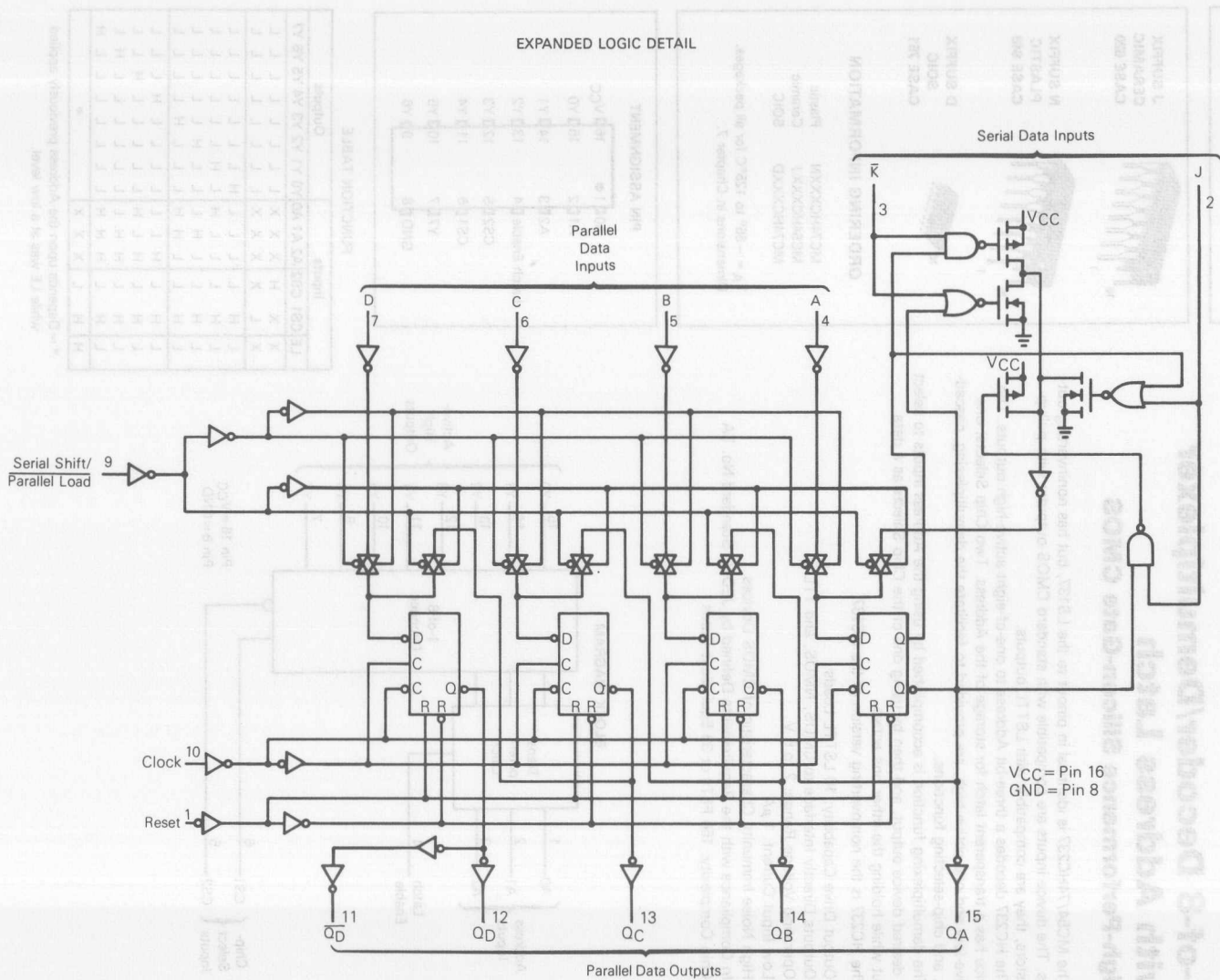


FIGURE 2 - TEST CIRCUIT



EXPANDED LOGIC DETAIL



1-of-8 Decoder/Demultiplexer with Address Latch

High-Performance Silicon-Gate CMOS

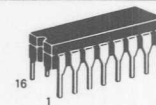
The MC54/74HC237 is identical in pinout to the LS137, but has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC237 decodes a three-bit Address to one-of-eight active-high outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active-low and one active-high, are provided to facilitate the demultiplexing, cascading, and chip-selecting functions.

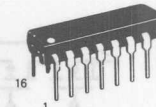
The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC237 is the noninverting version of the HC137.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 156 FETs or 39 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648

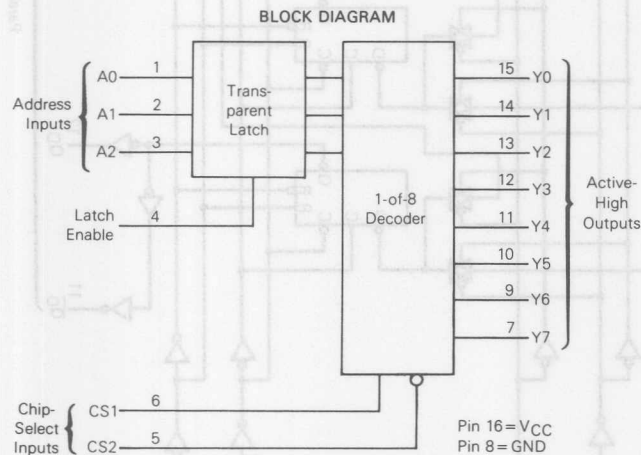


D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.



PIN ASSIGNMENT

A0	1	16	V_{CC}
A1	2	15	Y0
A2	3	14	Y1
Latch Enable	4	13	Y2
CS2	5	12	Y3
CS1	6	11	Y4
Y7	7	10	Y5
GND	8	9	Y6

FUNCTION TABLE

Inputs						Outputs							
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	*							

* = Depends upon the Address previously applied while LE was at a low level.

MC54/74HC237

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 2)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC237

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 6)	2.0	235	295	355	ns
		4.5	47	59	71	
		6.0	40	50	60	
t _{PHL}		2.0	185	230	280	
		4.5	37	46	56	
		6.0	31	39	48	
t _{PLH}	Maximum Propagation Delay, CS2 to Output Y (Figures 2 and 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t _{PHL}		2.0	145	180	220	
		4.5	29	36	44	
		6.0	25	31	38	
t _{PLH}	Maximum Propagation Delay, CS1 to Output Y (Figures 3 and 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t _{PHL}		2.0	160	200	240	
		4.5	32	40	48	
		6.0	27	34	41	
t _{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 4 and 6)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t _{PHL}		2.0	190	240	285	
		4.5	38	48	57	
		6.0	32	41	48	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		100	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input A to Latch Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Enable to Input A (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _w	Minimum Pulse Width, Latch Enable (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 2)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC237

PIN DESCRIPTIONS

ADDRESS INPUTS

A0, A1, A2 (PINS 1, 2, 3) — Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

CONTROL INPUTS

CS1, CS2 (PINS 6, 5) — Chip select inputs. For CS1 at a high level and CS2 at a low level, the chip is enabled and the outputs follow the data inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs are at a low level.

LATCH ENABLE (PIN 4) — Latch Enable input. A high level at this input latches the Address. A low level at this input allows the outputs to follow the Address (CS1=H and CS2=L).

OUTPUTS

Y0-Y7 (PINS 15, 14, 13, 12, 11, 10, 9, 7) — Active-high outputs. One of these eight outputs is selected when the chip is enabled (CS1=H and CS2=L) and the Address inputs correspond to that particular output. The selected output is at a high level while all others remain at a low level.

SWITCHING WAVEFORMS

FIGURE 1

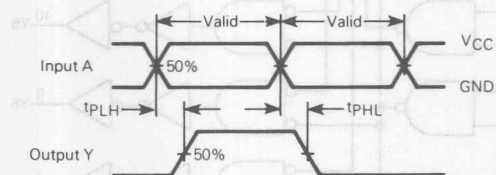


FIGURE 2

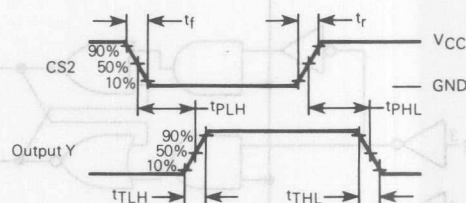


FIGURE 3

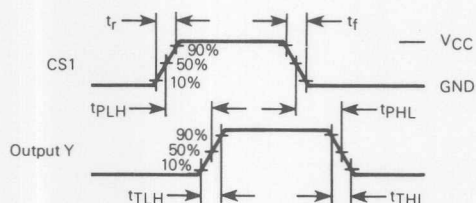


FIGURE 4

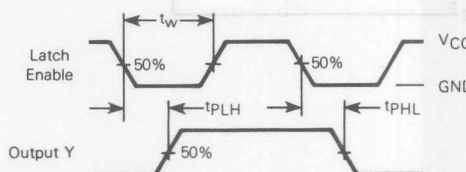


FIGURE 5

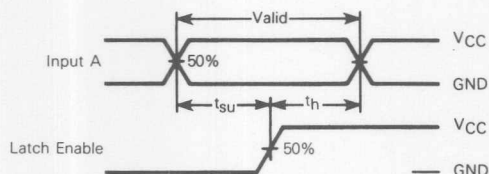
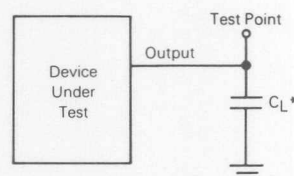
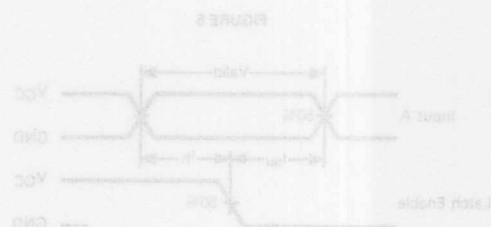
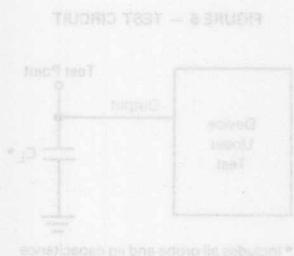
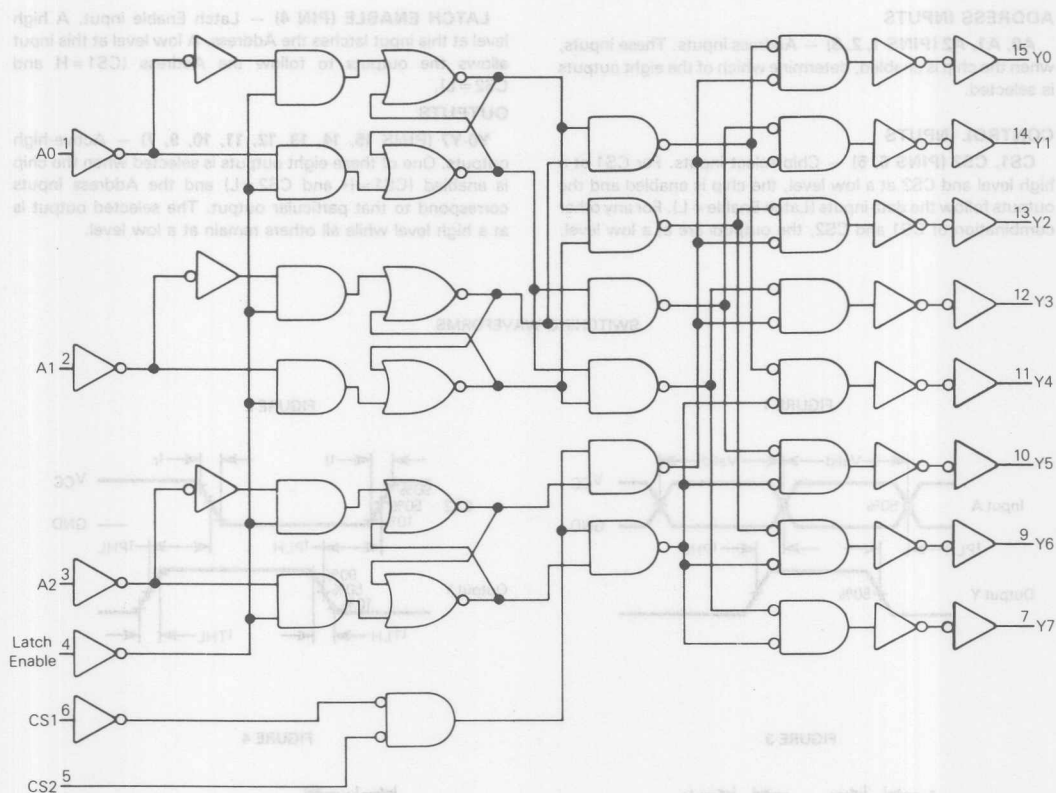


FIGURE 6 — TEST CIRCUIT



* Includes all probe and jig capacitance.



MC54/74HC240

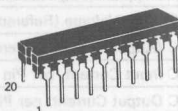
Octal 3-State Inverting Buffer/ Line Driver/Line Receiver High-Performance Silicon-Gate CMOS

The MC54/74HC240 is identical in pinout to the LS240. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

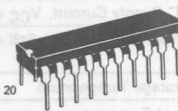
This octal inverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

The HC240 is similar in function to the HC241 and HC244.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 120 FETs or 30 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



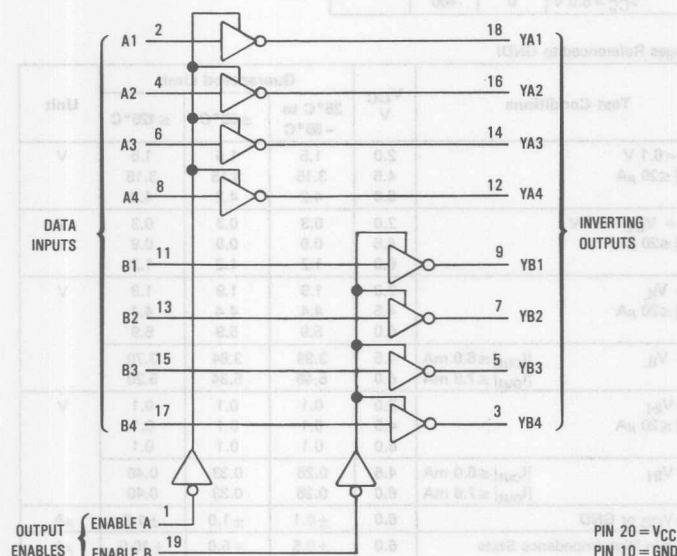
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

ENABLE A	1	20	V_{CC}
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	H
L	H	L
H	X	Z

Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC240

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		32	

SWITCHING WAVEFORMS

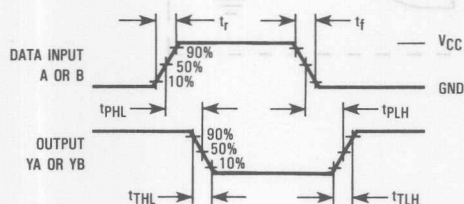


Figure 1

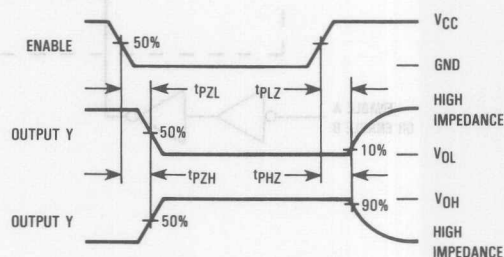
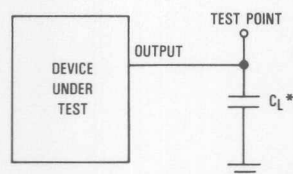
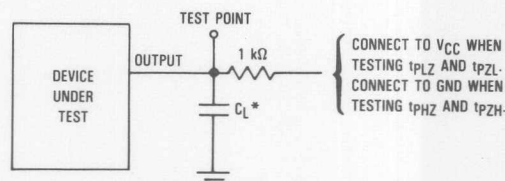


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4 (Pins 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

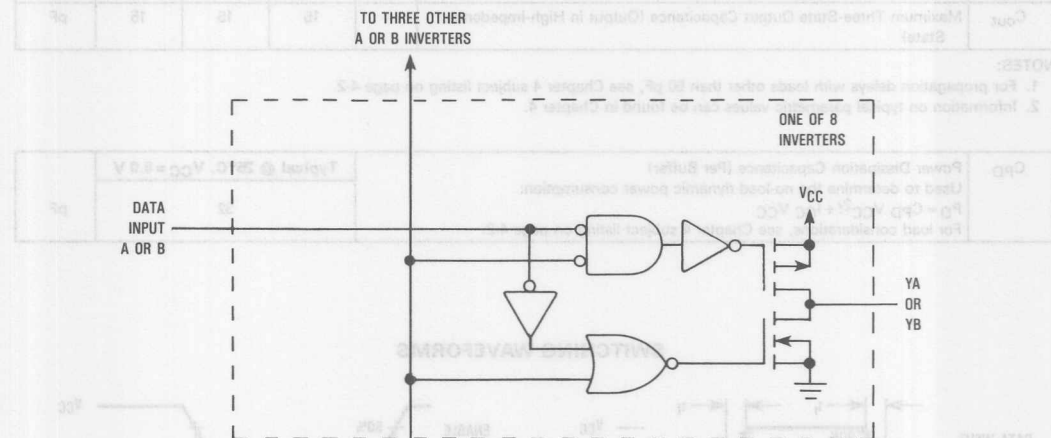
Enable A, Enable B (Pins 1, 19) — Output enables (active-low). When a low level is applied to these pins, the outputs

are enabled and the devices function as inverters. When a high level is applied, the outputs assume the high-impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (Pins 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either inverting outputs or high-impedance outputs.

LOGIC DETAIL



5



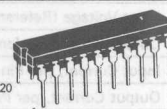
MC54/74HCT240

Octal 3-State Inverting Buffer/ Line Driver/Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

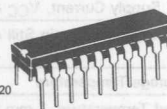
The HCT240 is identical in pinout to the LS240. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT240 is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

The HCT240 is the inverting version of the HCT244. See also HCT241.

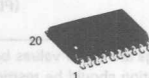
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 110 FETs or 27.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



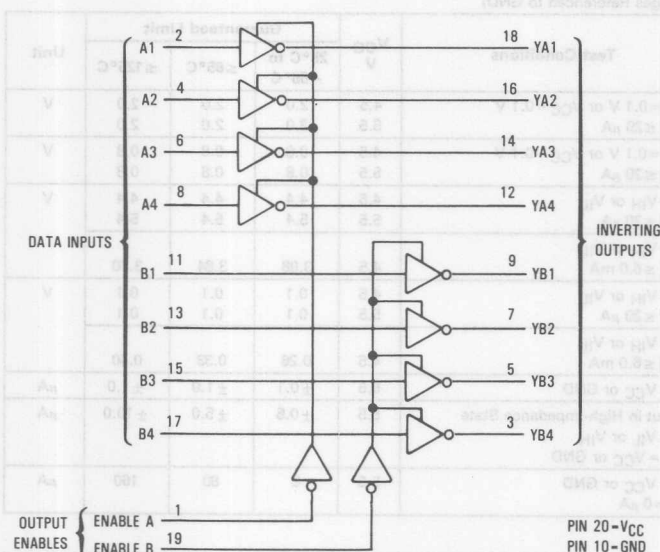
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

ENABLE A	1	20	VCC
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	H
L	H	L
H	X	Z

Z = High Impedance
X = Don't Care

5

MC54/74HCT240

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	$\geq -55^\circ\text{C}$ 2.9	25°C to 125°C 2.4		mA

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT240

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	22	28	33	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	pF
		55	

SWITCHING WAVEFORMS

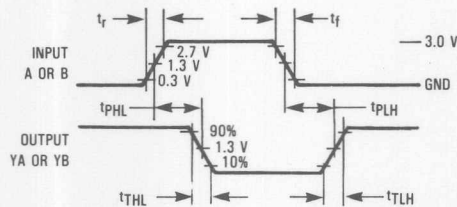


Figure 1

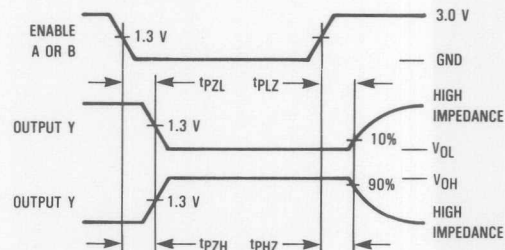
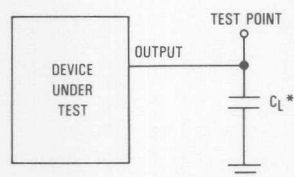
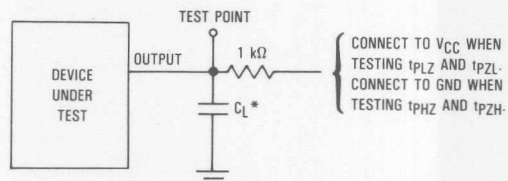


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

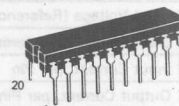
The MC54/74HC241 is identical in pinout to the LS241. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverted outputs and two output enables. Enable A is active-low and Enable B is active-high.

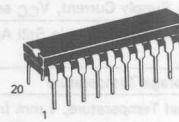
The HC241 is similar in function to the HC244 and HC240.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

MC54/74HC241



**J SUFFIX
CERAMIC
CASE 732**



**N SUFFIX
PLASTIC
CASE 738**



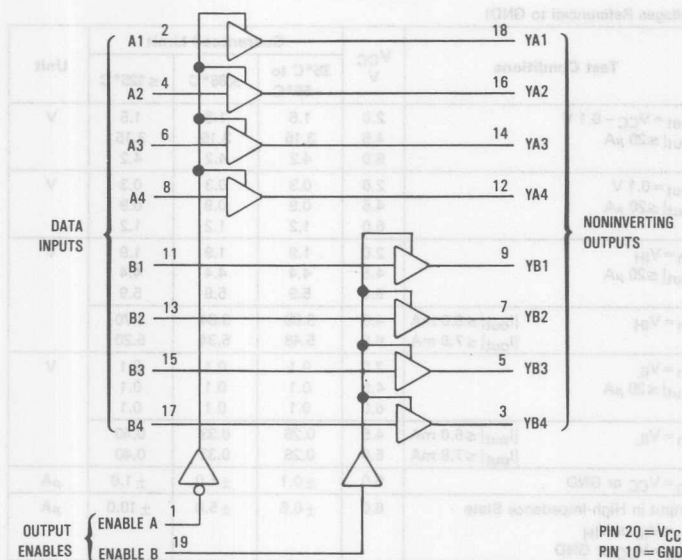
**DW SUFFIX
SOIC
CASE 751D**

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

ENABLE A	1	20	VCC
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs			Output		
Enable A	A	YA	Enable B	B	YB
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

Z = high impedance

MC54/74HC241

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or } GND$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC241

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		34	

SWITCHING WAVEFORMS

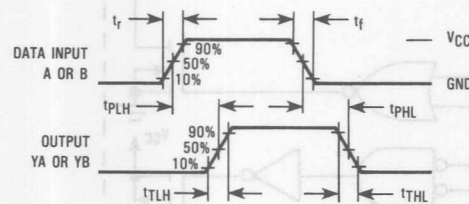


Figure 1

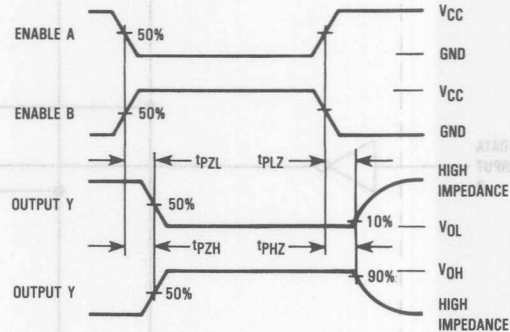
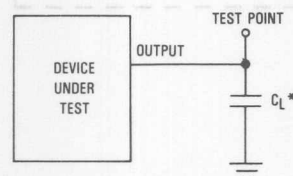
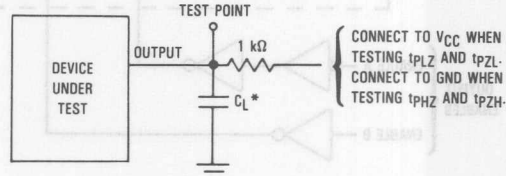


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4 (PINS 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs when the outputs are enabled.

CONTROLS

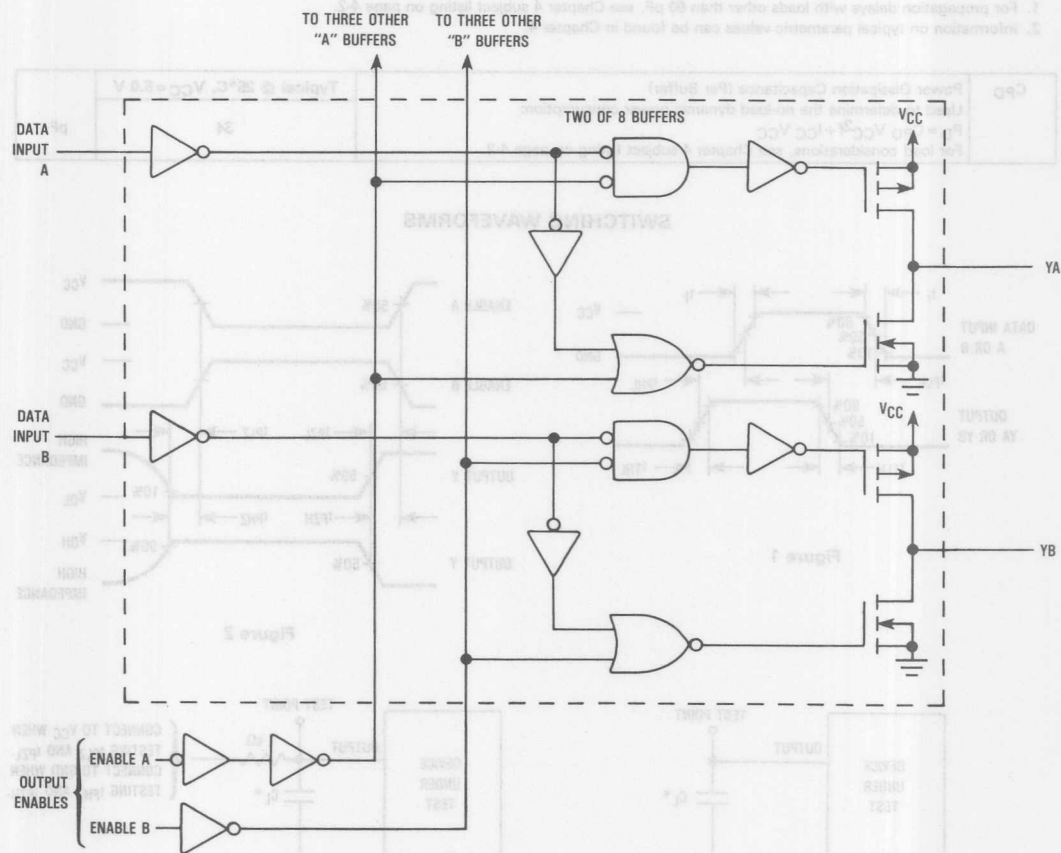
Enable A (PIN 1) — Output enable (active-low). When a low level is applied to this pin, the outputs of the "A" devices are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high-impedance state.

Enable B (PIN 19) — Output enable (active-high). When a high level is applied to this pin, the outputs of the "B" devices are enabled and the devices function as noninverting buffers. When a low level is applied, the outputs assume the high-impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (PINS 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

LOGIC DETAIL



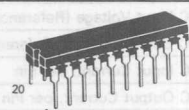
MC54/74HCT241

Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

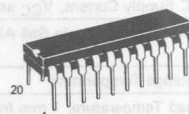
The HCT241 is identical in pinout to the LS241. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT241 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two output enables. Enable A is active-low and Enable B is active-high.

The HCT241 is similar in function to the HCT244. See also HCT240.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 118 FETs or 29.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



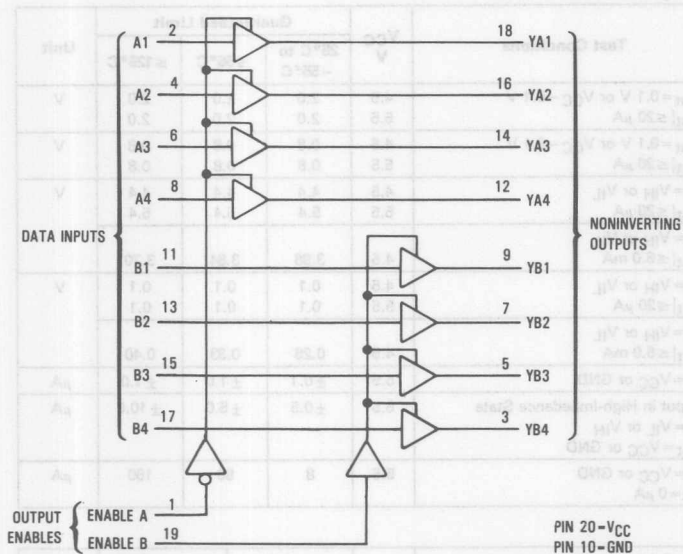
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCTXXN	Plastic
MC54HCTXXJ	Ceramic
MC74HCTXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

ENABLE A	1	20	VCC
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs		Output
Enable A	A	YA
L	L	L
L	H	H
H	X	Z
Inputs		Output
Enable B	B	YB
H	L	L
H	H	H
L	X	Z

Z = high impedance
X = don't care

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V}$, Any One Input $V_{in} = V_{CC} \text{ or GND}$, Other Inputs $I_{out} = 0 \mu\text{A}$	5.5	$\geq -55^\circ\text{C}$ 2.9	25°C to 125°C 2.4		mA

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT241

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	25	31	38	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		55	

SWITCHING WAVEFORMS

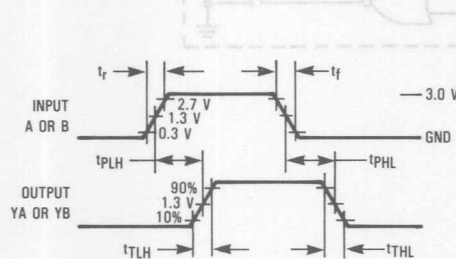


Figure 1

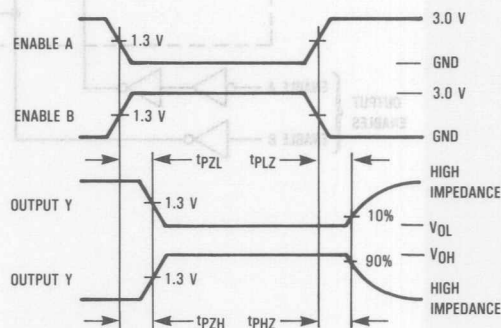
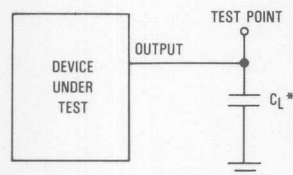
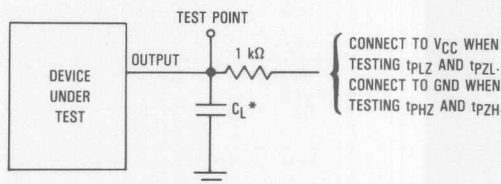


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

Quad 3-State Bus Transceivers

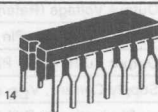
High-Performance Silicon-Gate CMOS

The MC54/74HC242 and MC54/74HC243 are identical in pinout to the LS242 and LS243. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

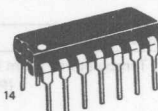
These quad bus transceivers are designed for asynchronous two-way communications between data buses. The states of the Output Enables (A-to-B Enable and B-to-A Enable) determine both the direction of data flow (from A to B or from B to A) and the modes of the Data Ports (input, output, or high-impedance).

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 130 FETs or 32.5 Equivalent Gates (HC242)
146 FETs or 36.5 Equivalent Gates (HC243)

MC54/74HC242 MC54/74HC243



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



S SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

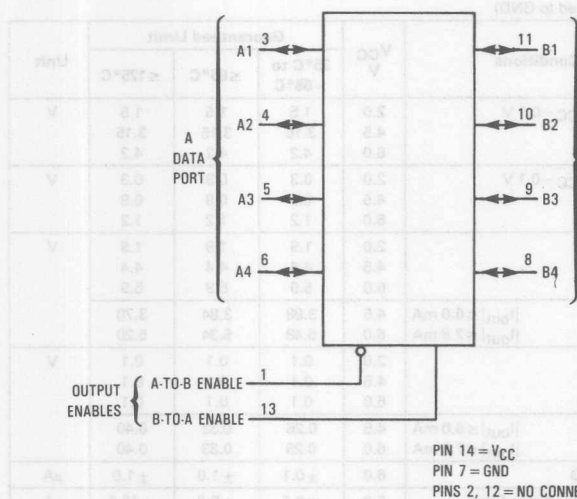
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM

HC242—Inverting Outputs

HC243—Noninverting Outputs



PIN ASSIGNMENT

A-TO-B ENABLE	1	14	VCC
NC	2	13	B-TO-A ENABLE
A1	3	12	NC
A2	4	11	B1
A3	5	10	B2
A4	6	9	B3
GND	7	8	B4

NC = NO CONNECTION

FUNCTION TABLE

Control Inputs		MC54/74HC242		MC54/74HC243	
		Data Port Status		Data Port Status	
A-to-B Enable	B-to-A Enable	A	B	A	B
H	H	\bar{O}	I	O	I
L	H	Z	Z	Z	Z
H	L	Z	Z	Z	Z
L	L	I	\bar{O}	I	O

I = input, O = output, \bar{O} = inverting output,
Z = high impedance

MC54/74HC242•MC54/74HC243

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400 ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or } GND$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC242•MC54/74HC243

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
tPLH, tPHL	Maximum Propagation Delay, A to B/B to A (Figures 1 and 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Output A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Output A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
Cin	Maximum Input Capacitance	—	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	
		31	pF

PIN DESCRIPTIONS

DATA PORTS

A1, A2, A3, A4 (Pins 3, 4, 5, 6) and B1, B2, B3, B4 (Pins 11, 10, 9, 8) — Data on these pins may be transferred between data buses. Depending upon the states of the Output Enables, these pins may be inputs, outputs, or open circuits (high-impedance).

CONTROL INPUTS

A-to-B Enable (Pin 1) and B-to-A Enable (Pin 13) — Data on these Output Enables determine both the direction of data flow (from A to B or from B to A) and the states of the outputs (standard or high impedance), according to the Function Table.

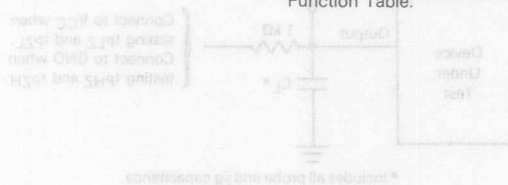


FIGURE 1a — HC242

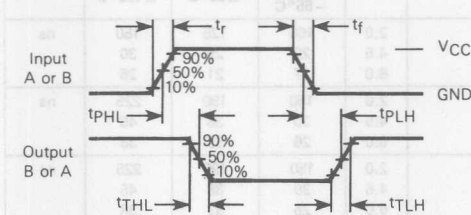


FIGURE 1b — HC243

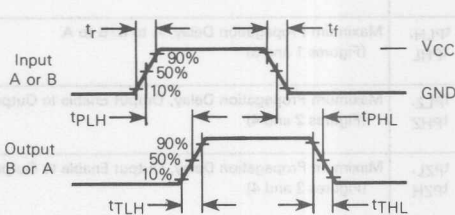


FIGURE 2

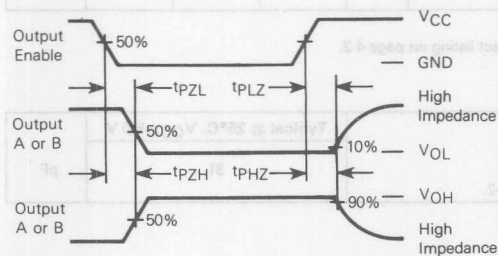
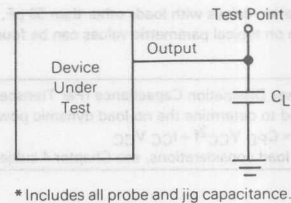
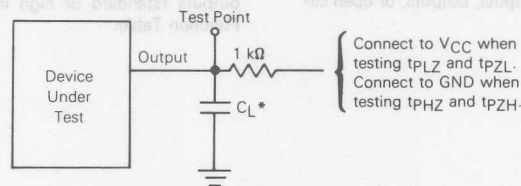


FIGURE 3 — TEST CIRCUIT



* Includes all probe and jig capacitance.

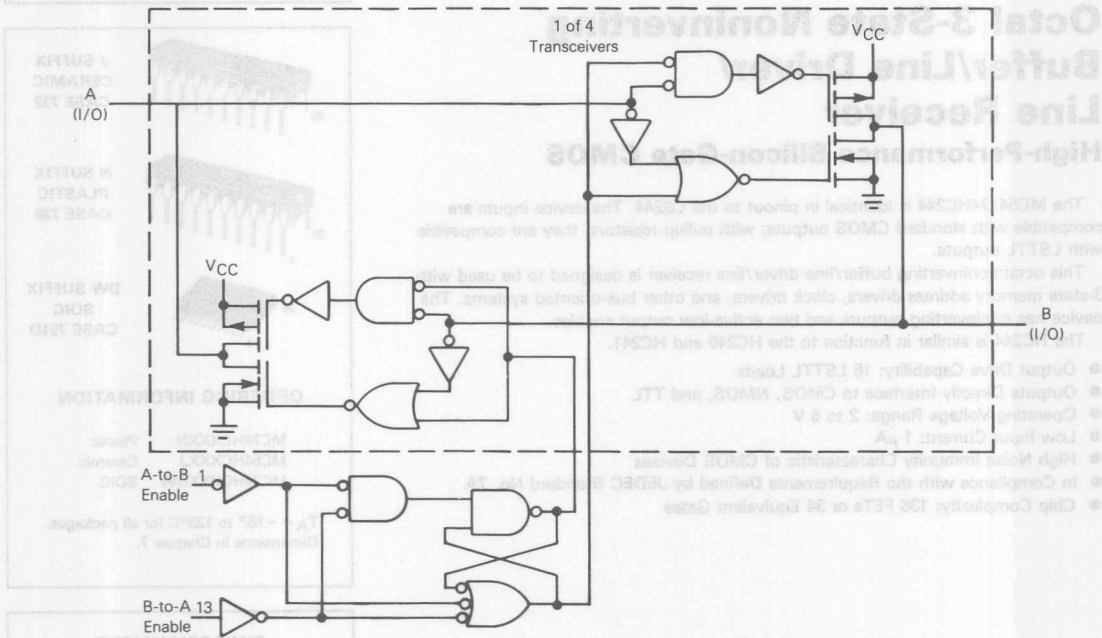
FIGURE 4 — TEST CIRCUIT



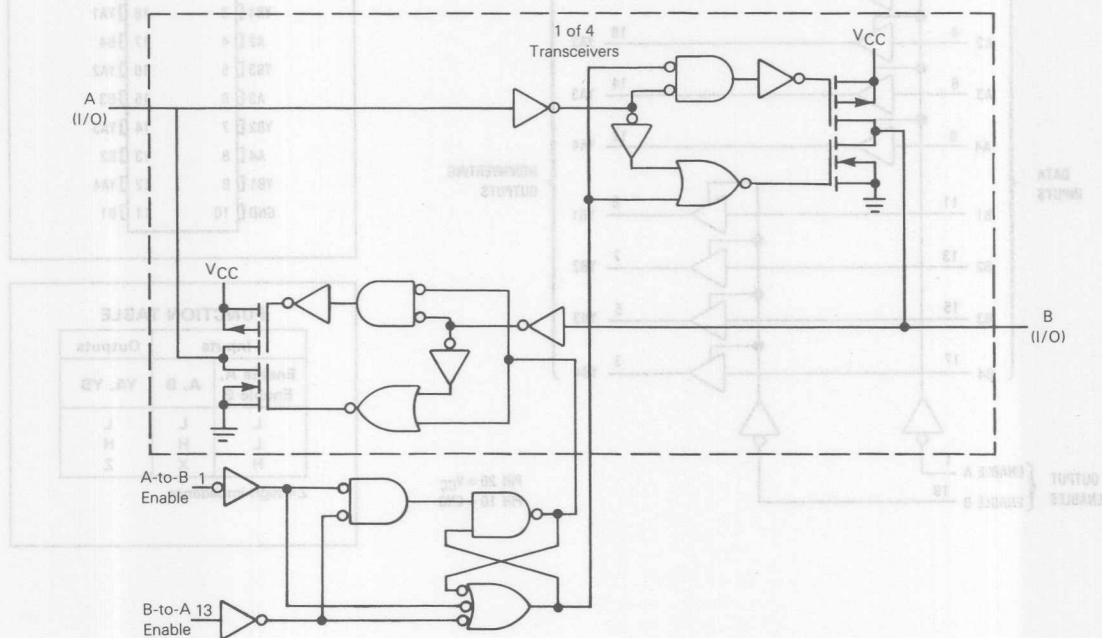
* Includes all probe and jig capacitance.

MC54/74HC242•MC54/74HC243

LOGIC DETAIL HC242



LOGIC DETAIL HC243



Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver

High-Performance Silicon-Gate CMOS

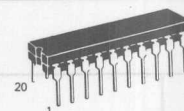
The MC54/74HC244 is identical in pinout to the LS244. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs and two active-low output enables.

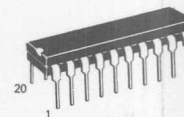
The HC244 is similar in function to the HC240 and HC241.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates

MC54/74HC244



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



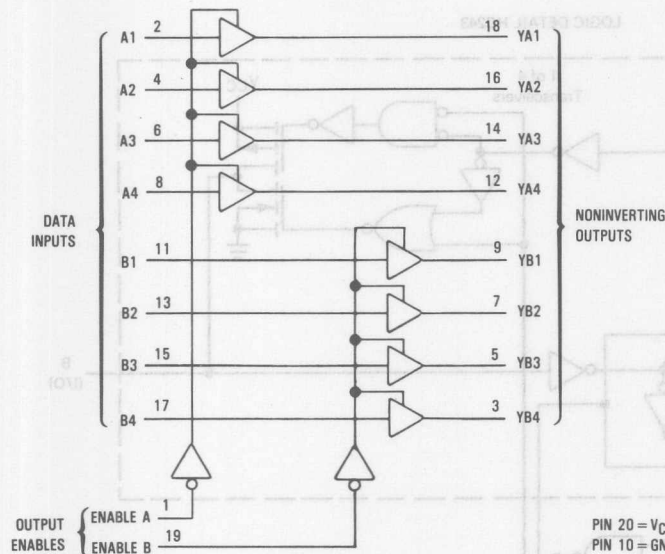
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

ENABLE A	1	20	V_{CC}
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance

MC54/74HC244

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400
				ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		34	

SWITCHING WAVEFORMS

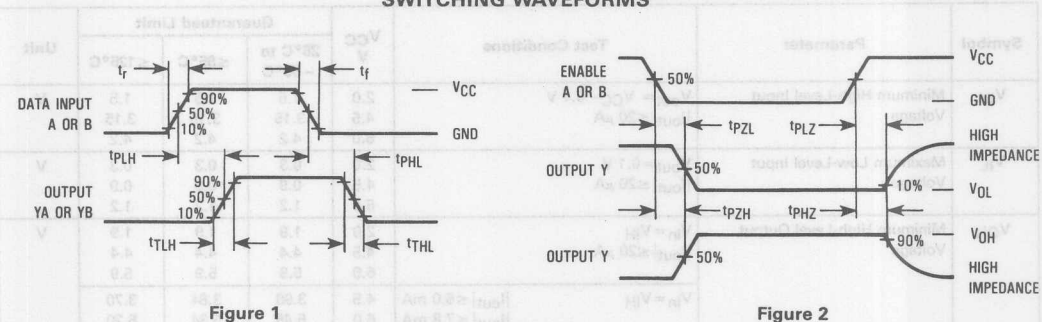
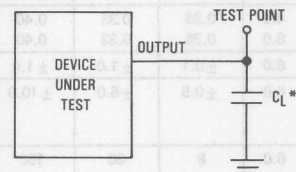


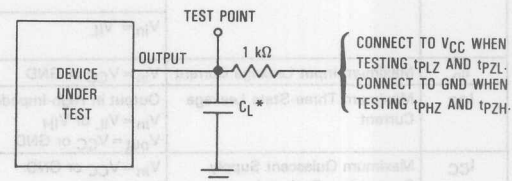
Figure 1

Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

MC54/74HC244

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4 (PINS 2, 4, 6, 8, 11, 13, 15, 17) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

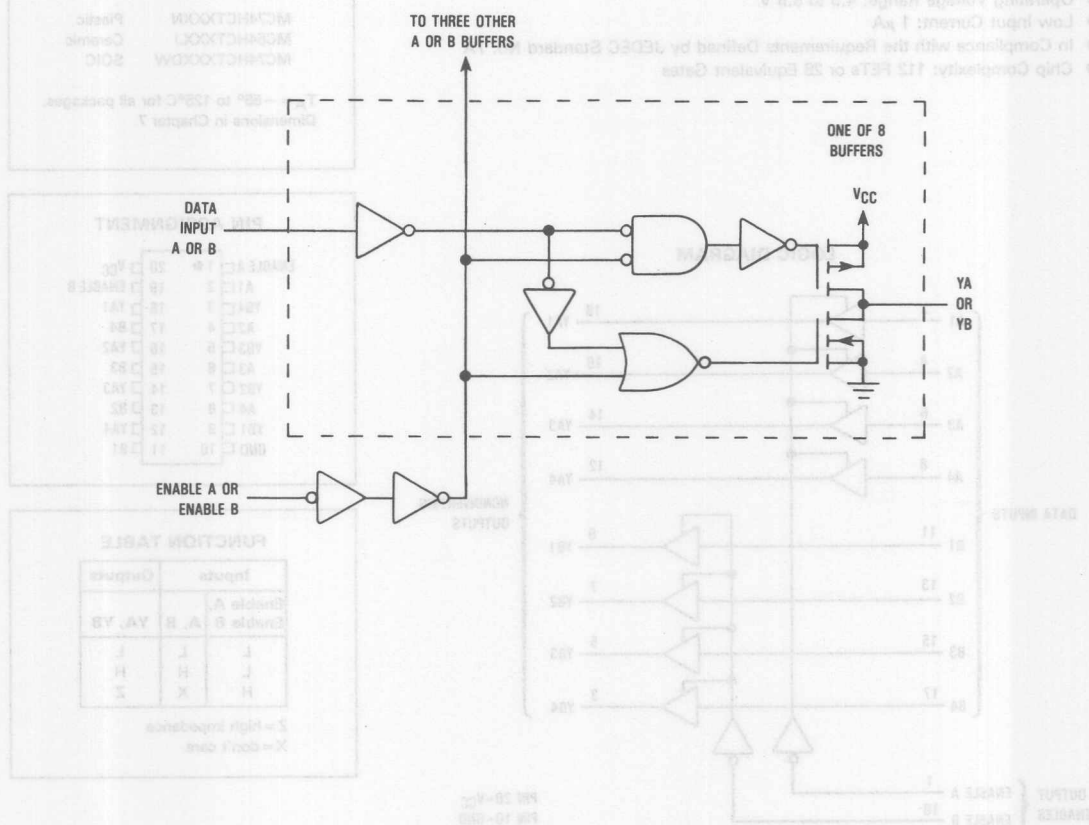
Enable A, Enable B (PINS 1, 19) — Output enables (active-low). When a low level is applied to these pins, the outputs

are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high-impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (PINS 18, 16, 14, 12, 9, 7, 5, 3) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

LOGIC DETAIL



MC54/74HCT244

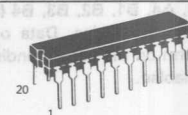
Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

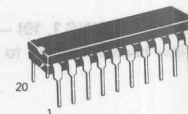
The HCT244 is identical in pinout to the LS244. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT244 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two active-low output enables.

The HCT244 is the noninverting version of the HCT240. See also HCT241.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 112 FETs or 28 Equivalent Gates



J SUFFIX
 CERAMIC
 CASE 732



N SUFFIX
 PLASTIC
 CASE 738



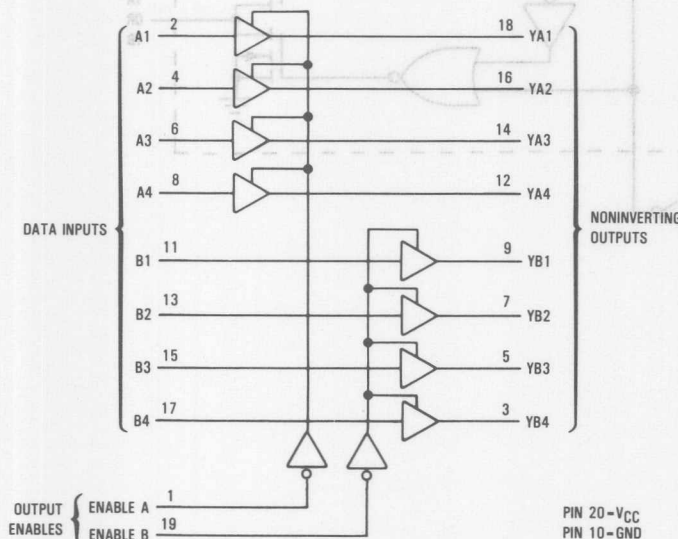
DW SUFFIX
 SOIC
 CASE 751D

ORDERING INFORMATION

MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

ENABLE A	1	20	V_{CC}
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance
 X = don't care

MC54/74HCT244

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	3.98 0.1	3.84 0.1	3.70 0.1	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	5.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C 2.9	25°C to 125°C 2.4		mA

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	25	31	38	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	30	38	45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	pF
		55	

SWITCHING WAVEFORMS

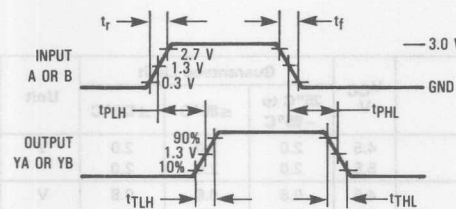


Figure 1

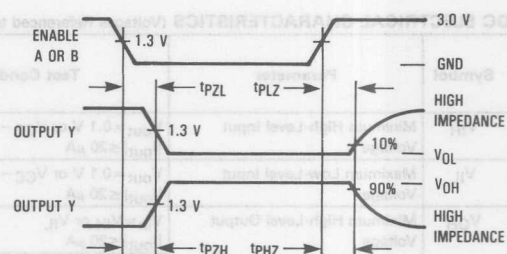
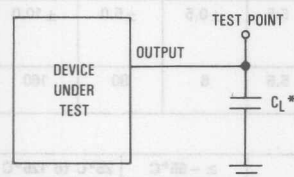
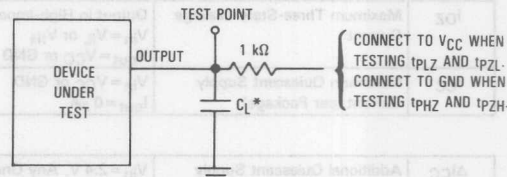


Figure 2



*Includes all probe and jig capacitance.



*Includes all probe and jig capacitance.

Figure 3. Test Circuit

Figure 4. Test Circuit

MC54/74HCT244

CERAMIC
CASE 732N SURFIX
PLASTIC
CASE 738DW SURFIX
SOIC
CASE 752D

ORDERING INFORMATION

MC54HCT244
Ceramic
MC74HCT244
Plastic
MC54HCT244D
SOIC

TA = -55° to 125°C for all packages.
Observations in Chapter 7.

PIN ASSIGNMENT

DIRECTION	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

FUNCTION TABLE

Enable	Output Direction	Operation
L	L	Data Transmitted from Bus A to Bus B
L	H	Data Transmitted from Bus B to Bus A
X	X	(High-Impedance State)

X = don't care

LOGIC DETAIL

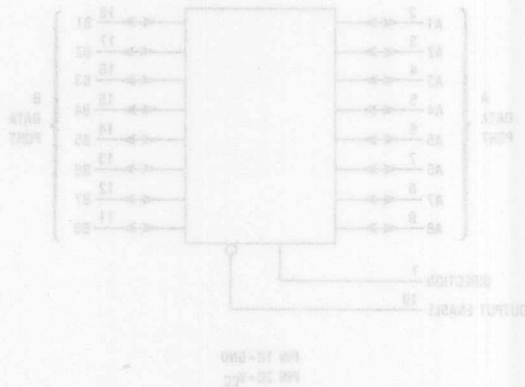
TO THREE OTHER
A OR B BUFFERSONE OF 8
BUFFERSDATA INPUT
A OR B

ENABLE A OR ENABLE B

VCC

YA
OR
YB

LOGIC DIAGRAM



Octal 3-State Noninverting Bus Transceiver

High-Performance Silicon-Gate CMOS

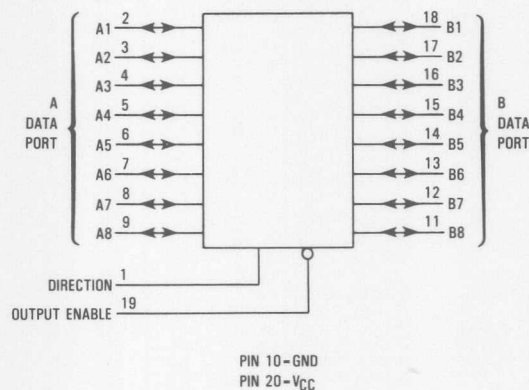
The MC54/74HC245 is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC245 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

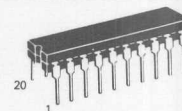
The HC245 performs functions similar to those of the HC640 and the HC643.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 308 FETs or 77 Equivalent Gates

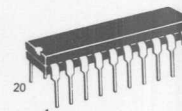
LOGIC DIAGRAM



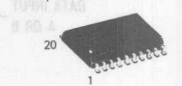
MC54/74HC245



J SUFFIX
 CERAMIC
 CASE 732



N SUFFIX
 PLASTIC
 CASE 738



DW SUFFIX
 SOIC
 CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT

DIRECTION	1	20	VCC
A1	2	19	OUTPUT ENABLE
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

X = don't care

MC54/74HC245

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin 1 or 19	± 20	mA
$I_{I/O}$	DC I/O Current, per I/O Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND, Pin 1 or 19}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND, I/O Pins}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, input $t_r = t_f = 0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance (Pin 1 or Pin 19)	—	10	10	10	pF
C_{out}	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		40	

SWITCHING WAVEFORMS

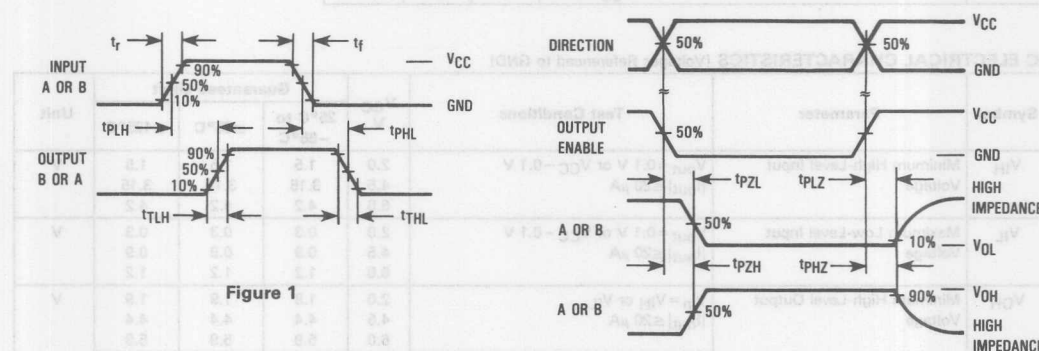
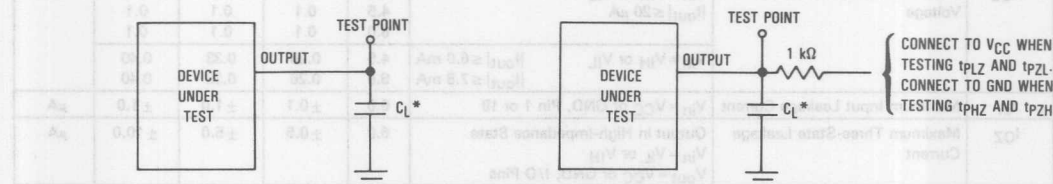


Figure 1

Figure 2



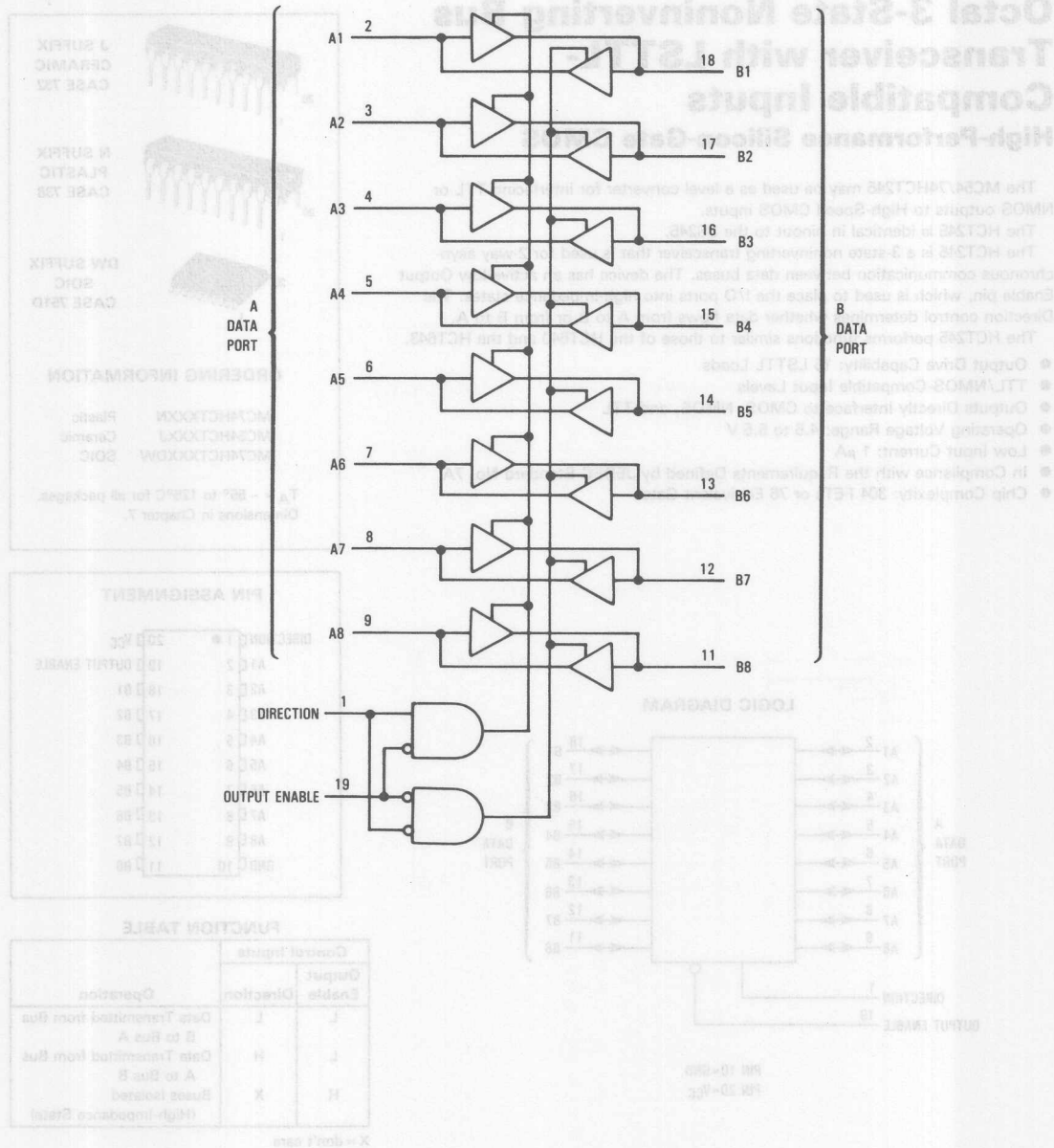
*Includes all probe and jig capacitance.

*Includes all probe and jig capacitance.

Figure 3. Test Circuit

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC54/74HCT245 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

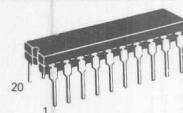
The HCT245 is identical in pinout to the LS245.

The HCT245 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

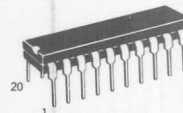
The HCT245 performs functions similar to those of the HCT640 and the HCT643.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 304 FETs or 76 Equivalent Gates

MC54/74HCT245



J SUFFIX
 CERAMIC
 CASE 732



N SUFFIX
 PLASTIC
 CASE 738



DW SUFFIX
 SOIC
 CASE 751D

ORDERING INFORMATION

MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT

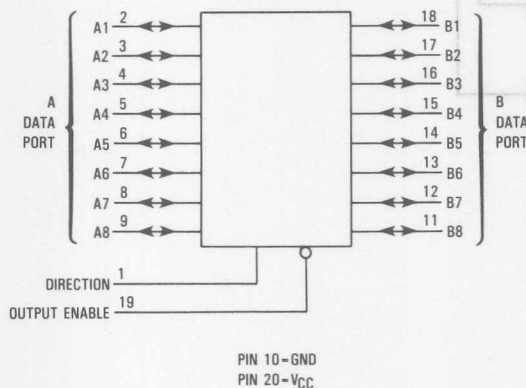
DIRECTION	1	20	V _{CC}
A1	2	19	OUTPUT ENABLE
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

X = don't care

LOGIC DIAGRAM



MC54/74HCT245

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin 1 or 19	± 20	mA
$I_{I/O}$	DC I/O Current, per I/O Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_{r, t_f}	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5 5.5	3.98 0.1	3.84 0.1	3.70 0.1	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND, Pin 1 or 19}$	5.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND, I/O Pins}$	5.5	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C 2.9	25°C to 125°C 2.4		mA

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to B or B to A (Figures 1 and 3)	22	28	33	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C _{in}	Maximum Input Capacitance (Pin 1 or 19)	10	10	10	pF
C _{out}	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		45	

SWITCHING WAVEFORMS

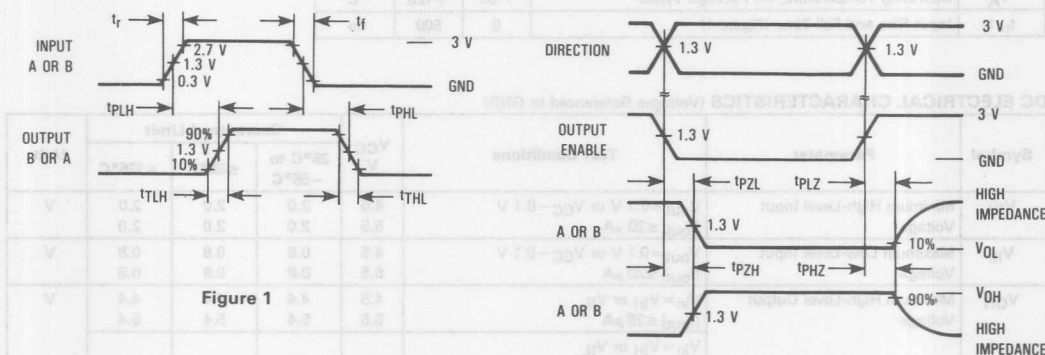


Figure 1

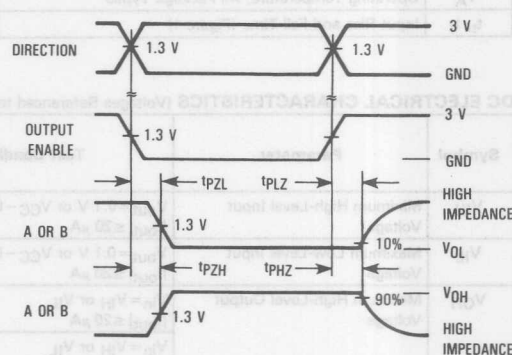
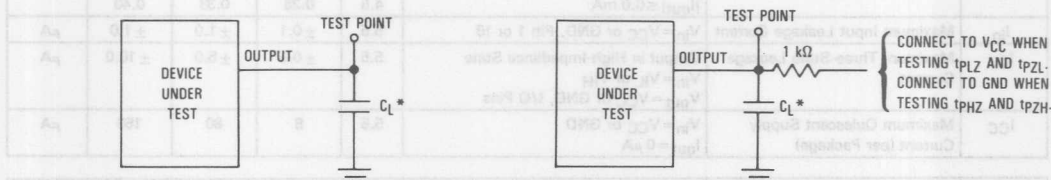
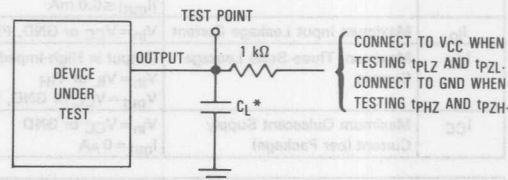


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit

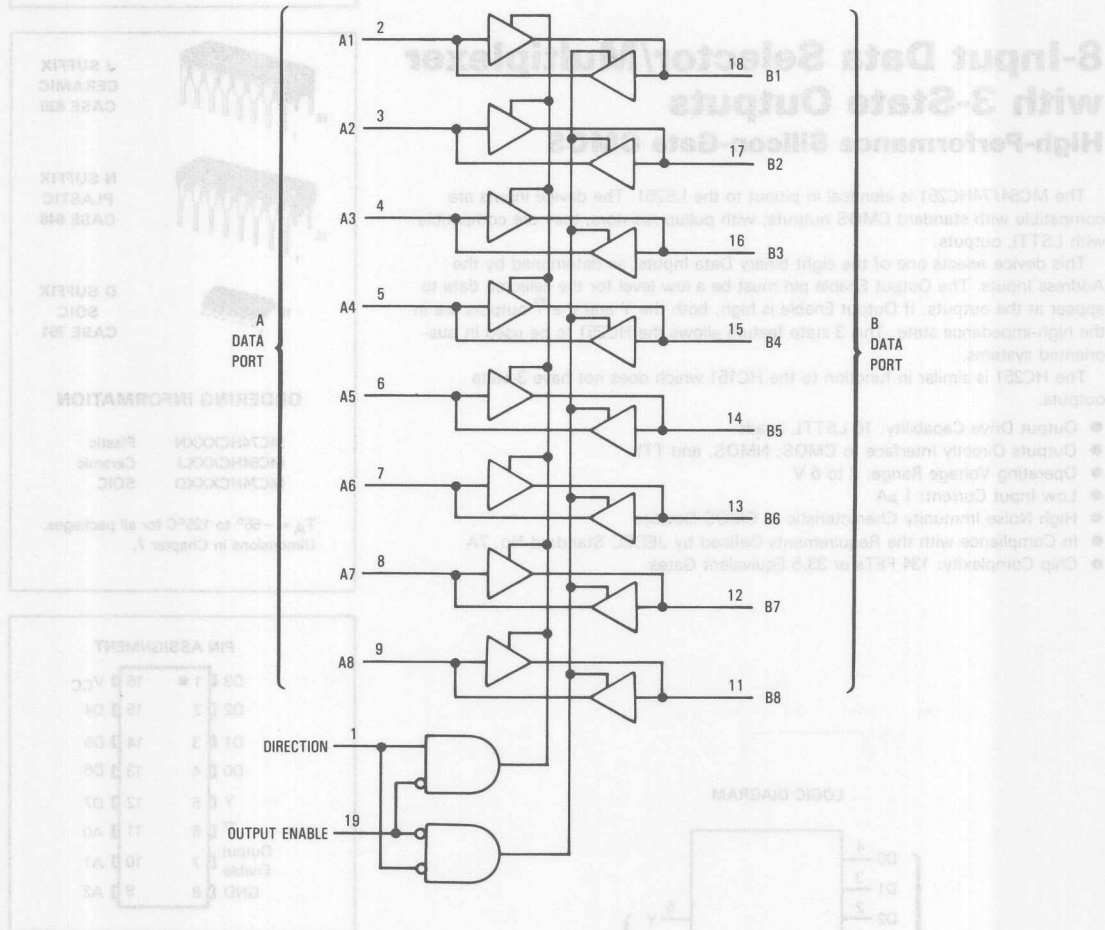


*Includes all probe and jig capacitance.

Figure 4. Test Circuit

MC54/74HCT245

EXPANDED LOGIC DIAGRAM



FUNCTION TABLE

Inputs	Output	Y
A1 A2	Output Enable	Y
X X	H	2
L L	L	00
L H	L	01
L H	L	02
L H	L	03
L H	L	04
L H	L	05
L H	L	06
L H	L	07
L H	L	08
L H	L	09
L H	L	10
L H	L	11
L H	L	12
L H	L	13
L H	L	14
L H	L	15
L H	L	16
L H	L	17
L H	L	18
L H	L	19
L H	L	20
L H	L	21
L H	L	22
L H	L	23
L H	L	24
L H	L	25
L H	L	26
L H	L	27
L H	L	28
L H	L	29
L H	L	30
L H	L	31

L = high-impedance state
D0, D1, D2 = the level of the respective D input



MC54/74HC251

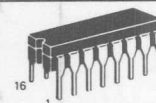
8-Input Data Selector/Multiplexer with 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC251 is identical in pinout to the LS251. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

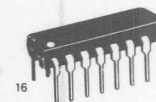
This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be a low level for the selected data to appear at the outputs. If Output Enable is high, both the Y and the \bar{Y} outputs are in the high-impedance state. This 3-state feature allows the HC251 to be used in bus-oriented systems.

The HC251 is similar in function to the HC151 which does not have 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

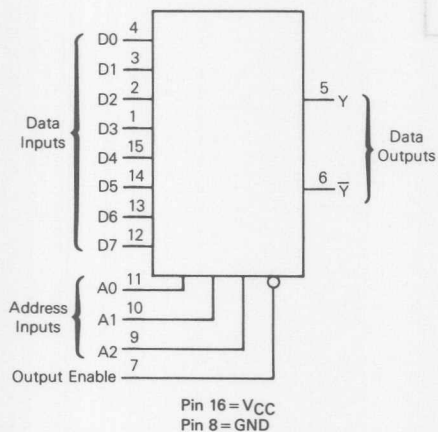
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

D3	1	16	V _{CC}
D2	2	15	D4
D1	3	14	D5
D0	4	13	D6
Y	5	12	D7
\bar{Y}	6	11	A0
Output Enable	7	10	A1
GND	8	9	A2

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output Enable	Outputs	
A2	A1	A0		Y	\bar{Y}
X	X	X	H	Z	Z
L	L	L	L	D0	$\bar{D0}$
L	L	H	L	D1	$\bar{D1}$
L	H	L	L	D2	$\bar{D2}$
L	H	H	L	D3	$\bar{D3}$
H	L	L	L	D4	$\bar{D4}$
H	L	H	L	D5	$\bar{D5}$
H	H	L	L	D6	$\bar{D6}$
H	H	H	L	D7	$\bar{D7}$

Z = high-impedance state
D0, D1, . . . D7 = the level of the respective D input

MC54/74HC251

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 25	mA
I_{out}	DC Output Current, per Pin	± 50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	– 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	25°C to -55°C	≤85°C	≤125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Output Y or \bar{Y} (Figures 1, 2 and 5)	2.0 4.5 6.0	185 37 31	230 46 39	280 56 48	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y or \bar{Y} (Figures 3 and 5)	2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6)	2.0 4.5 6.0	195 39 33	245 49 42	295 59 50	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 4 and 6)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Output \bar{Y} (Figures 4 and 6)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Output \bar{Y} (Figures 4 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		36	

5

PIN DESCRIPTIONS

INPUTS

D0, D1, . . . , D7 (PINS 4, 3, 2, 1, 15, 14, 13, 12) — Data inputs. Data on one of these eight binary inputs may be selected to appear on the output.

CONTROL INPUTS

A0, A1, A2 (PINS 11, 10, 9) — Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

OUTPUT ENABLE (PIN 7) — Output Enable. This input pin must be at a low level for the selected data to appear at the outputs. If the Output Enable pin is high, both the Y and \bar{Y} outputs are taken to the high-impedance state.

OUTPUTS

Y, \bar{Y} (PINS 5, 6) — Data outputs. The selected data is presented at these pins in both true (Y output) and complemented (\bar{Y} output) forms.

MC54/74HC251

SWITCHING WAVEFORMS

FIGURE 1

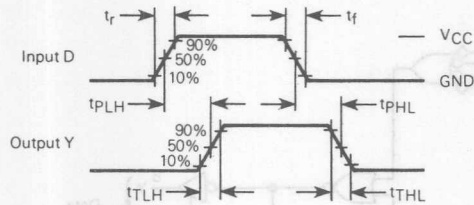


FIGURE 2

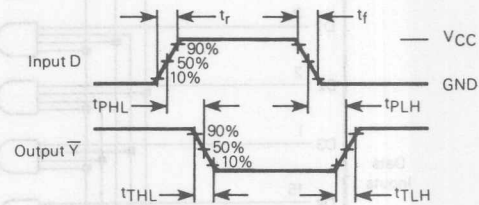


FIGURE 3

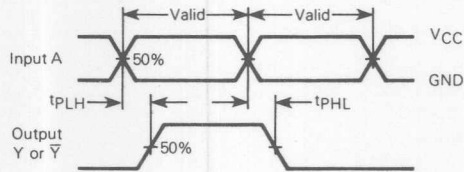


FIGURE 4

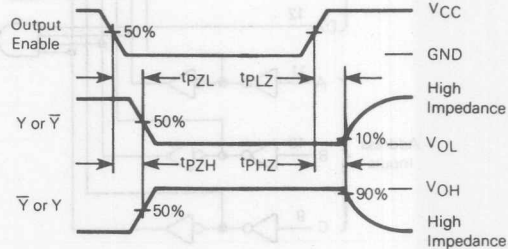
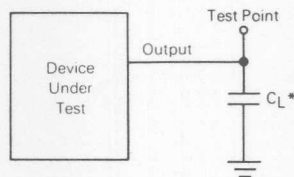
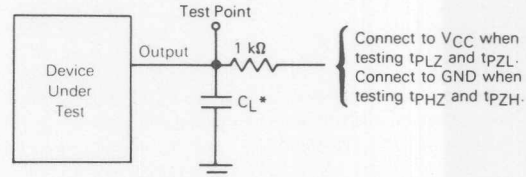


FIGURE 5 — TEST CIRCUIT



* Includes all probe and jig capacitance.

FIGURE 6 — TEST CIRCUIT

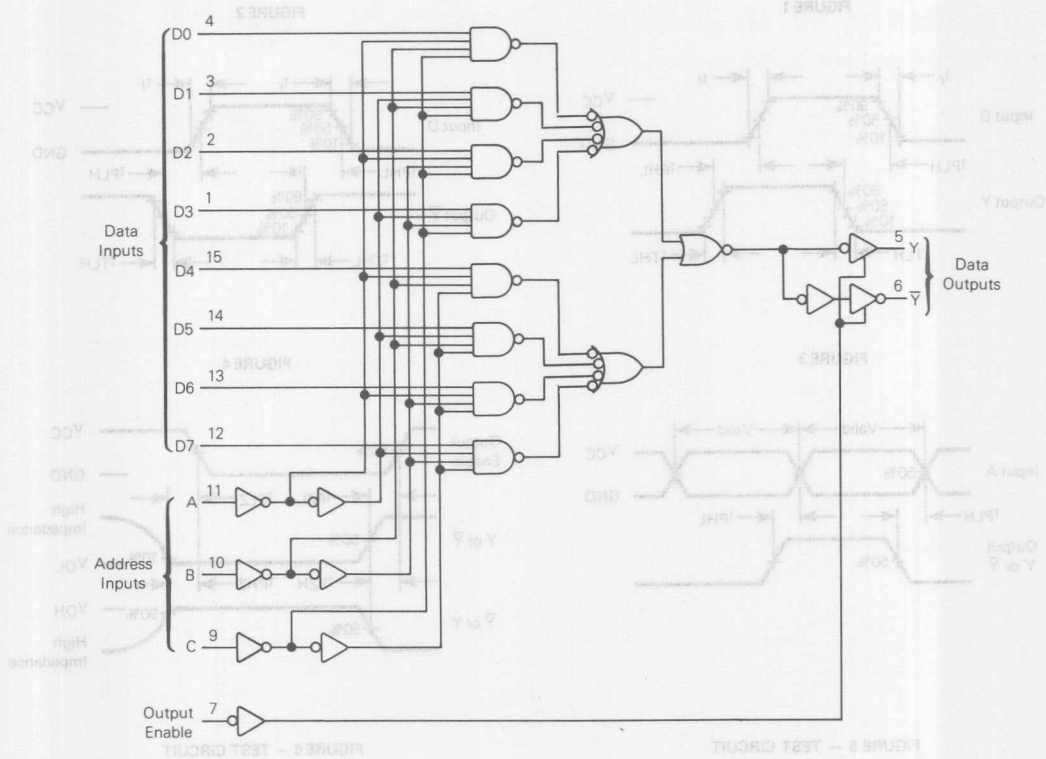


* Includes all probe and jig capacitance.

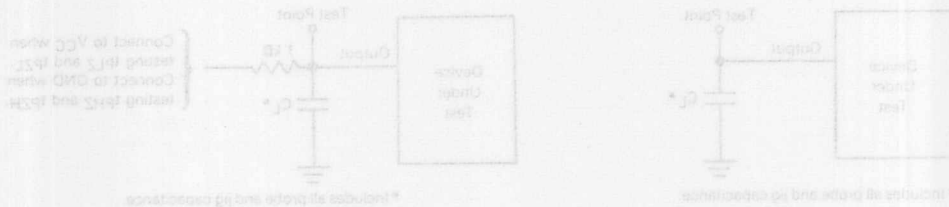
5

MC54/74HC251

EXPANDED LOGIC DIAGRAM



5



MC54/74HC253

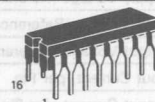
Dual 4-Input Data Selector/ Multiplexer With 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC253 is identical in pinout to the LS253. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

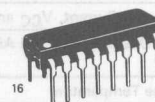
The Address inputs select one of four Data inputs from each multiplexer. Each multiplexer has an active-low Output Enable control and a three-state noninverting output.

The HC253 is similar in function to the HC153 which does not have three-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



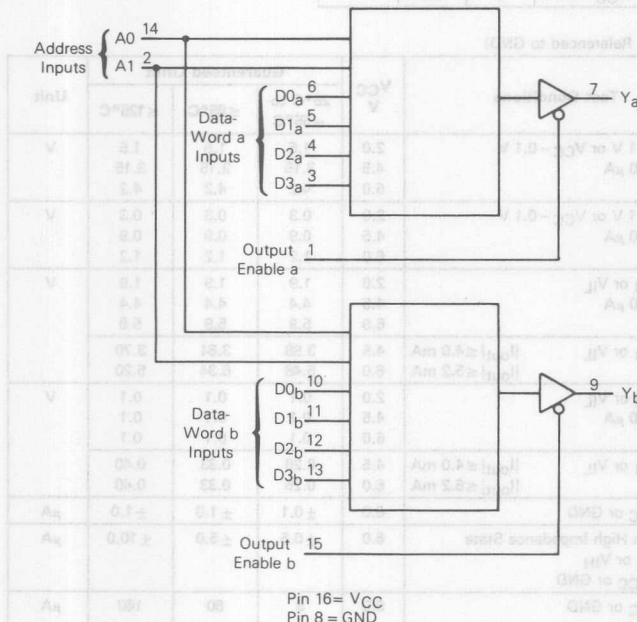
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

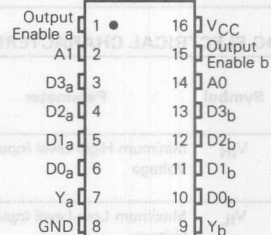
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output	Output
A1	A0	Enable	Y
X	X	H	Z
L	L	L	D0
L	H	L	D1
H	L	L	D2
H	H	L	D3

D0, D1, D2, and D3 = the level of the respective Data Inputs
Z = high impedance

V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out}=0.1\text{ V}$ or $V_{CC}-0.1\text{ V}$ $ I_{out} \leq 20\text{ }\mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out}=0.1\text{ V}$ or $V_{CC}-0.1\text{ V}$ $ I_{out} \leq 20\text{ }\mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 20\text{ }\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 4.0\text{ mA}$ $ I_{out} \leq 5.2\text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 20\text{ }\mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 4.0\text{ mA}$ $ I_{out} \leq 5.2\text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in}=V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in}=V_{IL}$ or V_{IH} $V_{out}=V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in}=V_{CC}$ or GND $I_{out}=0\text{ }\mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC253

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Data to Output Y (Figures 1 and 3)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Address to Output Y (Figures 1 and 3)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Multiplexer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		31	

SWITCHING WAVEFORMS

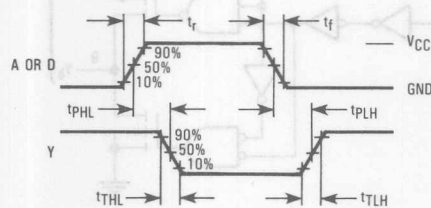


Figure 1

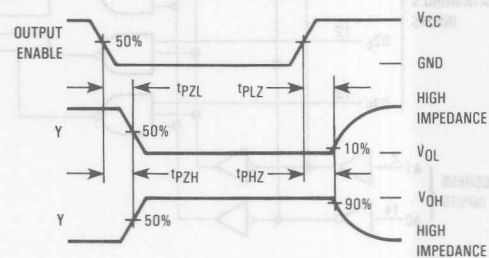
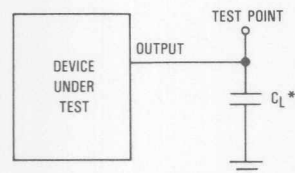
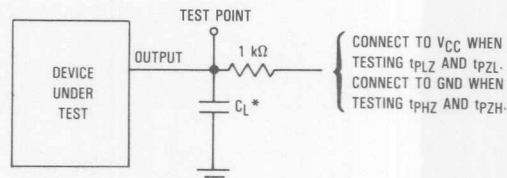


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

MC54/74HC253

PIN DESCRIPTIONS

DATA INPUTS

D0_a-D3_a, D0_b-D3_b (PINS 3, 4, 5, 6, 10, 11, 12, 13) — Data inputs. When one of these pairs of inputs is selected and the outputs are enabled, the outputs assume the state of the respective inputs.

CONTROL INPUTS

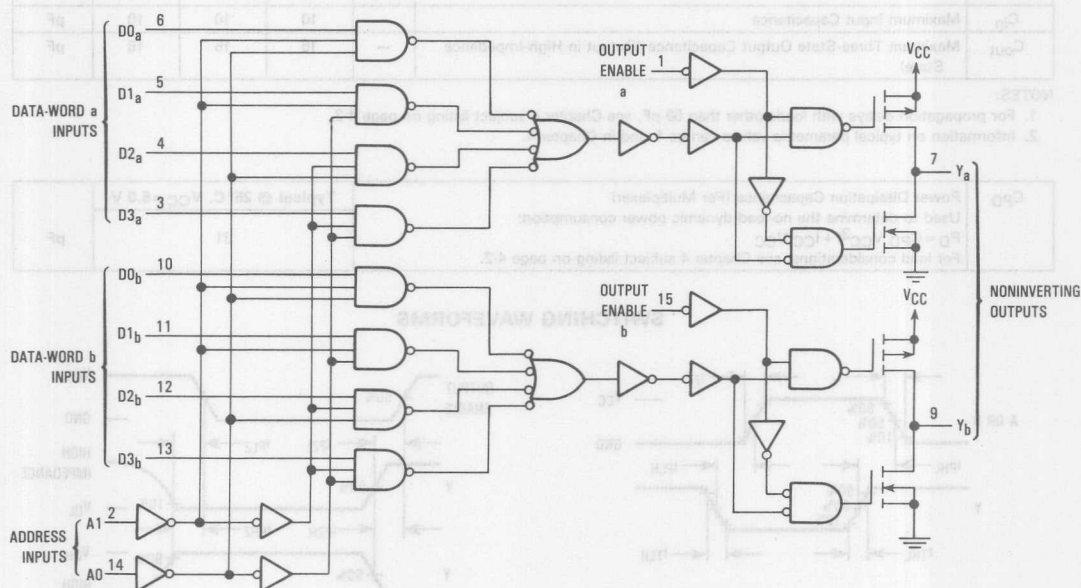
A0, A1 (PINS 2, 14) — Address inputs. These inputs select the pair of Data inputs to appear at the corresponding outputs.

OUTPUT ENABLE (PINS 1, 15) — Active-low three-state Output Enable. When a low level is applied to these inputs, the corresponding outputs are enabled. When a high level is applied, the outputs assume the high-impedance state.

OUTPUTS

Y_a, Y_b (PINS 7, 9) — Noninverting three-state outputs.

LOGIC DETAIL



5

MC54/74HC257

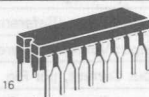
Quad 2-Input Data Selector/ Multiplexer With 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC257 is identical in pinout to the LS257. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

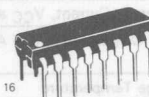
This device selects a (4-bit) nibble from either the A or B inputs as determined by the Select input. The nibble is presented at the outputs in noninverted form when the Output Enable pin is at a low level. A high level on the Output Enable pin switches the outputs into the high-impedance state.

The HC257 is similar in function to the HC157 which do not have 3-state outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates



J SUFFIX
 CERAMIC
 CASE 620



N SUFFIX
 PLASTIC
 CASE 648



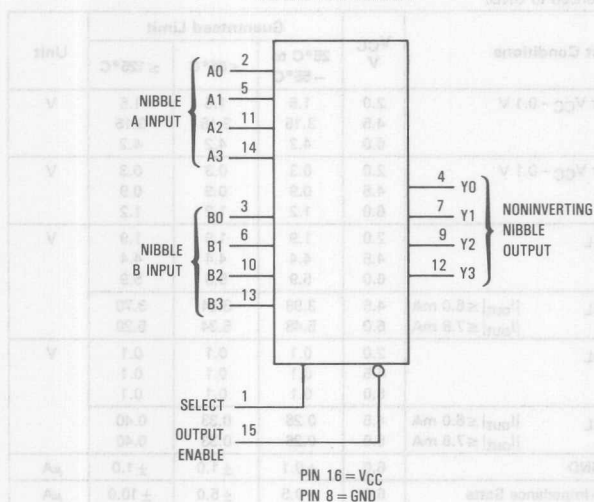
D SUFFIX
 SOIC
 CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 * Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

SELECT	1	16	VCC
A0	2	15	OUTPUT ENABLE
B0	3	14	A3
Y0	4	13	B3
A1	5	12	Y3
B1	6	11	A2
Y1	7	10	B2
GND	8	9	Y2

FUNCTION TABLE

Inputs		Outputs
Output Enable	Select	Y0-Y3
H	X	Z
L	L	A0-A3
L	H	B0-B3

X = don't care
 Z = high-impedance state
 A0-A3, B0-B3 = the levels of the respective Nibble Inputs.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC257

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
tPLH, tPHL	Maximum Propagation Delay, Nibble A or B to Output Y (Figures 1 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
tPLH, tPHL	Maximum Propagation Delay, Select to Output Y (Figures 2 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	pF
		39	

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (PINS 2, 5, 11, 14) — Nibble A input. The data present on these pins is transferred to the output when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

B0, B1, B2, B3 (PINS 3, 6, 10, 13) — Nibble B input. The logic data present on these pins is transferred to the output when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

OUTPUTS

Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12) — Nibble output. The selected nibble input is presented at these outputs when the

Output Enable input is at a low level. For the Output Enable input at a high level, the outputs are switched to the high impedance state.

CONTROL INPUTS

SELECT (PIN 1) — Nibble select. This input determines the nibble to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

OUTPUT ENABLE (PIN 15) — Output Enable. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input forces the outputs into the high-impedance state.

MC54/74HC257

SWITCHING WAVEFORMS

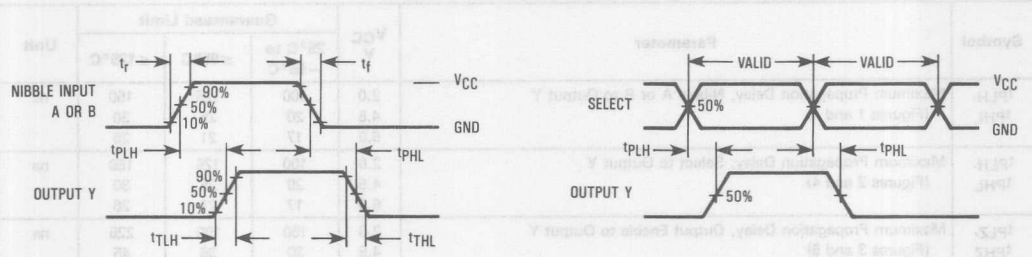


Figure 1

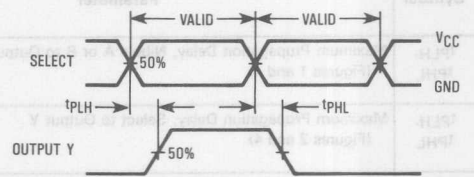


Figure 2

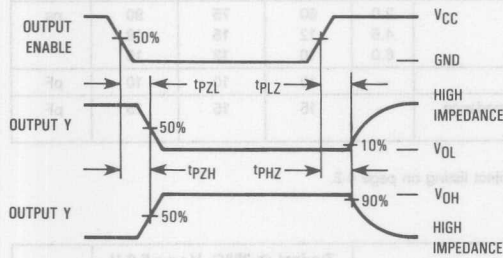
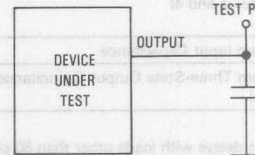
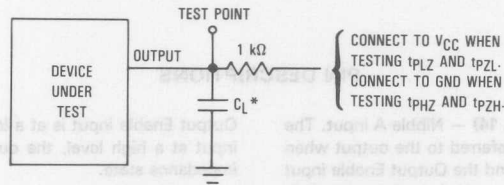


Figure 3



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

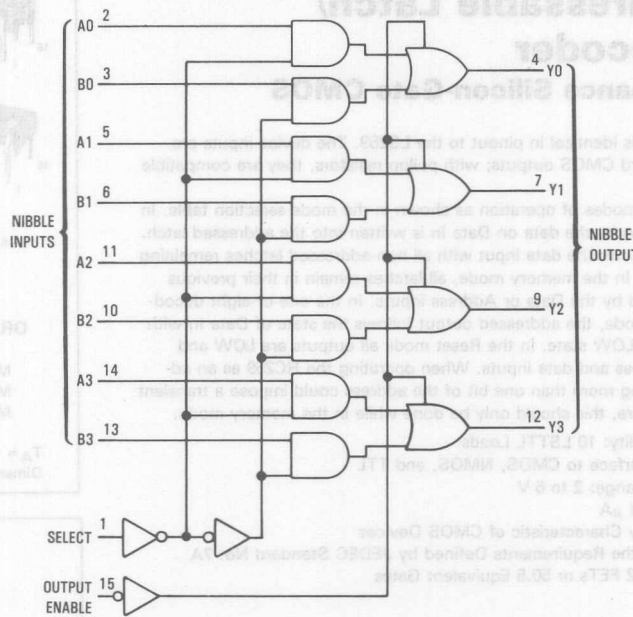


*Includes all probe and jig capacitance.

Figure 5. Test Circuit

MC54/74HC257

EXPANDED LOGIC DIAGRAM



1 SURFAC
CERAMIC
CASE 853

1 SURFAC
PLASTIC
CASE 866

1 SURFAC
SOIC
CASE 751

ORDERING INFORMATION

MC54HC257 Plastic
MC74HC257 Plastic
MC54HC257 SOIC
MC74HC257 SOIC

T_A = -55°C to 125°C for all packages.
Dimensions in Centimeters

PIN ASSIGNMENT

Pin	Symbol	Pin	Symbol
1	SELECT	14	A3
2	A0	15	OUTPUT ENABLE
3	B0	16	B3
4	Y0	17	A1
5	A1	18	B1
6	B1	19	Y1
7	Y1	20	A2
8	A2	21	B2
9	B2	22	Y2
10	Y2	23	A3
11	A3	24	B3
12	B3	25	Y3
13	Y3	26	A0

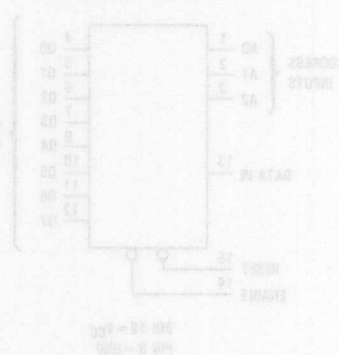
MODE SELECTION TABLE

Mode	Enable	Reset
1-of-8 Decoder	L	H
2-of-4 Decoder	L	L
3-of-2 Decoder	L	L

LATCH SELECTION TABLE

Address Inputs	Address Inputs	Address Inputs
A0	A1	A2
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L
L	L	L

LOGIC DIAGRAM



Advance Information

8-Bit Addressable Latch/ 1-of-8 Decoder

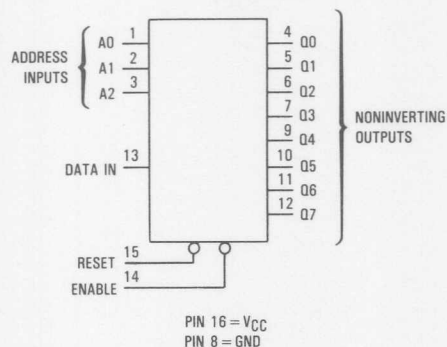
High-Performance Silicon-Gate CMOS

The MC54/74HC259 is identical in pinout to the LS259. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

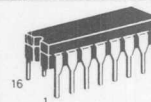
The HC259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode all outputs are LOW and unaffected by the address and data inputs. When operating the HC259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates

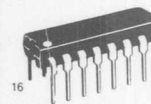
LOGIC DIAGRAM



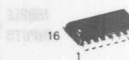
MC54/74HC259



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



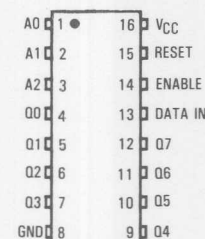
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8-Line Demultiplexer
H	L	Reset

LATCH SELECTION TABLE

Address Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC259

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0$ V 0 $V_{CC} = 4.5$ V 0 $V_{CC} = 6.0$ V	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC259

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Data to Output (Figures 1 and 6)	2.0	185	230	280	ns
		4.5	37	46	56	
		6.0	31	39	48	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Address Select to Output (Figures 2 and 6)	2.0	215	270	325	ns
		4.5	43	54	65	
		6.0	37	46	55	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Enable to Output (Figures 3 and 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t_{PHL}	Maximum Propagation Delay, Reset to Output (Figures 4 and 6)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		30	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Address or Data to Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_h	Minimum Hold Time, Enable to Address or Data (Figure 5)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_w	Minimum Pulse Width, Reset or Enable (Figure 3 or 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

V	1.0	1.0	1.0	0.5	Maximum Low-Level Output Voltage
	1.0	1.0	1.0	0.5	
	1.0	1.0	1.0	0.5	
V _{OL}	0.5	0.5	0.5	0.5	Maximum Input Leakage Current
	0.5	0.5	0.5	0.5	
	0.5	0.5	0.5	0.5	
I _{CC}	0.5	0.5	0.5	0.5	Maximum Ambient Supply Current (per package)
	0.5	0.5	0.5	0.5	
	0.5	0.5	0.5	0.5	

MC54/74HC259

SWITCHING WAVEFORMS

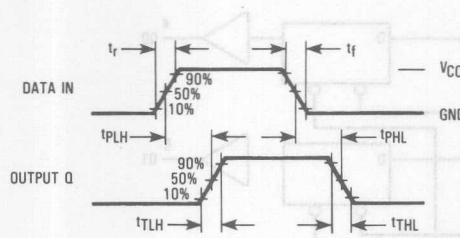


Figure 1

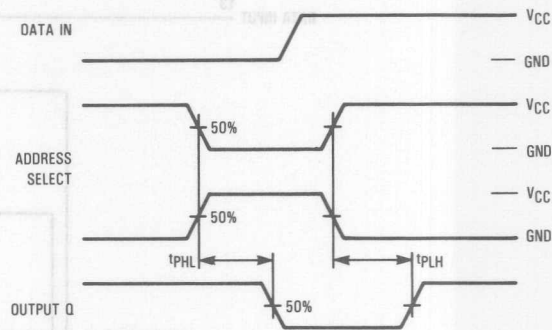


Figure 2

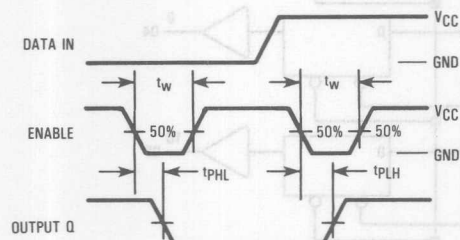


Figure 3

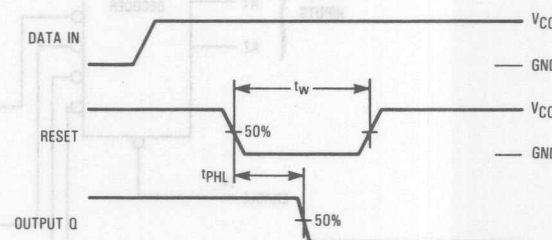


Figure 4

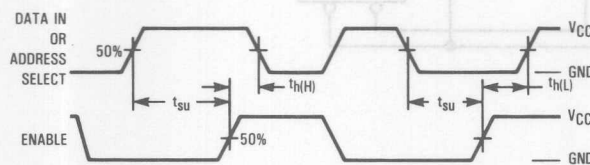
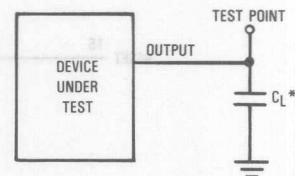
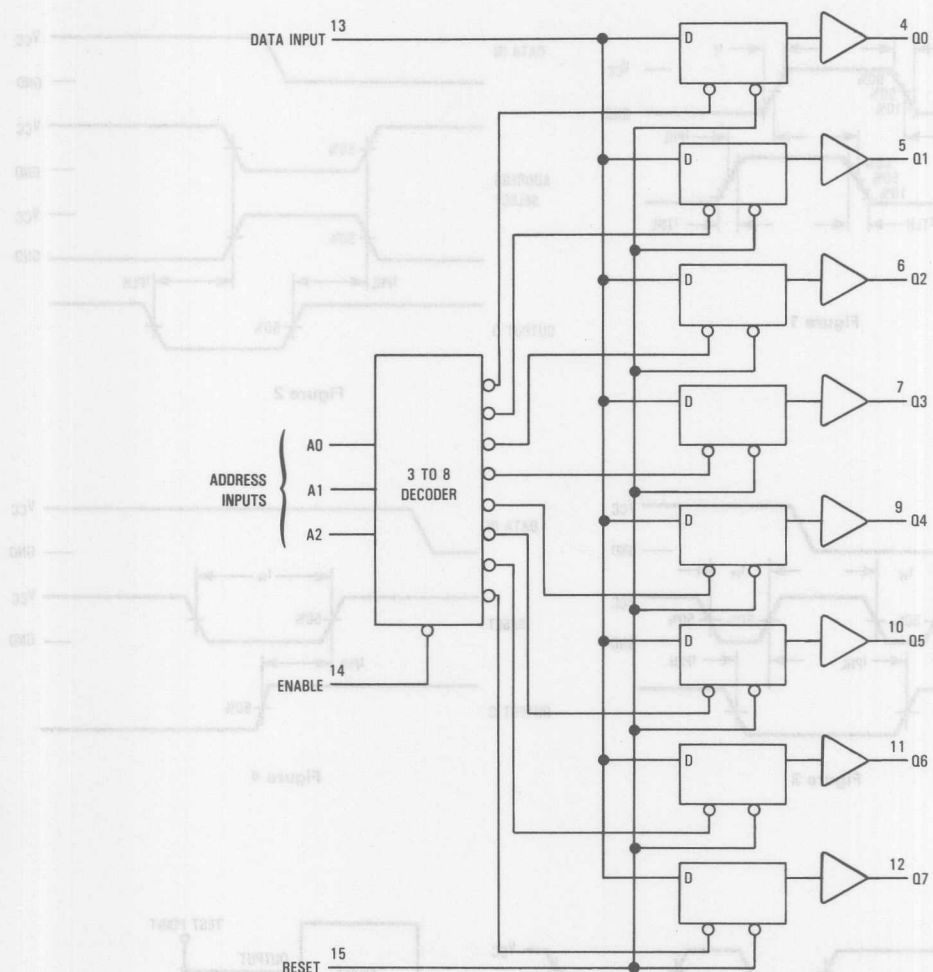


Figure 5



*Includes all probe and jig capacitance.

Figure 6. Test Circuit



MC54/74HC266

Quad 2-Input Exclusive NOR Gate with Open-Drain Outputs High-Performance Silicon-Gate CMOS

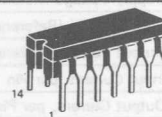
The MC54/74HC266 is identical in pinout to the LS266. The HC266 inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC266 output is a high-performance MOS N-Channel FET. Therefore, with suitable output pullup resistors, this gate can be used in wired AND applications. Using the output characteristic curves in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

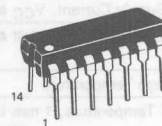
To comply with JEDEC Standard No. 7A, Motorola's HC266 manufactured after the date code 8547 has open-drain outputs. HC266 prior to the date code 8547 has standard CMOS outputs. (See Figure 4 for date code identifier.)

For applications requiring Standard CMOS outputs, use the HC7266.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 52 FETs or 13 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



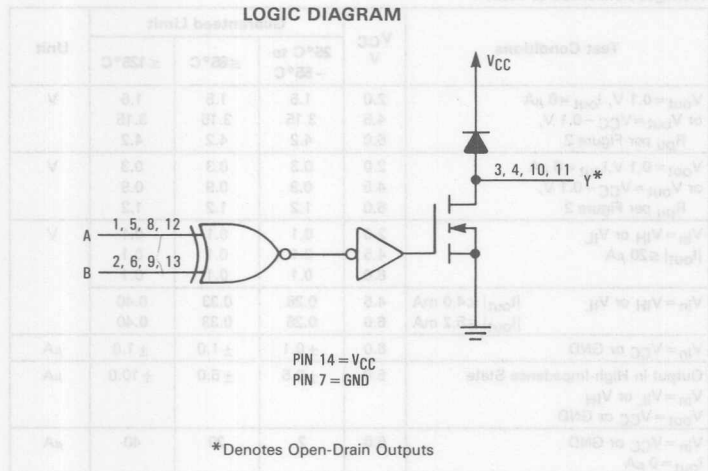
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	B4
Y1	3	12	A4
Y2	4	11	Y4
A2	5	10	Y3
B2	6	9	B3
GND	7	8	A3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	Z
L	H	L
H	L	L
H	H	Z

Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	−55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V 0 V _{CC} = 4.5 V 0 V _{CC} = 6.0 V 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$, $I_{out} = 0 \mu\text{A}$ or $V_{out} = V_{CC} - 0.1 \text{ V}$, R_{pu} per Figure 2	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$, $I_{out} = 0 \mu\text{A}$ or $V_{out} = V_{CC} - 0.1 \text{ V}$, R_{pu} per Figure 2	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC266

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLZ} , t_{PZL}	Maximum Propagation Delay, (Figures 1 and 2)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		11	

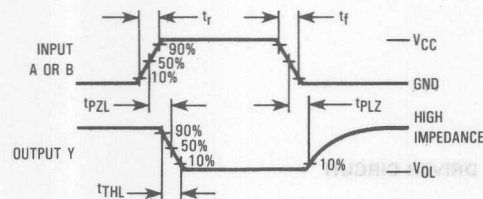
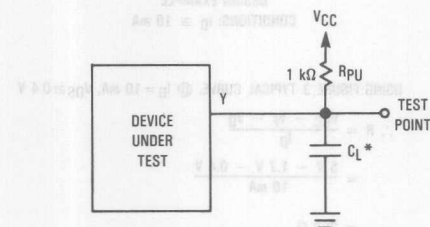
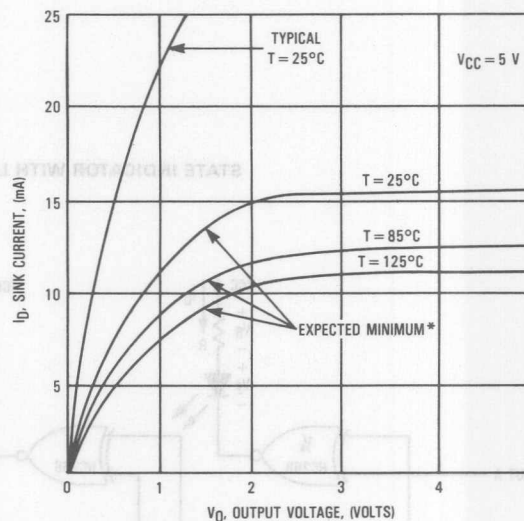


Figure 1. Switching Waveforms



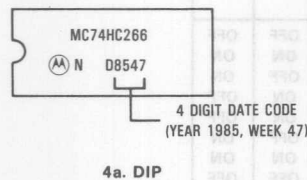
*Includes all probe and jig capacitance.

Figure 2. Test Circuit

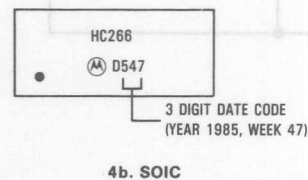


*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics



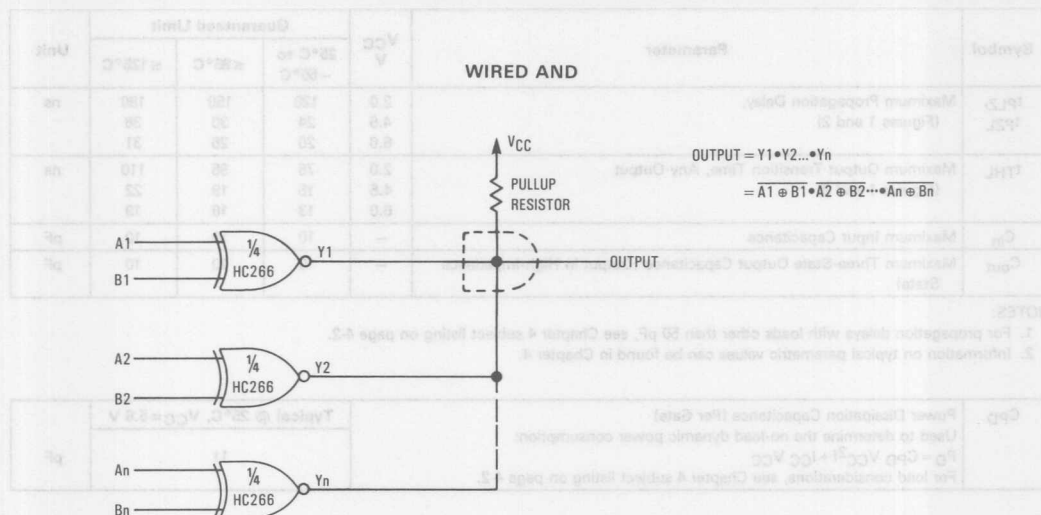
4a. DIP



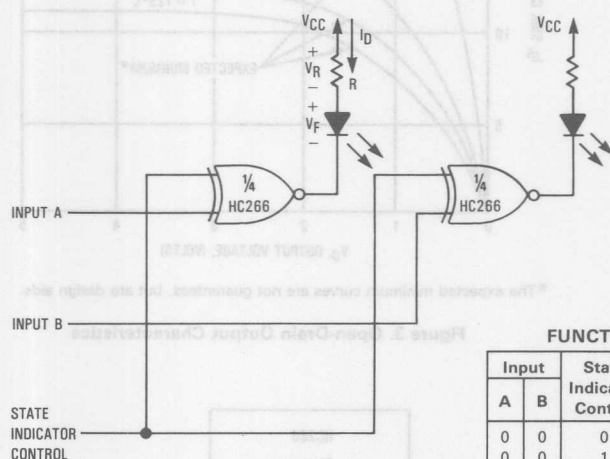
4b. SOIC

Figure 4. Date Code Identifier

WIRED AND



STATE INDICATOR WITH LED DRIVER CIRCUIT



DESIGN EXAMPLE
 CONDITIONS: $I_D \approx 10 \text{ mA}$

USING FIGURE 3 TYPICAL CURVE, @ $I_D = 10 \text{ mA}$, $V_{DS} \approx 0.4 \text{ V}$

$$R = \frac{V_{CC} - V_F - V_D}{I_D}$$

$$= \frac{5 \text{ V} - 1.7 \text{ V} - 0.4 \text{ V}}{10 \text{ mA}}$$

$$= 290 \Omega$$

Use $R = 270 \Omega$

FUNCTION TABLE

Input		State Indicator Control	LED 1	LED 2
A	B			
0	0	0	OFF	OFF
0	0	1	ON	ON
0	1	0	OFF	ON
0	1	1	ON	OFF
1	0	0	ON	OFF
1	0	1	OFF	ON
1	1	0	ON	ON
1	1	1	OFF	OFF

MC54/74HC273

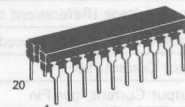
Octal D Flip-Flop with Common Clock and Reset

High-Performance Silicon-Gate CMOS

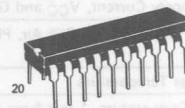
The MC54/74HC273 is identical in pinout to the LS273. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The device consists of eight D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



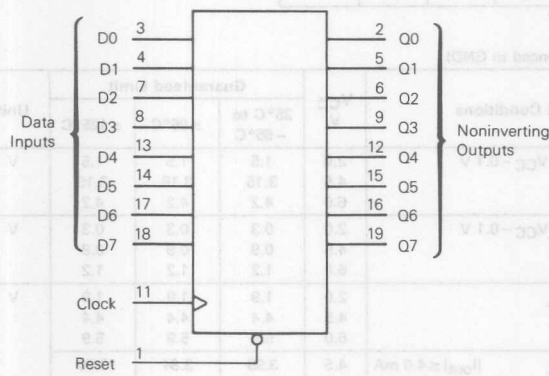
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Reset	1	20	V_{CC}
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	Clock

FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	X	H	H
H	X	L	L
H	L	X	no change
H	X	X	no change

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC273

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		38	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

FIGURE 1

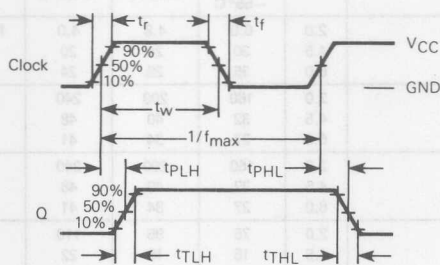


FIGURE 2

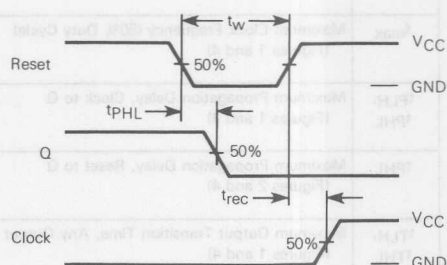


FIGURE 3

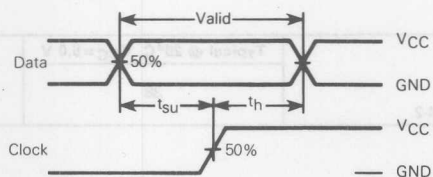
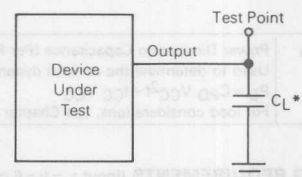


FIGURE 4 - TEST CIRCUIT



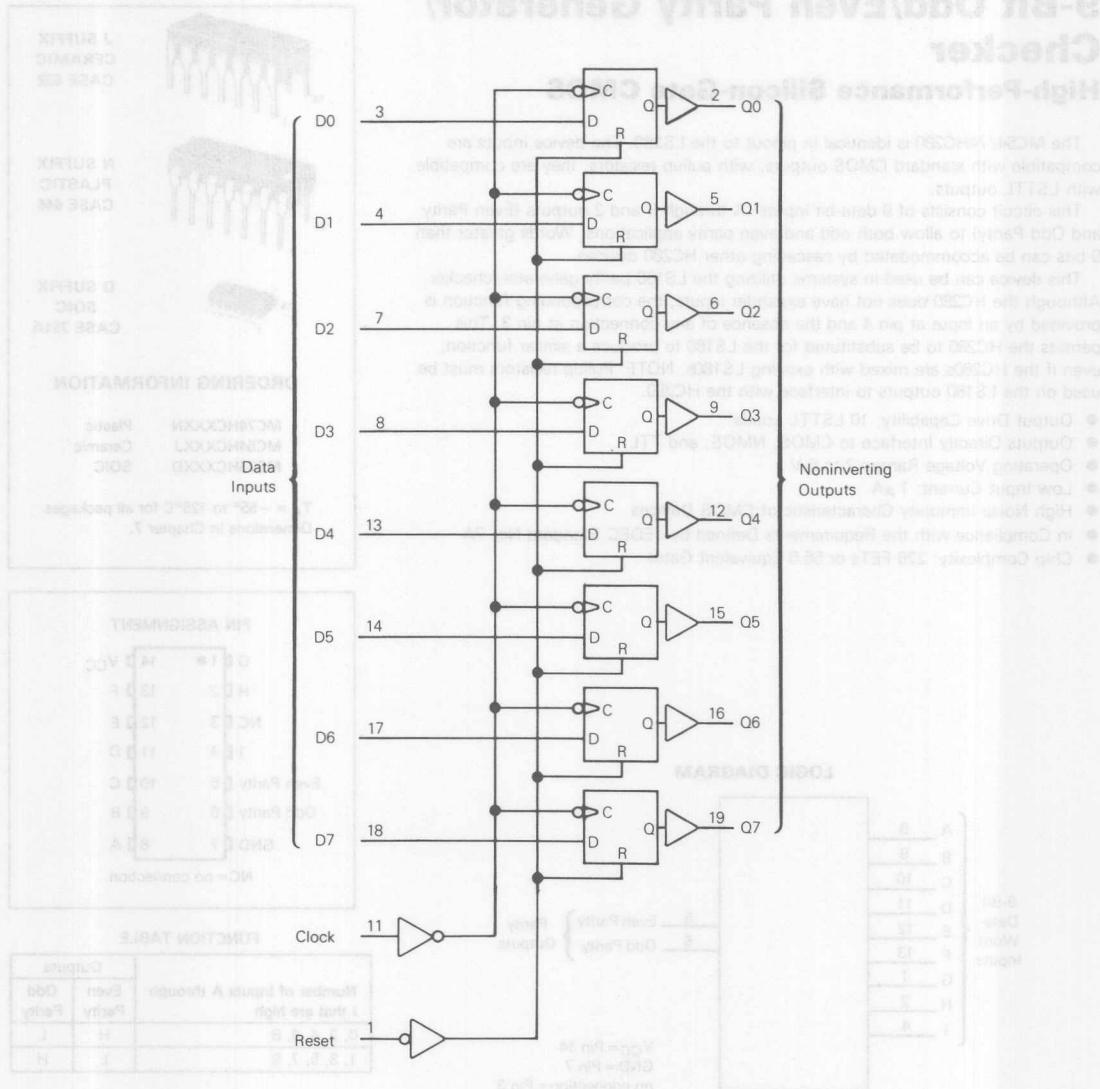
*Includes all probe and jig capacitance.

Symbol	Parameter	VCC = 5.0 V, TA = 25°C	VCC = 3.0 V, TA = 25°C	VCC = 1.8 V, TA = 25°C	Unit
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	10	10	10	ns
t _h	Minimum Hold Time, Clock to Data (Figure 3)	10	10	10	ns
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	10	10	10	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	10	10	10	ns
t _{PLH}	Minimum Pulse Width, High (Figure 2)	10	10	10	ns
t _{PLH}	Minimum Pulse Width, Low (Figure 2)	10	10	10	ns

NOTE: Information on typical parameter values can be found in Chapter 4 subject listing on page 4-5.

MC54/74HC273

EXPANDED LOGIC DIAGRAM



9-Bit Odd/Even Parity Generator/Checker

High-Performance Silicon-Gate CMOS

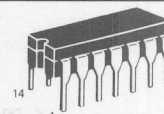
The MC54/74HC280 is identical in pinout to the LS280. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This circuit consists of 9 data-bit inputs (A through I) and 2 outputs (Even Parity and Odd Parity) to allow both odd and even parity applications. Words greater than 9-bits can be accommodated by cascading other HC280 devices.

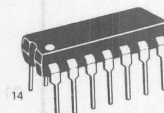
This device can be used in systems utilizing the LS180 parity generator/checker. Although the HC280 does not have expander inputs, the corresponding function is provided by an input at pin 4 and the absence of any connection at pin 3. This permits the HC280 to be substituted for the LS180 to produce a similar function, even if the HC280s are mixed with existing LS180s. NOTE: Pullup resistors must be used on the LS180 outputs to interface with the HC280.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 226 FETs or 56.5 Equivalent Gates

MC54/74HC280



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



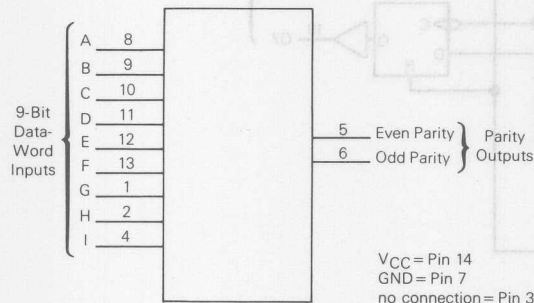
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

G	1	14	V_{CC}
H	2	13	F
NC	3	12	E
I	4	11	D
Even Parity	5	10	C
Odd Parity	6	9	B
GND	7	8	A
NC = no connection			

FUNCTION TABLE

Number of Inputs A through I that are high	Outputs	
	Even Parity	Odd Parity
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

MC54/74HC280

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Data Inputs to Parity Outputs (Figures 1 and 2)	2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		60	

PIN DESCRIPTIONS

INPUTS

A, B, C, D, E, F, G, H, I (Pins 8-13, 1, 2, 4) — Nine-bit data-word inputs. The data word placed on these pins is checked for even or odd parity.

OUTPUTS

Even Parity (Pin 5) — Even-parity output. This pin goes high if the data word has even parity and low if the data word has odd parity.

Odd Parity (Pin 6) — Odd-parity output. This pin goes high if the data word has odd parity and low if the data word has even parity.

FIGURE 1 — SWITCHING WAVEFORMS

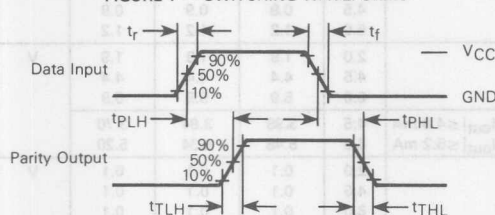
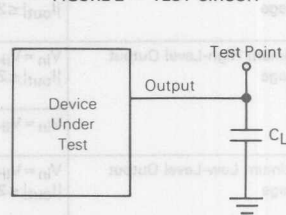
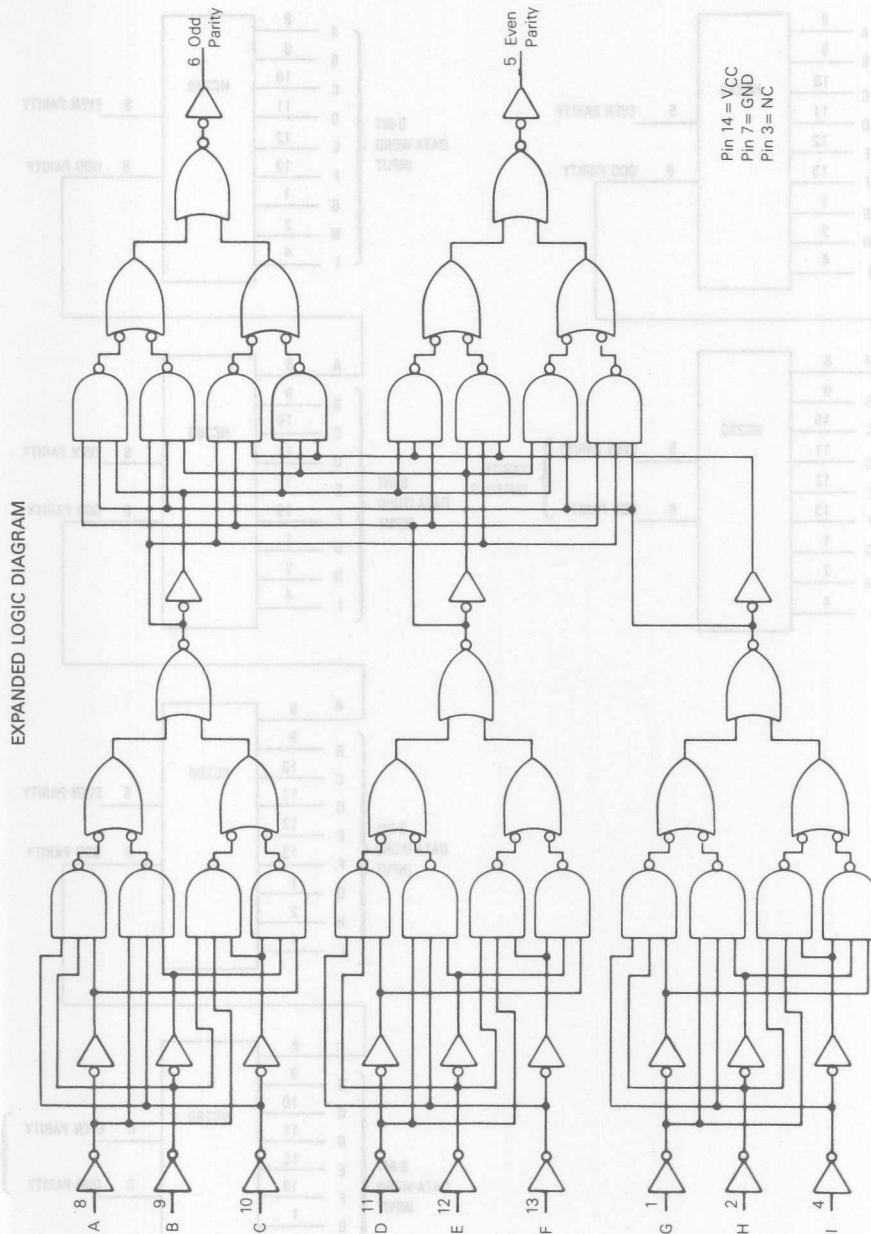


FIGURE 2 — TEST CIRCUIT



* Includes all probe and jig capacitance.

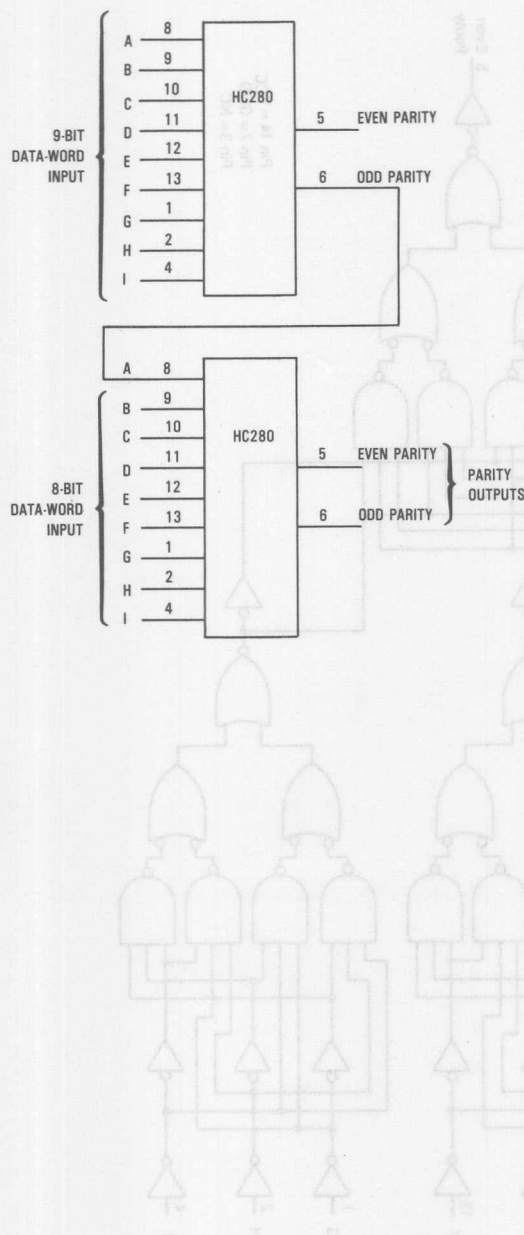
MC54/74HC280



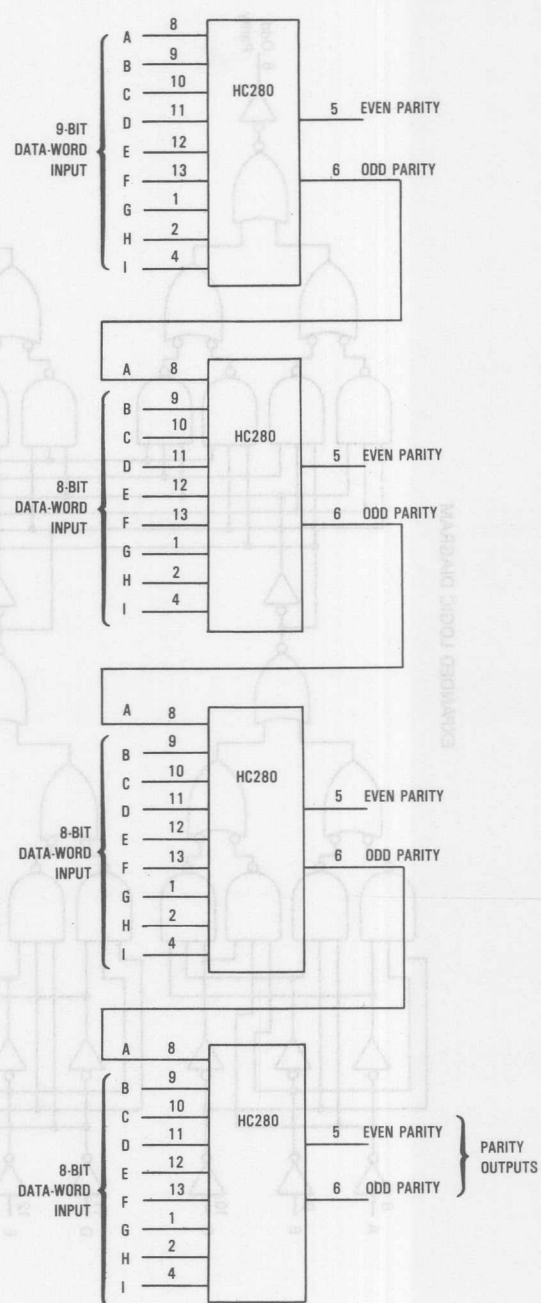
MC54/74HC280

TYPICAL APPLICATIONS

CASCADED 17-BIT ODD/EVEN PARITY
GENERATOR/CHECKER



CASCADED 33-BIT ODD/EVEN PARITY
GENERATOR/CHECKER



Product Preview

4-Bit Binary Full Adder with Fast Carry

High-Performance Silicon-Gate CMOS

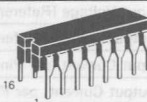
The MC54/74HC283 is identical in pinout to the LS283. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC283 is a high-speed 4-bit binary Full Adder with internal carry lookahead. The device adds two 4-bit words (A and B) plus the Carry-In bit. The binary sum appears at the Sum outputs (S), and any resulting carries appear at the Carry-Out pin.

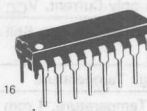
Because of the symmetry of the binary add function, the HC283 can be used either with all inputs and outputs active-high (positive logic), or with all inputs and outputs active-low (negative logic). With active-high inputs, Carry In must be held low when no carry-in is intended.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 212 FETs or 53 Equivalent Gates

MC54/74HC283



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



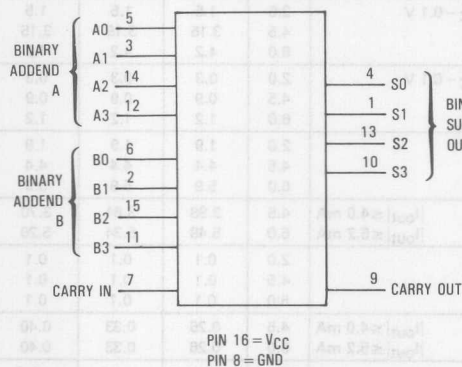
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN Plastic
MC54HCXXXJ Ceramic
MC74HCXXXD SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

S1	1	16	V_{CC}
B1	2	15	B2
A1	3	14	A2
S0	4	13	S2
A0	5	12	A3
B0	6	11	B3
CARRY IN	7	10	S3
GND	8	9	CARRY OUT

FUNCTION TABLE

Inputs			Outputs	
A_n	B_n	$C_n = C_{n-1}$	S_n	$C_{n+1} = C_n + 1$
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

$n=0, 1, 2, 3$ (A_3, B_3 , and S_3 are the most significant bits)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0 6.0	3.98 5.48 5.48	3.84 5.34 5.34	3.70 5.20 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC283

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Projected Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Carry In to Sum Out (Figures 1 and 3)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A or B to Sum Out (Figures 1 and 3)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Carry In to Carry Out (Figures 2 and 3)	2.0 4.5 6.0	195 39 33	245 49 42	295 59 50	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A or B to Carry Out (Figures 2 and 3)	2.0 4.5 6.0	225 45 38	280 56 48	340 68 58	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		130	

SWITCHING WAVEFORMS

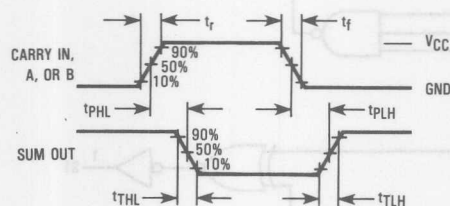


Figure 1

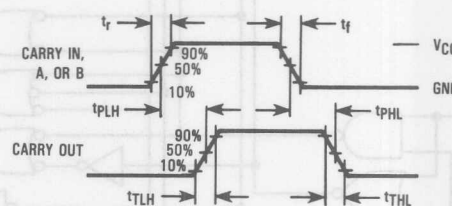
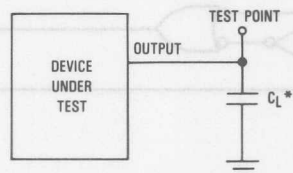


Figure 2

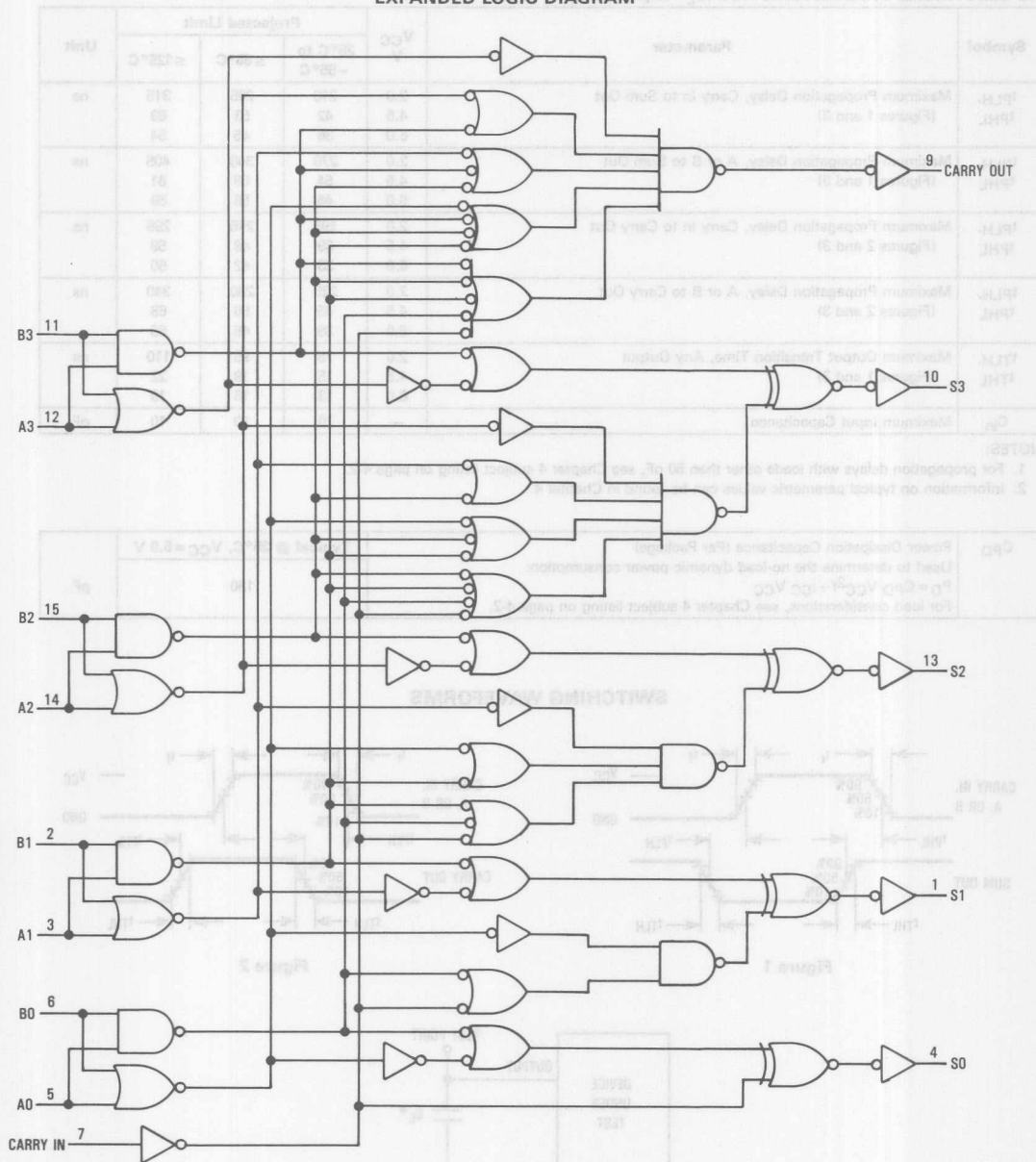


*Includes all probe and jig capacitance.

Figure 3. Test Circuit

MC54/74HC283

EXPANDED LOGIC DIAGRAM



5

MC54/74HC299

Advance Information

8-Bit Bidirectional Universal Shift Register with Parallel I/O

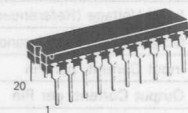
High-Performance Silicon-Gate CMOS

The MC54/74HC299 is identical in pinout to the LS299. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

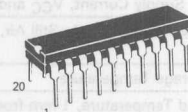
The HC299 features a multiplexed parallel input/output data port to achieve full 8-bit handling in a 20 pin package. Due to the large output drive capability and the 3-state feature, this device is ideally suited for interface with bus lines in a bus-oriented system.

Two Mode-Select inputs and two Output Enable inputs are used to choose the mode of operation as listed in the Function Table. Synchronous parallel loading is accomplished by taking both Mode-Select lines, S₁ and S₂, high. This places the outputs in the high-impedance state, which permits data applied to the data port to be clocked into the register. Reading out of the register can be accomplished when the outputs are enabled. The active-low asynchronous Reset overrides all other inputs.

- Output Drive Capability: 15 LSTTL Loads for Q_A through Q_H
10 LSTTL Loads for Q_{A'} and Q_{H'}
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

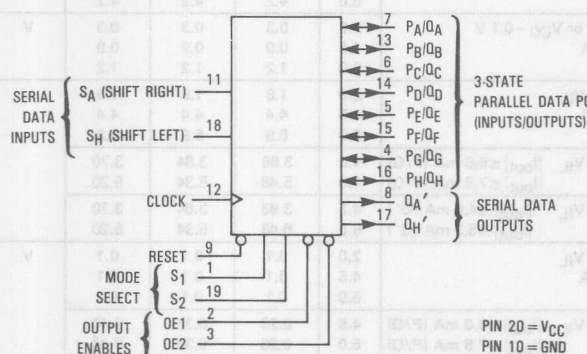
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

S ₁	1	20	V _{CC}
OE1	2	19	S ₂
OE2	3	18	S _H
P _G /Q _G	4	17	Q _{H'}
P _E /Q _E	5	16	P _H /Q _H
P _C /Q _C	6	15	P _F /Q _F
P _A /Q _A	7	14	P _D /Q _D
Q _{A'}	8	13	P _B /Q _B
RESET	9	12	CLOCK
GND	10	11	S _A

LOGIC DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA (P/Q)}$ $ I_{out} \leq 7.8 \text{ mA (P/Q)}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA (Q')}$ $ I_{out} \leq 5.2 \text{ mA (Q')}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA (P/Q)}$ $ I_{out} \leq 7.8 \text{ mA (P/Q)}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA (Q')}$ $ I_{out} \leq 5.2 \text{ mA (Q')}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current (Q_A thru Q_H)	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC299

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q _A ' or Q _H ' (Figures 1 and 5)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q _A thru Q _H (Figures 1 and 5)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q _A ' or Q _H ' (Figures 2 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q _A thru Q _H (Figures 2 and 5)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, OE1, OE2, S1, or S2 to Q _A thru Q _H (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, OE1, OE2, S1, or S2 to Q _A thru Q _H (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A thru Q _H (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A ' or Q _H ' (Figures 1 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q _A thru Q _H	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package), Outputs Enabled Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		240	

MC54/74HC299








TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Mode Select S1 or S2 to Clock (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Data Inputs S _A , S _H , P _A thru P _H to Clock (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Clock to Mode Select S1 or S2 (Figure 4)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_h	Minimum Hold Time, Clock to Data Inputs, S _A , S _H , P _A thru P _H (Figure 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC299

FUNCTION TABLE

Inputs									Response										
Mode	Reset	Mode Select		Output Enables		Clock	Serial Inputs		PA/QA PB/QB PC/QC PD/QD PE/QE PF/QF PG/QG PH/QH								QA' QH'		
		S2	S1	OE1†	OE2†		DA	DH											
Reset	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L		
	L	H	H	X	X	X	X	X	QA through QH = Z								L	L	
Shift Right	H	L	H	H	X		D	X	Shift Right: QA through QH = Z; DA → FA; FA → FB; etc.								D	QG	
	H	L	H	X	H		D	X	Shift Right: QA through QH = Z; DA → FA; FA → FB; etc.								D	QG	
	H	L	H	L	L		D	X	Shift Right: DA → FA = QA; FA → FB = QB; etc.								D	QG	
Shift Left	H	H	L	H	X		X	D	Shift Left: QA through QH = Z; DH → FH; FH → FG; etc.								QB	D	
	H	H	L	X	H		X	D	Shift Left: QA through QH = Z; DH → FH; FH → FG; etc.								QB	D	
	H	H	L	L	L		X	D	Shift Left: DH → FH = QH; FH → FG = QG; etc.								QB	D	
Parallel Load	H	H	H	X	X		X	X	Parallel Load: PN → FN								PA	PH	
Hold	H	L	L	H	X	X	X	X	Hold: QA through QH = Z; FN = FN								PA	PH	
	H	L	L	X	H	X	X	X	Hold: QA through QH = Z; FN = FN								PA	PH	
	H	L	L	L	L	X	X	X	Hold: QN = QN								PA	PH	

Z = high impedance

D = data on serial input

F = flip-flop (see Logic Diagram)

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

PIN DESCRIPTIONS

DATA INPUTS

S_A (PIN 11) — Serial data input (Shift Right). Data on this input is shifted into the shift register on the rising edge of Clock when S₂ is low and S₁ is high (shift right mode).

S_H (PIN 18) — Serial data input (Shift Left). Data on this input is shifted into the shift register on the rising edge of Clock when S₂ is high and S₁ is low (shift left mode).

P_A through P_H (PINS 7, 13, 6, 14, 5, 15, 4, 16) — Parallel data port inputs. Data on these pins can be parallel loaded into the shift register on the rising edge of Clock when both S₁ and S₂ are high. For any other combination of S₁ and S₂, these pins serve as the outputs of the shift register.

CONTROL INPUTS

CLOCK (PIN 12) — Clock input. A low-to-high transition on this pin shifts the data at each stage to the next stage (shift right or left mode) or loads the data at the parallel data inputs into the shift register (parallel load mode).

OE1, OE2 (PINS 2, 3) — Active-low output enables. When both OE1 and OE2 are low, the outputs Q_A through Q_H are enabled. When one or both output enables are high, the outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

RESET (PIN 9) — Active-low reset. A low on this pin resets all stages of the register to a low level. The reset operation is asynchronous.

S₁, S₂ (PINS 1, 19) — Mode select inputs. The levels present at these pins determine the shift register's mode of operation:

S₁ = S₂ = Low. Hold.

S₁ = Low, S₂ = High. Shift left.

S₁ = High, S₂ = Low. Shift right.

S₁ = S₂ = High. Parallel load.

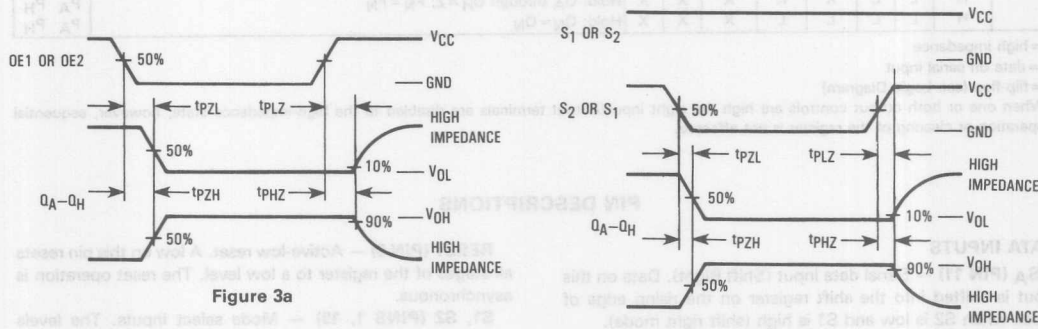
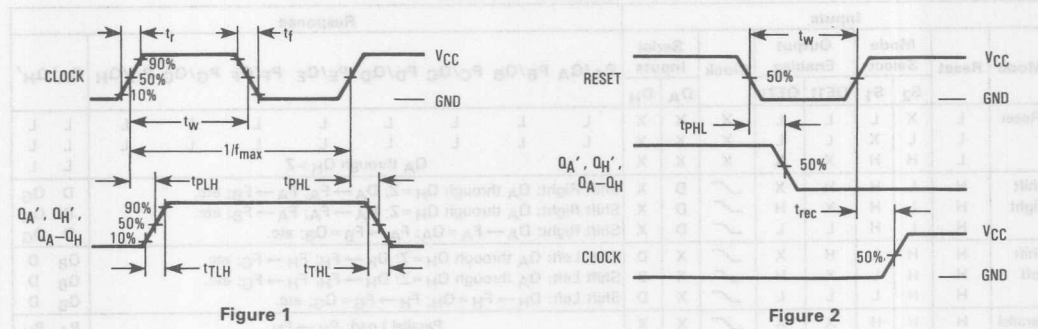
OUTPUTS

Q_A', Q_H' (PINS 8, 17) — Serial data outputs. These are the outputs of the first and last stages of the shift register, respectively. These outputs are not 3-state outputs and have standard drive capabilities.

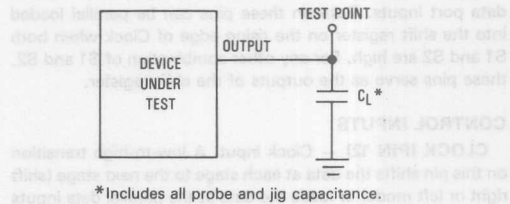
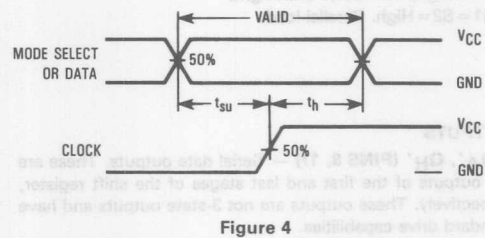
Q_A through Q_H (PINS 7, 13, 6, 14, 5, 15, 4, 16) — Parallel data port outputs. Shifted data is present at these pins when OE1 and OE2 are low. For all other combinations of OE1 and OE2 these outputs are in the high-impedance state.

MC54/74HC299

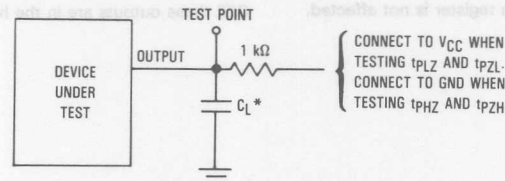
SWITCHING WAVEFORMS



5



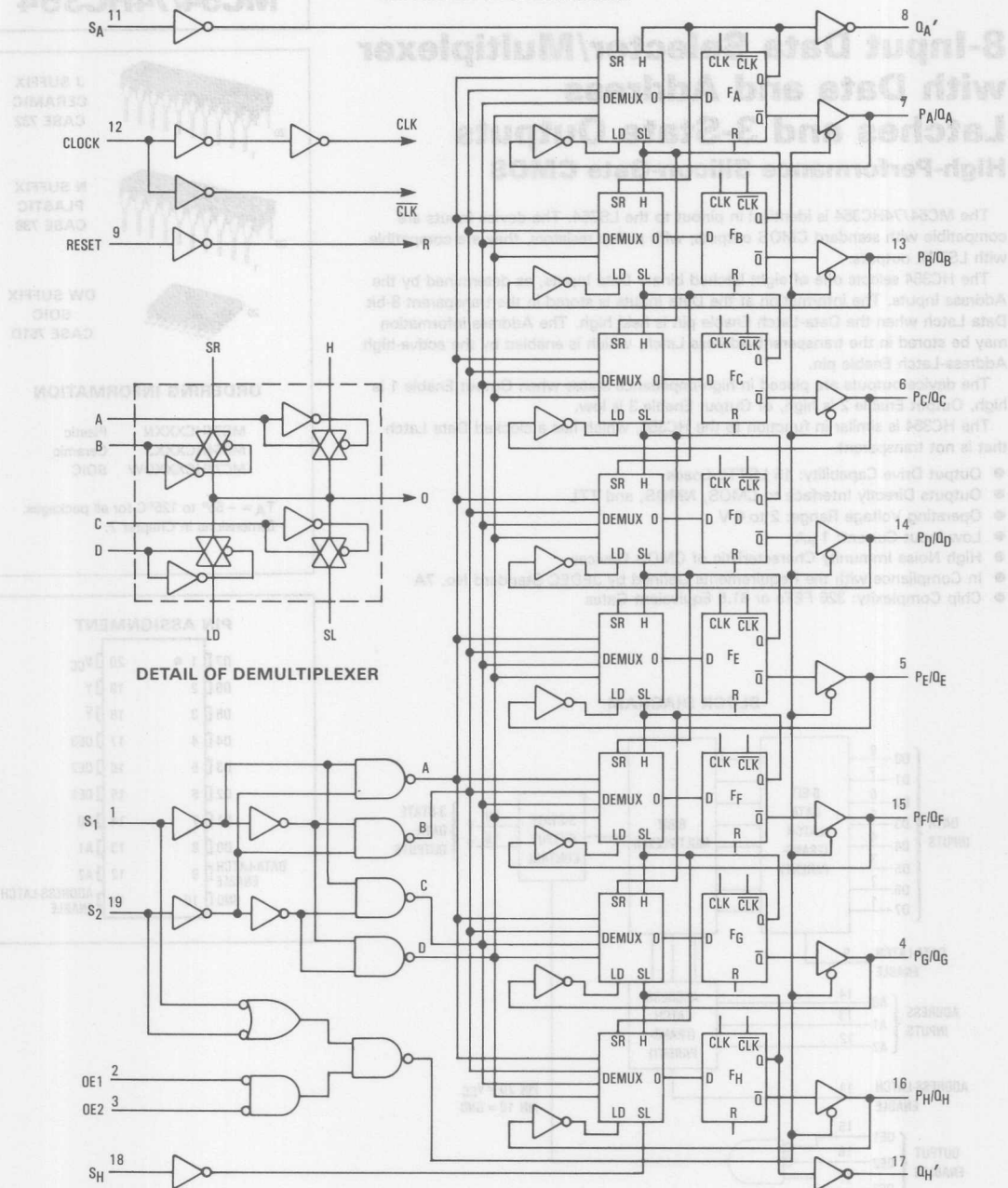
*Includes all probe and jig capacitance.



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC354 is identical in pinout to the LS354. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

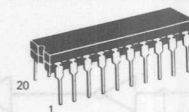
The HC354 selects one of eight latched binary Data Inputs, as determined by the Address Inputs. The information at the Data Inputs is stored in the transparent 8-bit Data Latch when the Data-Latch Enable pin is held high. The Address information may be stored in the transparent Address Latch, which is enabled by the active-high Address-Latch Enable pin.

The device outputs are placed in high-impedance states when Output Enable 1 is high, Output Enable 2 is high, or Output Enable 3 is low.

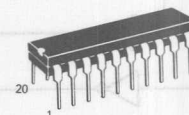
The HC354 is similar in function to the HC356, which has a clocked Data Latch that is not transparent.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 326 FETs or 81.5 Equivalent Gates

MC54/74HC354



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



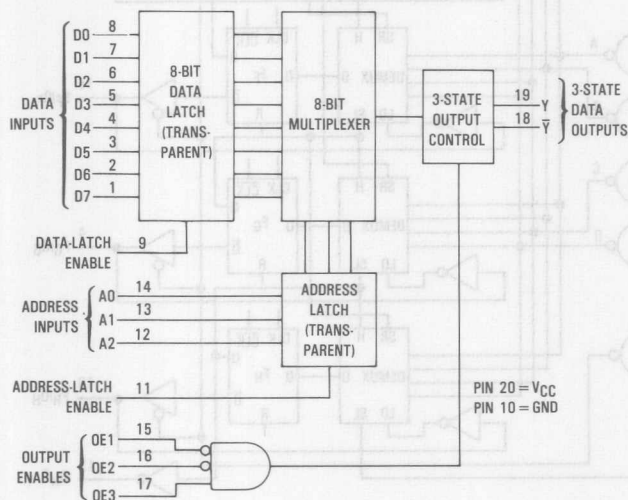
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

BLOCK DIAGRAM



PIN ASSIGNMENT

D7	1	20	V_{CC}
D6	2	19	Y
D5	3	18	\bar{Y}
D4	4	17	OE3
D3	5	16	OE2
D2	6	15	OE1
D1	7	14	A0
D0	8	13	A1
DATA-LATCH ENABLE	9	12	A2
GND	10	11	ADDRESS-LATCH ENABLE

MC54/74HC354

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ 0 $V_{CC} = 4.5 \text{ V}$ 0 $V_{CC} = 6.0 \text{ V}$ 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC354

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, D0-D7 to Y or \bar{Y} (Figures 2 and 6)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Data-Latch Enable to Y or \bar{Y} (Figures 3 and 6)	2.0 4.5 6.0	260 52 44	325 65 55	390 78 66	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A0-A2 to Y or \bar{Y} (Figures 2 and 6)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Address-Latch Enable to Y or \bar{Y} (Figures 3 and 6)	2.0 4.5 6.0	270 54 46	340 68 58	405 81 69	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, OE1-OE3 to Y or \bar{Y} (Figures 4 and 7)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, OE1-OE3 to Y or \bar{Y} (Figures 4 and 7)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		48	

5

PIN DESCRIPTIONS

D0-D7 (PINS 8-1) DATA INPUTS

These eight data bits are stored in a transparent latch when the Data-Latch Enable pin is active (high). Once enabled, changing inputs will not change the contents of the latch.

A0, A1, A2 (Pins 14, 13, 12) ADDRESS INPUTS

Selects which data bit stored in the Data Latch is routed to the outputs Y and \bar{Y} .

DATA-LATCH ENABLE (Pin 9)

The latch is transparent to D0-D7 when enable is inactive (low). The Data-Latch contents are unaffected when enable is held active (high).

ADDRESS-LATCH ENABLE (Pin 11)

The latch is transparent to A0, A1, and A2 when enable is inactive (low). The Address-Latch contents are unaffected when enable is held active (high).

OE1, OE2, OE3 (Pins 15, 16, 17) OUTPUT ENABLES

Any of the output enable pins inactive (OE1=High or OE2=High or OE3=Low) causes the outputs (Y and \bar{Y}) to be in high-impedance states.

Y, \bar{Y} (Pins 19, 18)

These 3-state outputs (when not 3-stated) represent the data bit in the Data Latch selected by the Address Latch.

MC54/74HC354

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, D0-D7 to Data-Latch Enable (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_{su}	Minimum Setup Time, A0-A2 to Address-Latch Enable (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_h	Minimum Hold Time, Data-Latch Enable to D0-D7 (Figure 5)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_h	Minimum Hold Time, Address-Latch Enable to A0-A2 (Figure 5)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_w	Minimum Pulse Width, Data-Latch Enable (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Address-Latch Enable (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

FUNCTION TABLE

Address Latch Contents #			Inputs				Outputs		Description
			Data- Latch Enable	Output Enables			Y	\bar{Y}	
A2	A1	A0		OE1	OE2	OE3			
X	X	X	X	H	X	X	Z	Z	Outputs in high-impedance states
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	L	L	L	H	D0	$\bar{D0}$	Data Latch is transparent
L	L	H	L	L	L	H	D1	$\bar{D1}$	
L	H	L	L	L	L	H	D2	$\bar{D2}$	
L	H	H	L	L	L	H	D3	$\bar{D3}$	
H	L	L	L	L	L	H	D4	$\bar{D4}$	
H	L	H	L	L	L	H	D5	$\bar{D5}$	
H	H	L	L	L	L	H	D6	$\bar{D6}$	
H	H	H	L	L	L	H	D7	$\bar{D7}$	
L	L	L	H	L	L	H	D0 _n	$\bar{D0}_n$	New data is stored in Data Latch and is not alterable
L	L	H	H	L	L	H	D1 _n	$\bar{D1}_n$	
L	H	L	H	L	L	H	D2 _n	$\bar{D2}_n$	
L	H	H	H	L	L	H	D3 _n	$\bar{D3}_n$	
H	L	L	L	L	L	H	D4 _n	$\bar{D4}_n$	
H	L	H	H	L	L	H	D5 _n	$\bar{D5}_n$	
H	H	L	H	L	L	H	D6 _n	$\bar{D6}_n$	
H	H	H	H	L	L	H	D7 _n	$\bar{D7}_n$	

Represents bits in the Address Latch. See Address-Latch Enable pin description.

X = don't care

Z = high impedance

D0-D7 = the data at inputs D0 through D7

D0_n-D7_n = the data present at inputs D0 through D7 when the Data-Latch Enable pin was taken high.

MC54/74HC354

SWITCHING WAVEFORMS

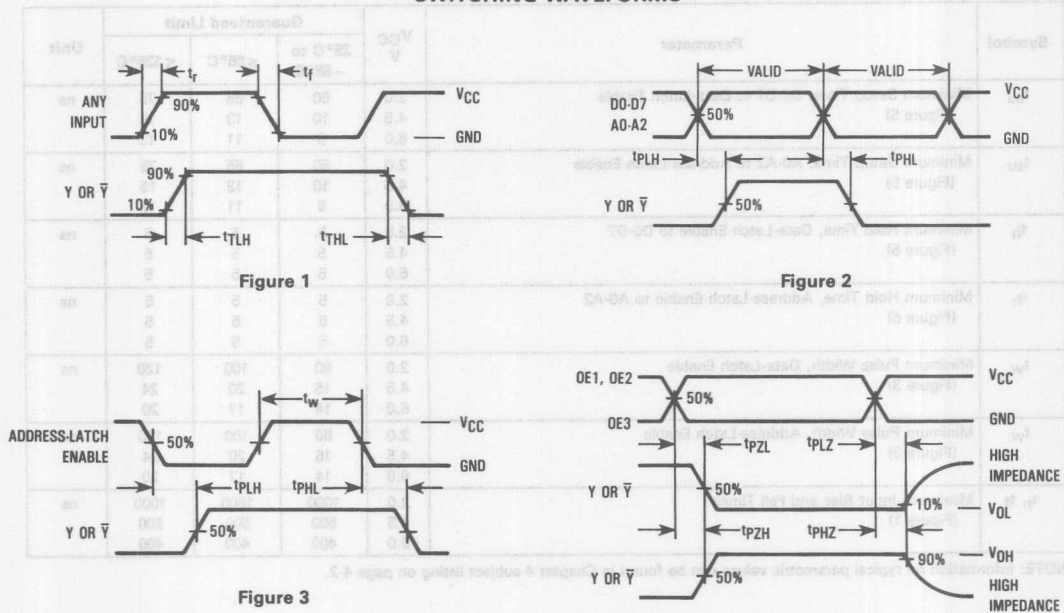


Figure 1

Figure 2

Figure 3

Figure 4

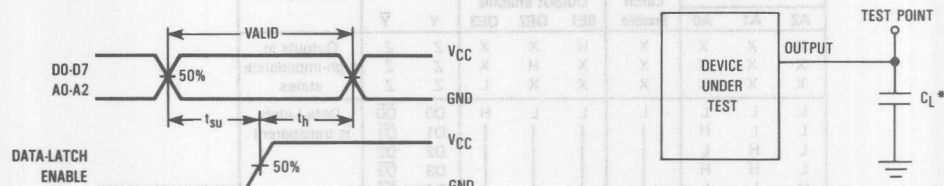
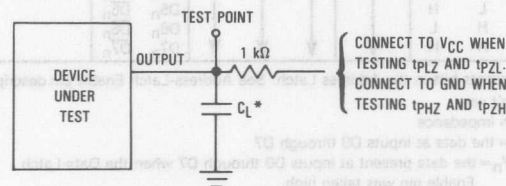


Figure 5

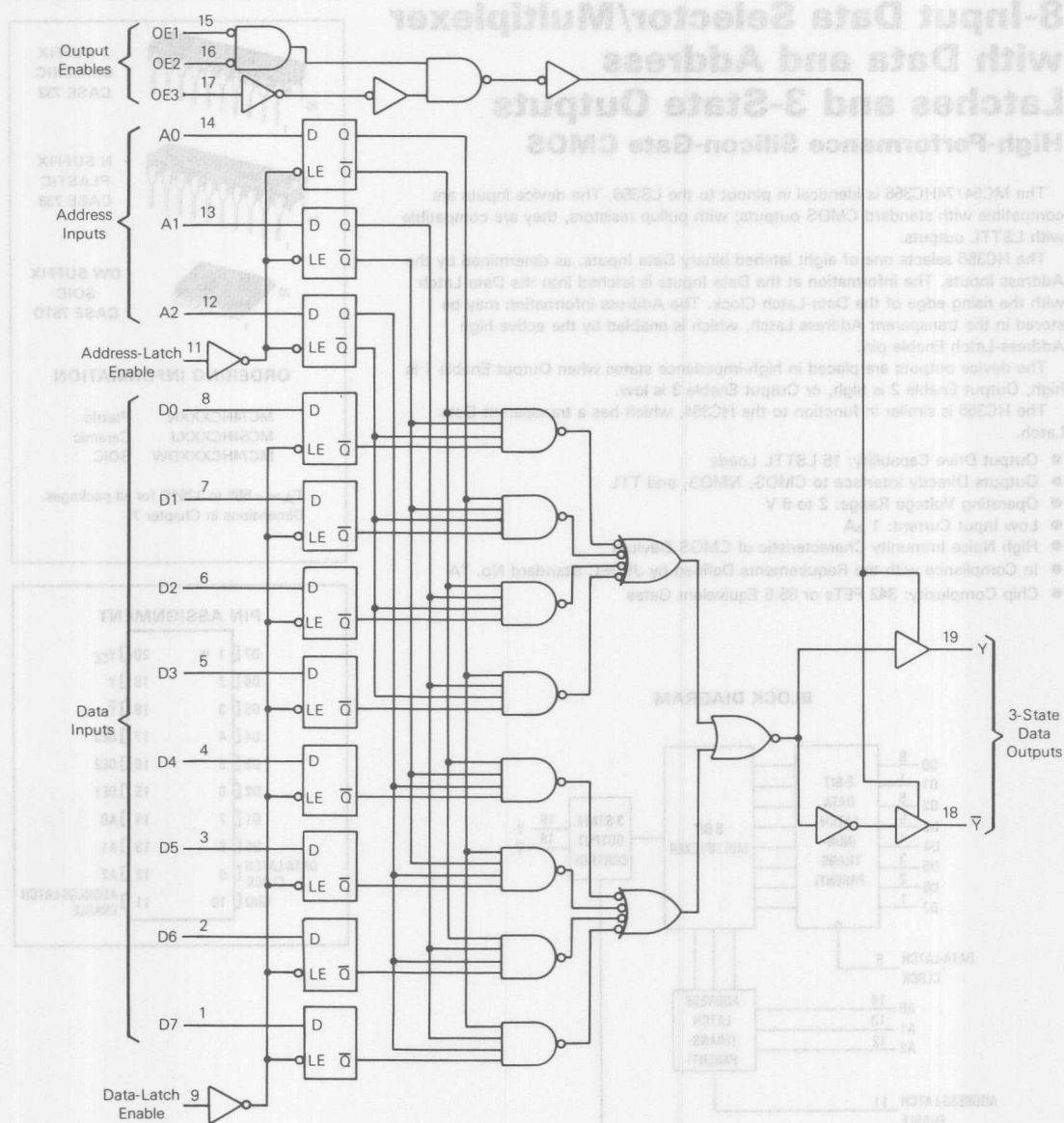
Figure 6. Test Circuit



*Includes all probe and jig capacitance.

Figure 7. Test Circuit

EXPANDED LOGIC DIAGRAM



8-Input Data Selector/Multiplexer with Data and Address Latches and 3-State Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC356 is identical in pinout to the LS356. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

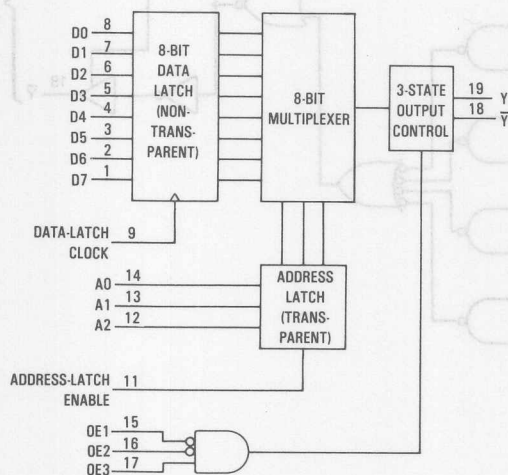
The HC356 selects one of eight latched binary Data Inputs, as determined by the Address Inputs. The information at the Data Inputs is latched into the Data Latch with the rising edge of the Data-Latch Clock. The Address information may be stored in the transparent Address Latch, which is enabled by the active-high Address-Latch Enable pin.

The device outputs are placed in high-impedance states when Output Enable 1 is high, Output Enable 2 is high, or Output Enable 3 is low.

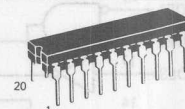
The HC356 is similar in function to the HC354, which has a transparent Data Latch.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 342 FETs or 85.5 Equivalent Gates

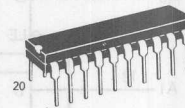
BLOCK DIAGRAM



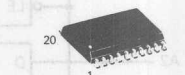
MC54/74HC356



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

D7	1	20	V _{CC}
D6	2	19	Y
D5	3	18	Y-bar
D4	4	17	OE3
D3	5	16	OE2
D2	6	15	OE1
D1	7	14	A0
D0	8	13	A1
DATA-LATCH CLOCK	9	12	A2
GND	10	11	ADDRESS-LATCH ENABLE

MC54/74HC356

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400 ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC356

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Data-Latch Clock to Y or \bar{Y} (Figures 1 and 7)	2.0	240	300	360	ns
		4.5	48	60	72	
		6.0	41	51	61	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A0-A2 to Y or \bar{Y} (Figures 2 and 7)	2.0	270	340	405	ns
		4.5	54	68	81	
		6.0	46	58	69	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Address-Latch Enable to Y or \bar{Y} (Figures 3 and 7)	2.0	270	340	405	ns
		4.5	54	68	81	
		6.0	46	58	69	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, OE1-OE3 to Y or \bar{Y} (Figures 4 and 8)	2.0	160	200	240	ns
		4.5	32	40	48	
		6.0	27	34	41	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, OE1-OE3 to Y or \bar{Y} (Figures 4 and 8)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 7)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		48	

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, D0-D7 to Data-Latch Clock (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _{su}	Minimum Setup Time, A0-A2 to Address-Latch Enable (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _h	Minimum Hold Time, Data-Latch Clock to D0-D7 (Figure 5)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _h	Minimum Hold Time, Address-Latch Enable to A0-A2 (Figure 6)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Data-Latch Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Address-Latch Enable (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC356

FUNCTION TABLE

Inputs							Outputs		Description
Address Latch Contents *			Data-Latch Clock	Output Enables			Y	Y̅	
A2	A1	A0		OE1	OE2	OE3			
X	X	X	X	H	X	X	Z	Z	Outputs in high-impedance states
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	↗	L	L	H	D _{0n}	D̅ _{0n}	New data is clocked into Data Latch
L	L	H	↓	L	L	H	D _{1n}	D̅ _{1n}	
L	H	L	↓	L	L	H	D _{2n}	D̅ _{2n}	
L	H	H	↓	L	L	H	D _{3n}	D̅ _{3n}	
H	L	L	↓	L	L	H	D _{4n}	D̅ _{4n}	
H	L	H	↓	L	L	H	D _{5n}	D̅ _{5n}	
H	H	L	↓	L	L	H	D _{6n}	D̅ _{6n}	
H	H	H	↓	L	L	H	D _{7n}	D̅ _{7n}	
L	L	L	H, L, or ↗	L	L	H	D̅ _{0p}	D _{0p}	Outputs do not change states. Data Latch contents are not alterable.
L	L	H	↓	L	L	H	D̅ _{1p}	D _{1p}	
L	H	L	↓	L	L	H	D̅ _{2p}	D _{2p}	
L	H	H	↓	L	L	H	D̅ _{3p}	D _{3p}	
H	L	L	↓	L	L	H	D̅ _{4p}	D _{4p}	
H	L	H	↓	L	L	H	D̅ _{5p}	D _{5p}	
H	H	L	↓	L	L	H	D̅ _{6p}	D _{6p}	
H	H	H	↓	L	L	H	D̅ _{7p}	D _{7p}	

* Represents bits in the Address Latch. See Address-Latch Enable pin description.

X = don't care

Z = high impedance

D0_n-D7_n = the data present at inputs D0 through D7 when the Data-Latch Clock made the transition from low to high.

D0_p-D7_p = the data previously latched into the Data Latch by the low-to-high transition of the Data-Latch Clock

PIN DESCRIPTIONS

D0-D7 (PINS 8-1) — DATA INPUTS

The information at the data inputs is latched into the data latch on the rising edge of the Data-Latch Clock. Changing the data inputs will not change the contents of the latch except on the rising edge of the clock.

A0, A1, A2 (PINS 14, 13, 12) — ADDRESS INPUTS

Selects which data bit stored in the data latch is routed to the outputs Y and \bar{Y} .

DATA-LATCH CLOCK (PIN 9)

The rising edge of the Data-Latch Clock latches the data (D0-D7) into the data latch.

ADDRESS-LATCH ENABLE (PIN 11)

The latch is transparent to inputs A0, A1, and A2 when Enable is inactive (low). The latch contents are unaffected when the Enable is held active (high)

OE1, OE2, OE3 (PINS 15, 16, 17) OUTPUT ENABLES

Any of the output enable pins being inactive (OE1 = high or OE2 = high or OE3 = low) causes the outputs Y and \bar{Y} to be in high-impedance states.

Y, \bar{Y} (PINS 19, 18)

These 3-state outputs, when not 3-stated, represent the data bit in the data latch selected by the address latch.

5

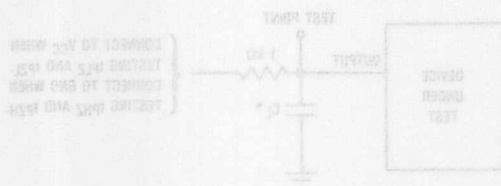


Figure 3: Test Circuit

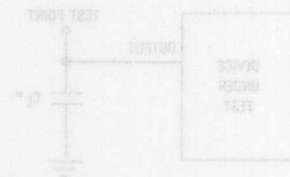


Figure 4: Test Circuit

MC54/74HC356

SWITCHING WAVEFORMS

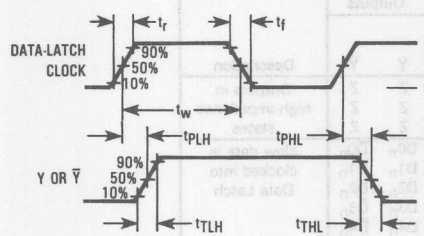


Figure 1

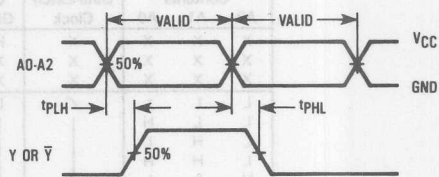


Figure 2

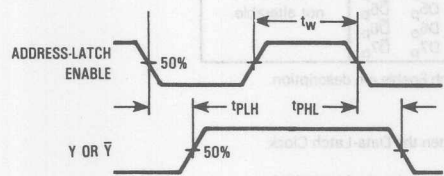


Figure 3

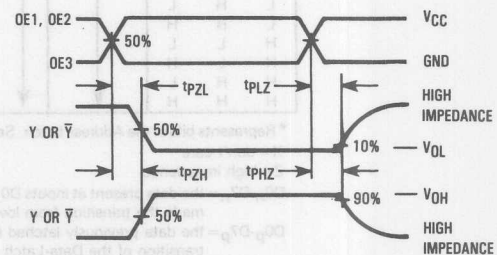


Figure 4

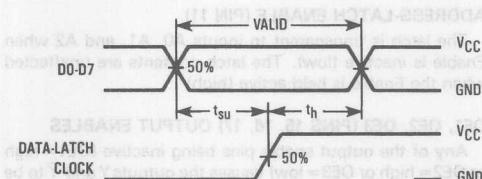


Figure 5

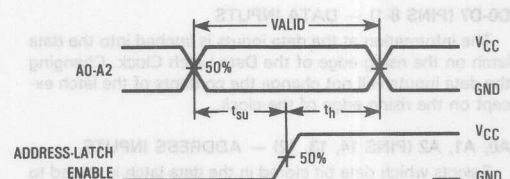
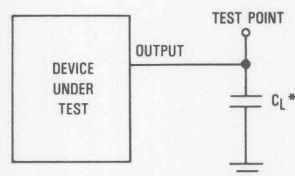
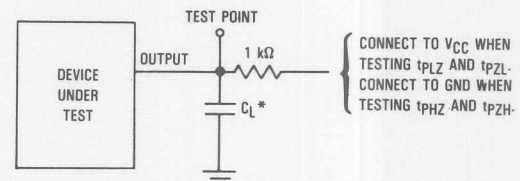


Figure 6



*Includes all probe and jig capacitance.

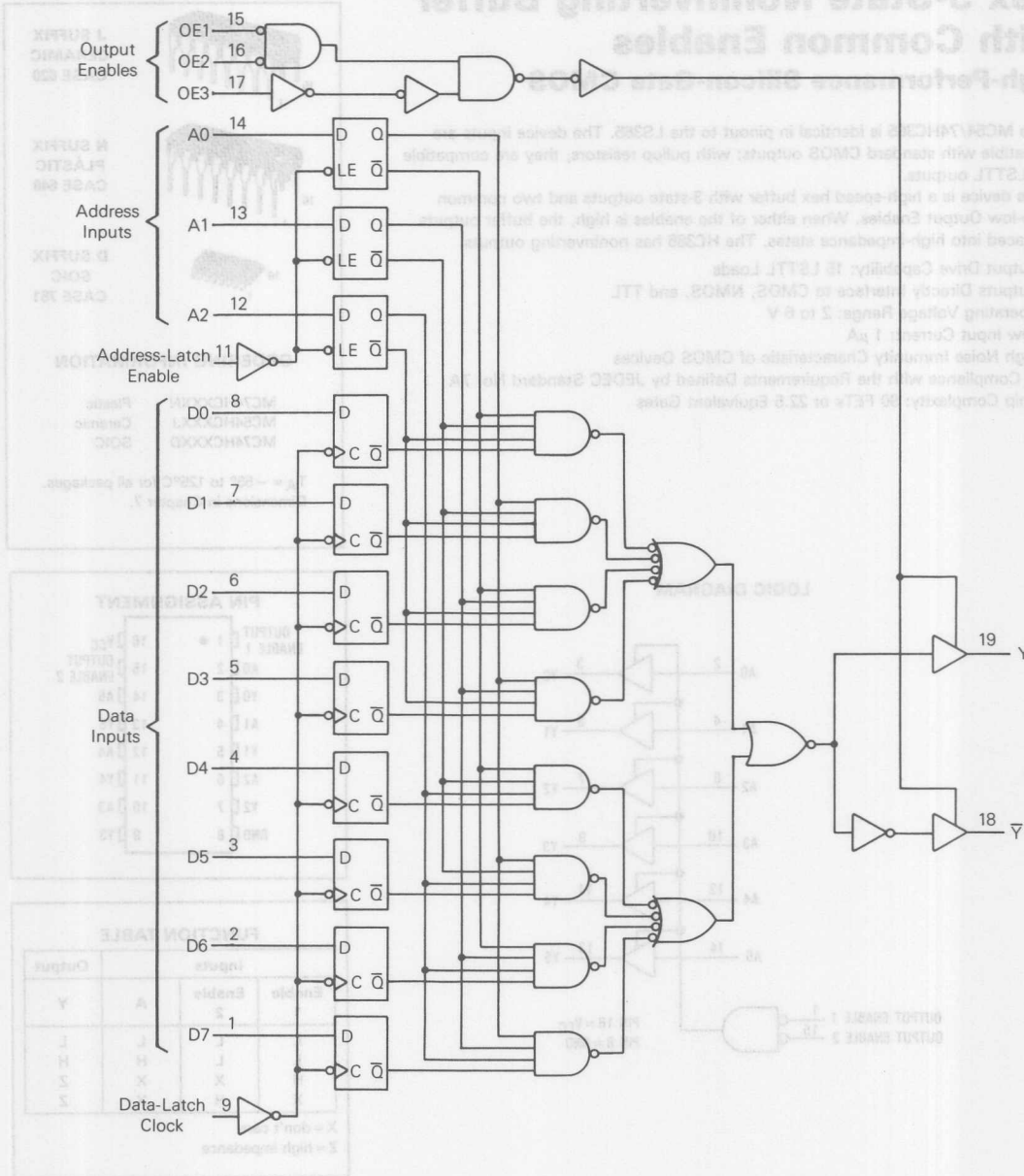
Figure 7. Test Circuit



*Includes all probe and jig capacitance.

Figure 8. Test Circuit

EXPANDED LOGIC DIAGRAM



Hex 3-State Noninverting Buffer with Common Enables

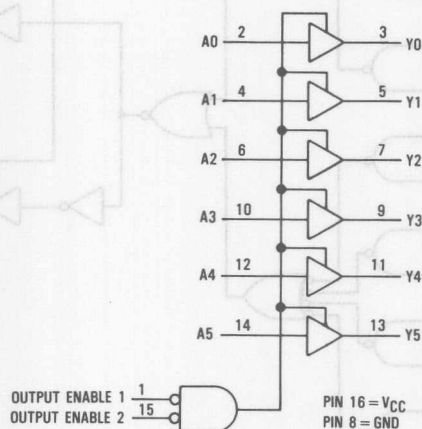
High-Performance Silicon-Gate CMOS

The MC54/74HC365 is identical in pinout to the LS365. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

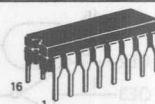
This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC365 has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates

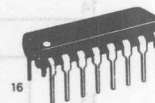
LOGIC DIAGRAM



MC54/74HC365



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

OUTPUT ENABLE 1	1	16	V _{CC}
A0	2	15	OUTPUT ENABLE 2
Y0	3	14	A5
A1	4	13	Y5
Y1	5	12	A4
A2	6	11	Y4
Y2	7	10	A3
GND	8	9	Y3

FUNCTION TABLE

Inputs			Output
Enable 1	Enable 2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

X = don't care
Z = high impedance

MC54/74HC365

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC365

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

SWITCHING WAVEFORMS

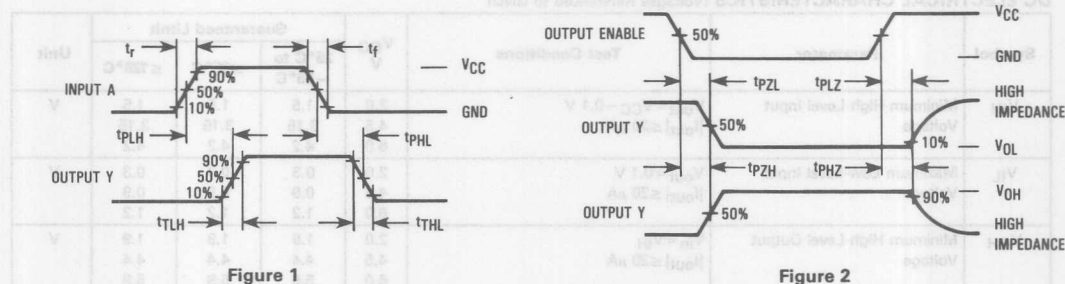
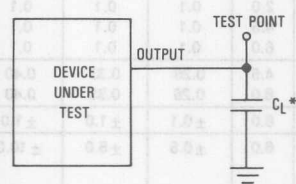


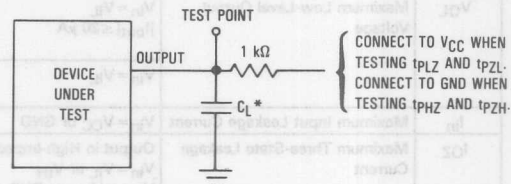
Figure 1

Figure 2



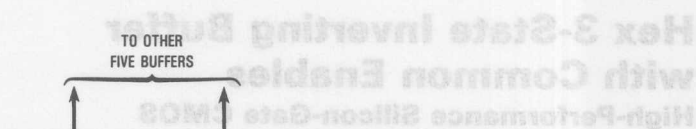
*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit



Hex 3-State Inverting Buffer with Common Enables

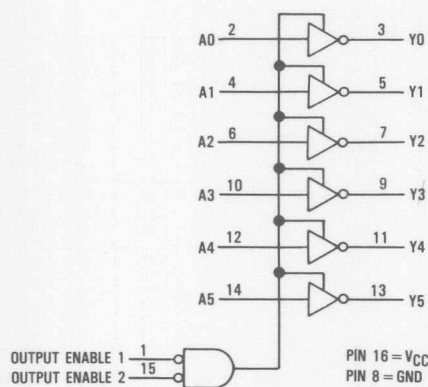
High-Performance Silicon-Gate CMOS

The MC54/74HC366 is identical in pinout to the LS366. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is a high-speed hex buffer with 3-state outputs and two common active-low Output Enables. When either of the enables is high, the buffer outputs are placed into high-impedance states. The HC366 has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 78 FETs or 19.5 Equivalent Gates

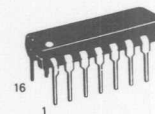
LOGIC DIAGRAM



MC54/74HC366



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



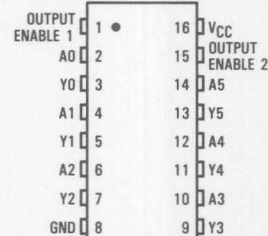
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Enable 1	Enable 2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

X = don't care
Z = high impedance

MC54/74HC366

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ 0 $V_{CC} = 4.5 \text{ V}$ 0 $V_{CC} = 6.0 \text{ V}$ 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC366

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

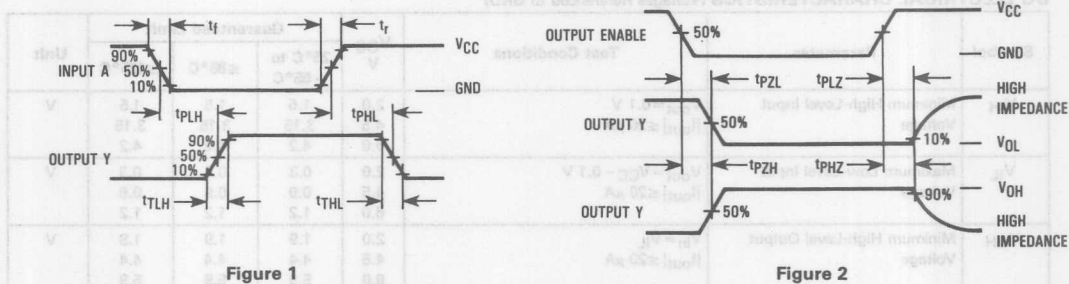
Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

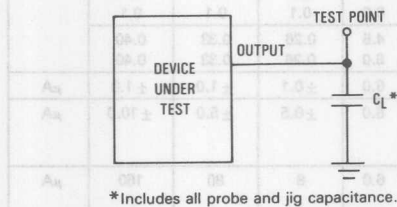
- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		40	pF

SWITCHING WAVEFORMS

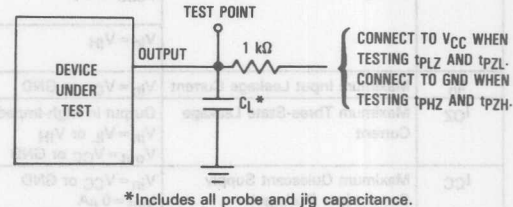


5



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

TO OTHER
FIVE BUFFERS

Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections

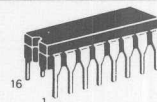
High-Performance Silicon-Gate CMOS

The MC54/74HC367 is identical in pinout to the LS367. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs.

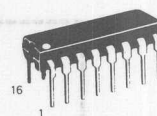
This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC367 has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 92 FETs or 23 Equivalent Gates

MC54/74HC367



J SUFFIX
 CERAMIC
 CASE 620



N SUFFIX
 PLASTIC
 CASE 648



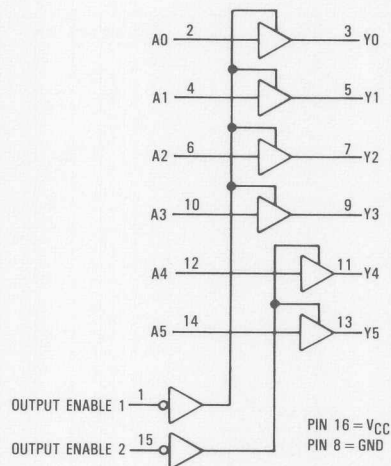
D SUFFIX
 SOIC
 CASE 751

ORDERING INFORMATION

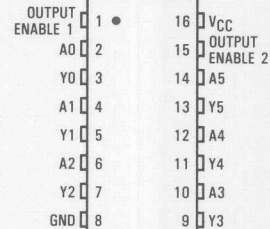
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
Enable 1, Enable 2	A	Y
L	L	L
L	H	H
H	X	Z

X = don't care
 Z = high-impedance

MC54/74HC367

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC367

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		40	

SWITCHING WAVEFORMS

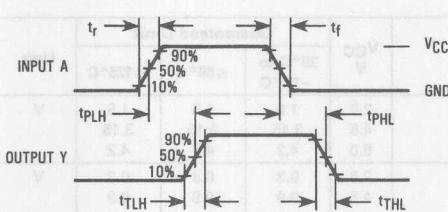


Figure 1

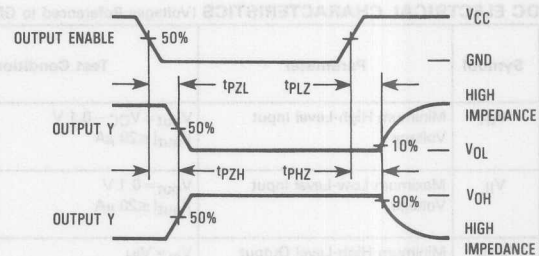
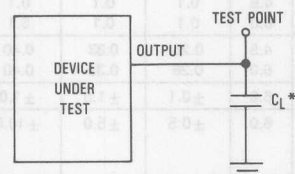
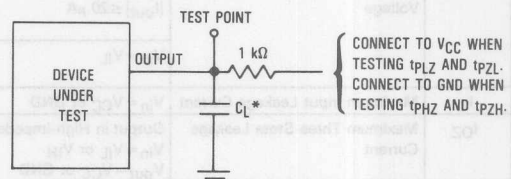


Figure 2



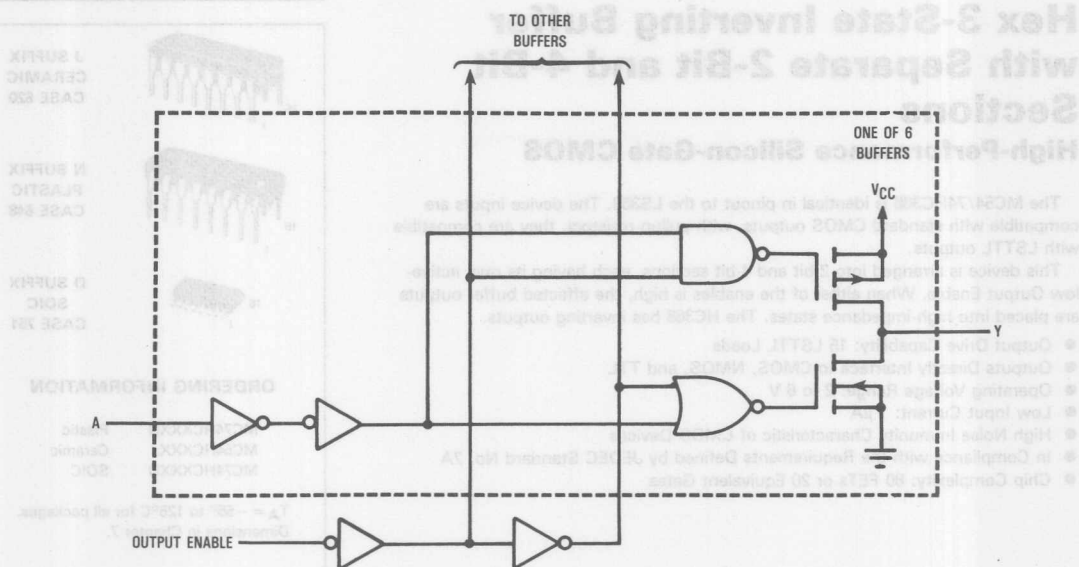
*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit



Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections

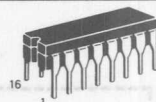
High-Performance Silicon-Gate CMOS

The MC54/74HC368 is identical in pinout to the LS368. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LSTTL outputs.

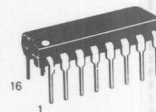
This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC368 has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 80 FETs or 20 Equivalent Gates

MC54/74HC368



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



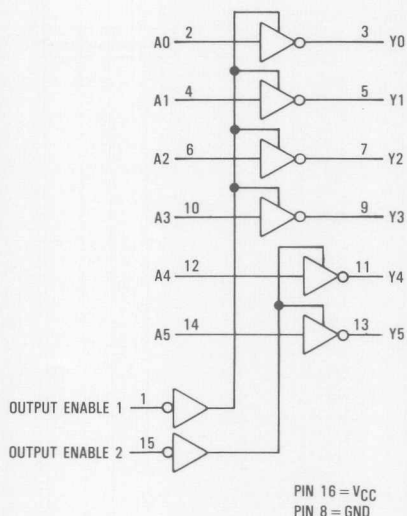
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

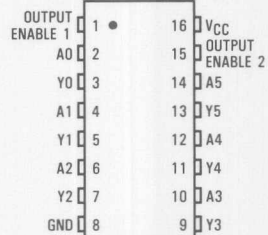
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output	
Enable 1, Enable 2	A	Y	
L	L	H	
L	H	L	
H	X	Z	

X = don't care
Z = high-impedance

MC54/74HC368

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC368

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		40	

SWITCHING WAVEFORMS

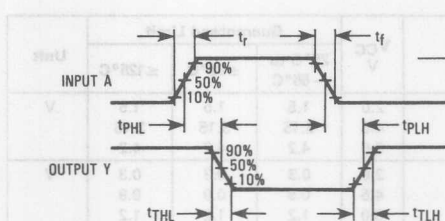


Figure 1

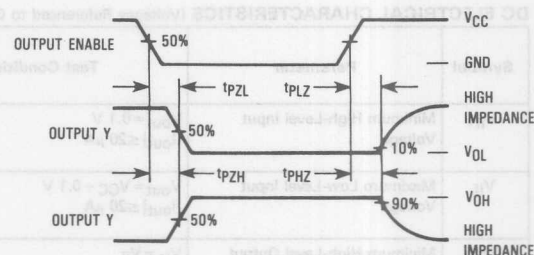
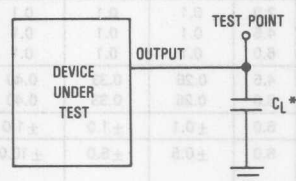
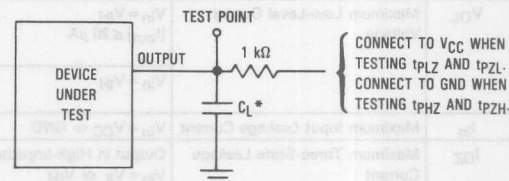


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

Octal 3-State Noninverting Transparent Latch

High-Performance Silicon-Gate CMOS

The MC54/74HC373 is identical in pinout to the LS373. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

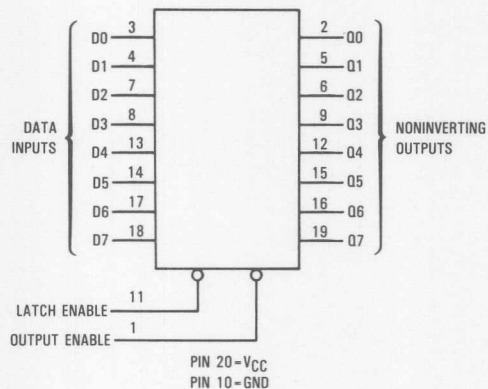
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

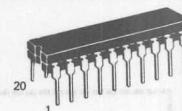
The HC373 is identical in function to the HC573, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC533, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates

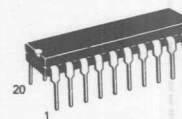
LOGIC DIAGRAM



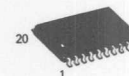
MC54/74HC373



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

OUTPUT ENABLE	1	20	VCC
D0	2	19	Q7
D0	3	18	Q7
D1	4	17	Q6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	Q5
D3	8	13	Q4
Q3	9	12	Q4
GND	10	11	LATCH ENABLE

FUNCTION TABLE

Output Enable	Inputs		Output
	Latch Enable	D	
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MC54/74HC373

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC373

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		41	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t _h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

A ₁	0.1 ±	0.1 ±	0.1 ±	0.1 ±	0.1 ±	0.1 ±
A ₂	0.01 ±	0.01 ±	0.01 ±	0.01 ±	0.01 ±	0.01 ±
A ₃	0.01 ±	0.01 ±	0.01 ±	0.01 ±	0.01 ±	0.01 ±
A ₄	0.01 ±	0.01 ±	0.01 ±	0.01 ±	0.01 ±	0.01 ±

5

SWITCHING WAVEFORMS

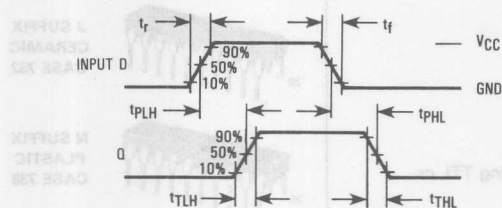


Figure 1

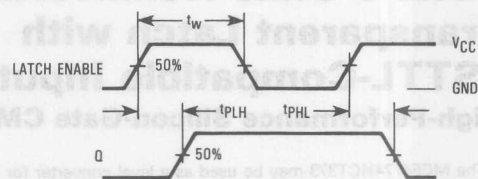


Figure 2

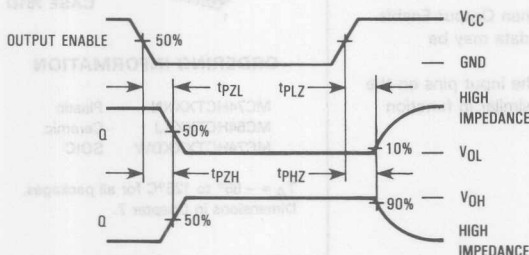


Figure 3

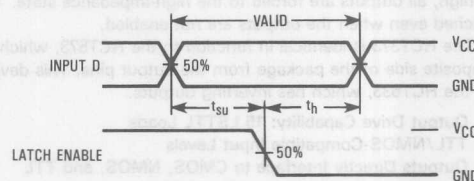
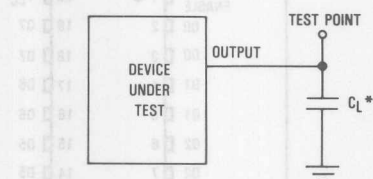
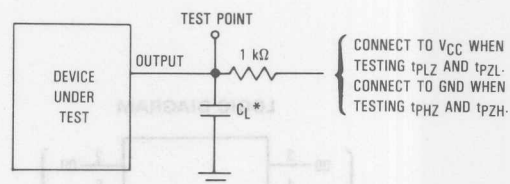


Figure 4



*Includes all probe and jig capacitance.

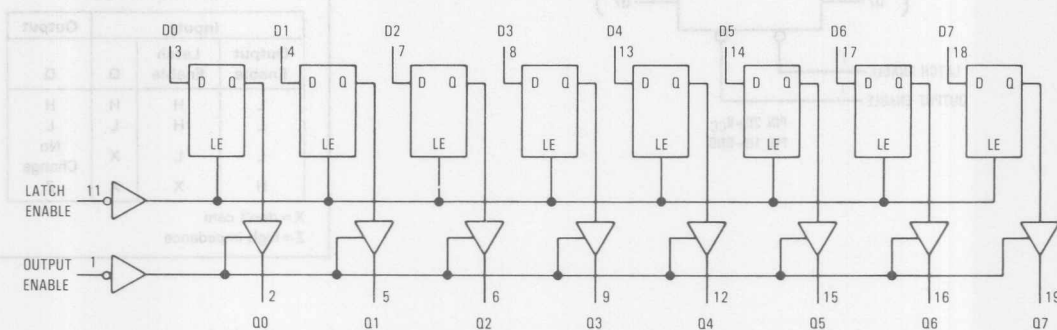
Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT373 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT373 is identical in pinout to the LS373.

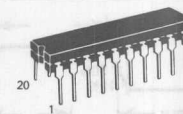
The eight latches of the HCT373 are transparent D-type latches. While the Latch Enable is high the Q outputs follow the Data Inputs. When Latch Enable is taken low, data meeting the setup and hold times becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

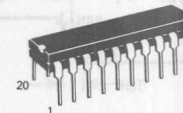
The HCT373 is identical in function to the HCT573, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT533, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates

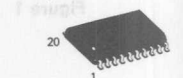
MC54/74HCT373



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



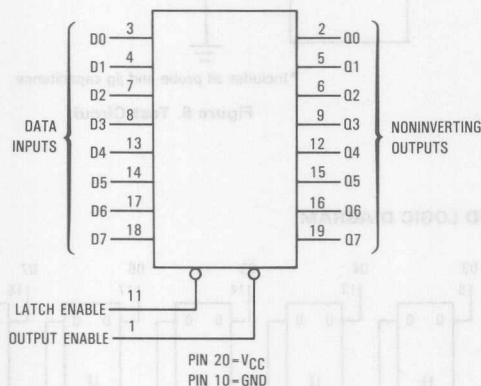
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

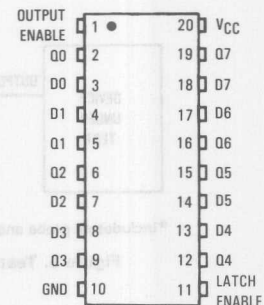
MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = don't care
Z = high impedance

MC54/74HCT373

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT373

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	35	44	53	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	35	44	53	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

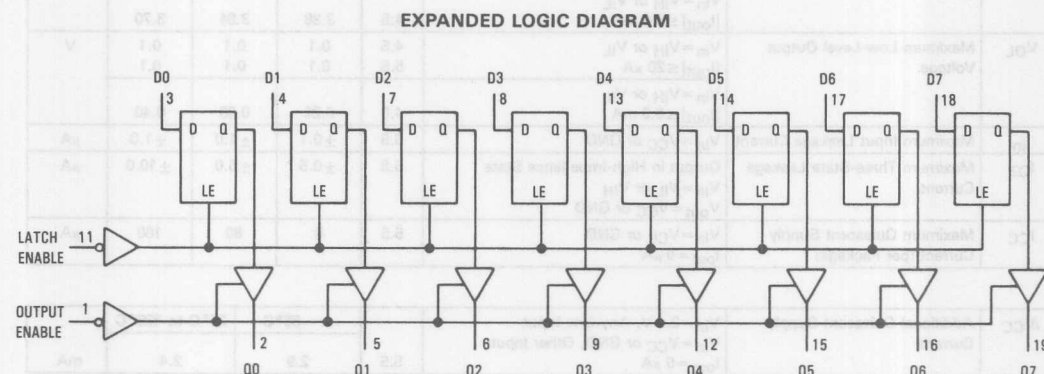
- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		65	

TIMING REQUIREMENTS ($V_{CC} = 5.0 \text{ V} \pm 10\%$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	10	13	15	ns
t_h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	10	13	15	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	16	20	24	ns
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.



SWITCHING WAVEFORMS

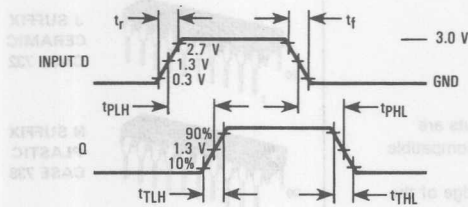


Figure 1

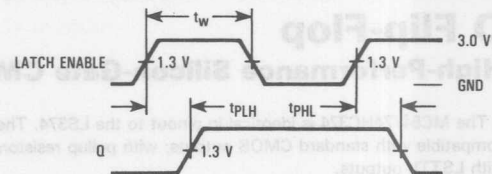


Figure 2

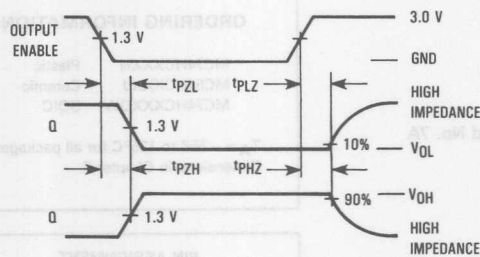


Figure 3

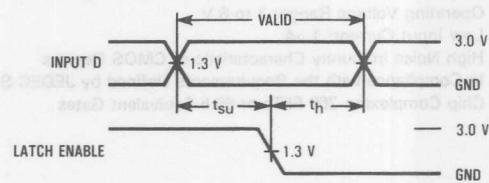
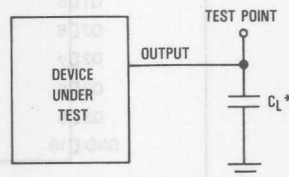
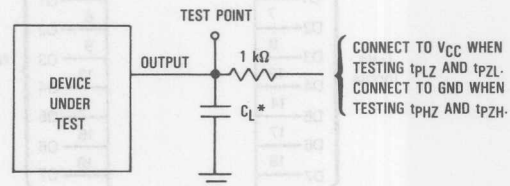


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

Octal 3-State Noninverting D Flip-Flop

High-Performance Silicon-Gate CMOS

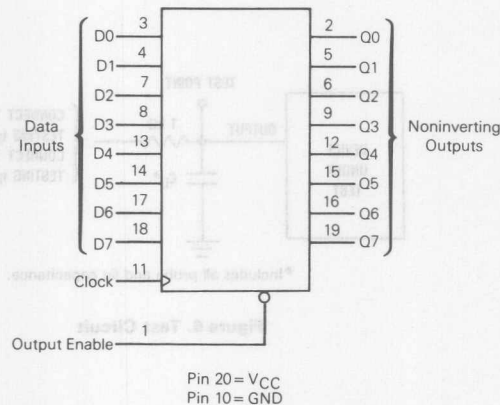
The MC54/74HC374 is identical in pinout to the LS374. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state; thus, data may be stored even when the outputs are not enabled.

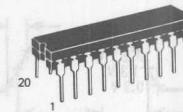
The HC374 is identical in function to the HC574, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC534, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates

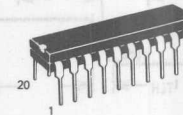
LOGIC DIAGRAM



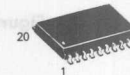
MC54/74HC374



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



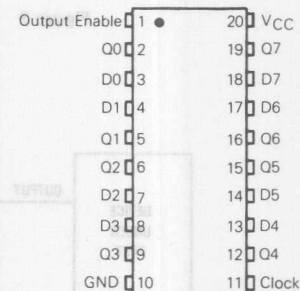
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Output Enable	Inputs		Output
	Clock	D	
L		H	H
L		L	L
L	L, H,	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MC54/74HC374

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC374

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	180	225	270	ns
		4.5	36	45	54	
		6.0	31	38	46	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = CPD \cdot V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

SWITCHING WAVEFORMS

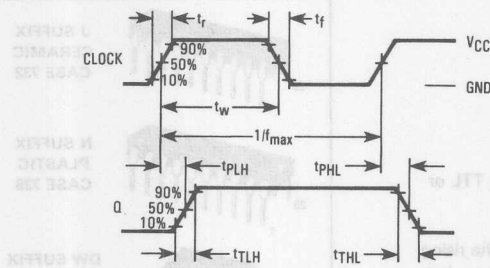


Figure 1

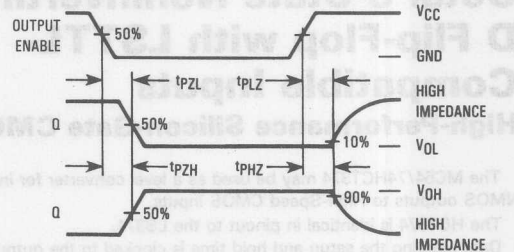


Figure 2

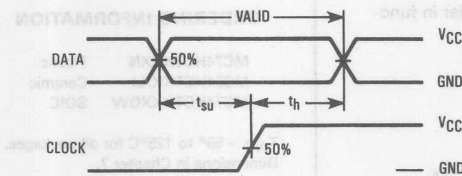
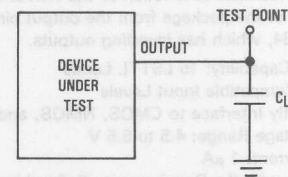
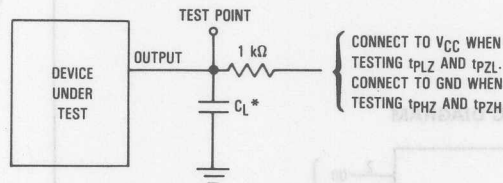


Figure 3



*Includes all probe and jig capacitance.

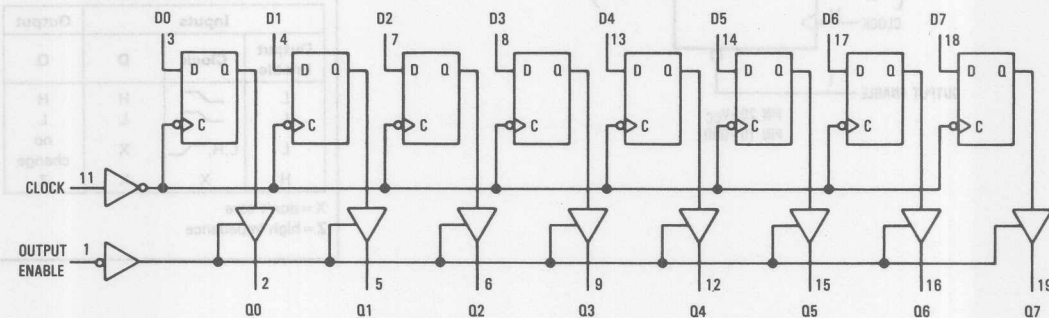
Figure 4. Test Circuit



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM



MC54/74HCT374

Octal 3-State Noninverting D Flip-Flop with LSTTL- Compatible Inputs High-Performance Silicon-Gate CMOS

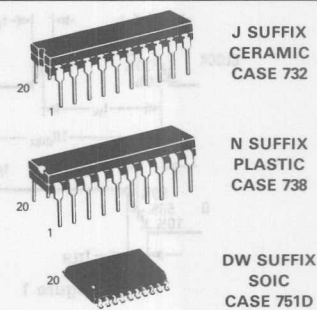
The MC54/74HCT374 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT374 is identical in pinout to the LS374.

Data meeting the setup and hold time is clocked to the outputs with the rising edge of Clock. The Output Enable does not affect the state of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HCT374 is identical in function to the HCT574, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT534, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates



ORDERING INFORMATION

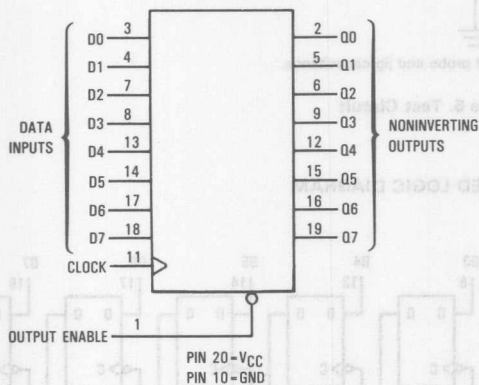
MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

OUTPUT ENABLE	1	20	V_{CC}
00	2	19	07
00	3	18	07
01	4	17	06
01	5	16	06
02	6	15	05
02	7	14	05
03	8	13	04
03	9	12	04
GND	10	11	CLOCK

LOGIC DIAGRAM



FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L		H	H
L		L	L
L	L, H,	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MC54/74HCT374

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT374

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	35	44	53	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	35	44	53	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	35	44	53	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	
		65	pF

TIMING REQUIREMENTS ($V_{CC}=5.0\text{ V} \pm 10\%$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	20	25	30	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	5	5	5	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	16	20	24	ns
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

5

MC54/74HCT374

SWITCHING WAVEFORMS

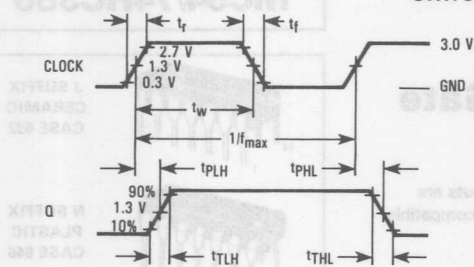


Figure 1

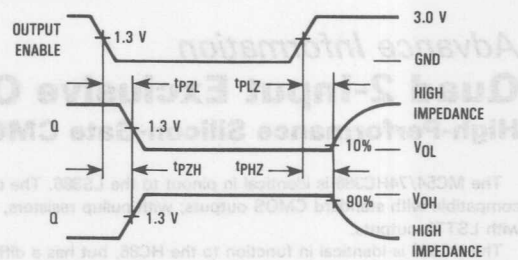


Figure 2

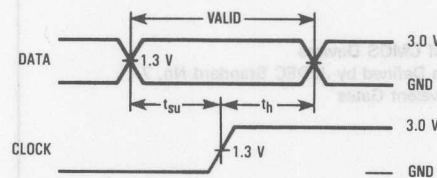
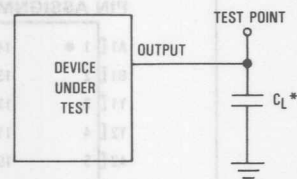
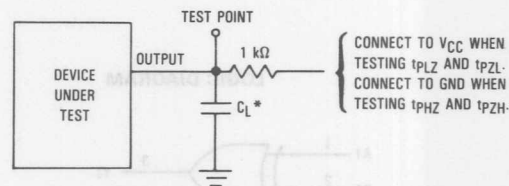


Figure 3



*Includes all probe and jig capacitance.

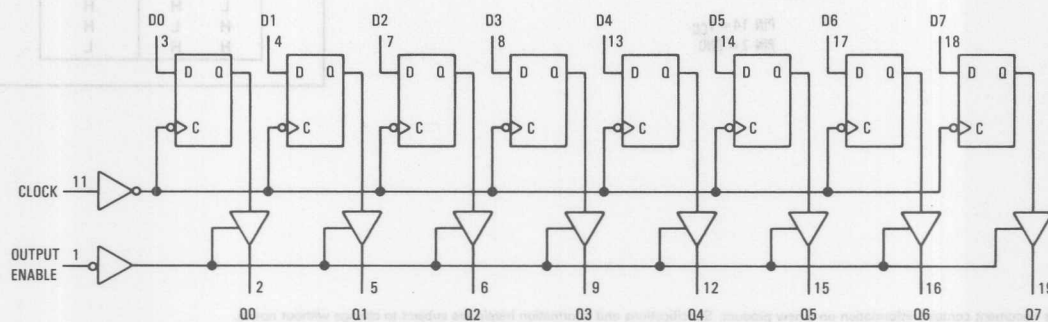
Figure 4. Test Circuit



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM



MC54/74HC386

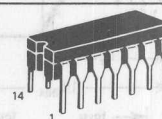
Advance Information

Quad 2-Input Exclusive OR Gate High-Performance Silicon-Gate CMOS

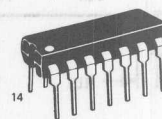
The MC54/74HC386 is identical in pinout to the LS386. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC386 is identical in function to the HC86, but has a different pin assignment.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



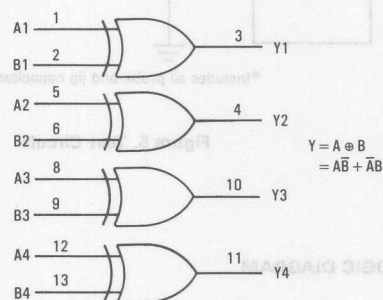
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	B4
Y1	3	12	A4
Y2	4	11	Y4
A2	5	10	Y3
B2	6	9	B3
GND	7	8	A3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

MC54/74HC386

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC386

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		33	

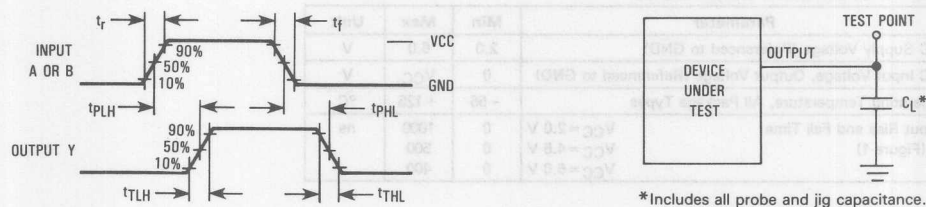
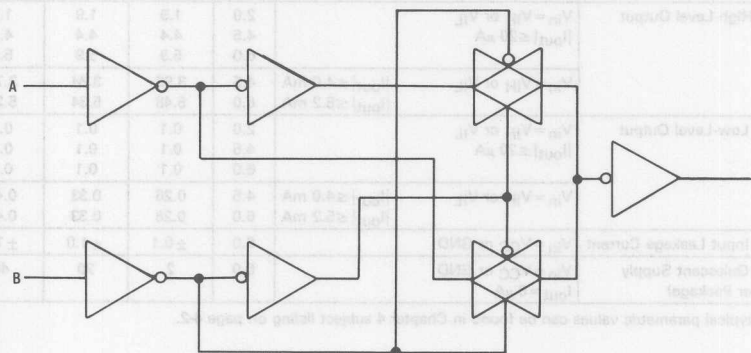


Figure 1. Switching Waveforms

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM (1/4 of the Device Shown)



Dual 4-Stage Binary Ripple Counter with $\div 2$ and $\div 5$ Sections

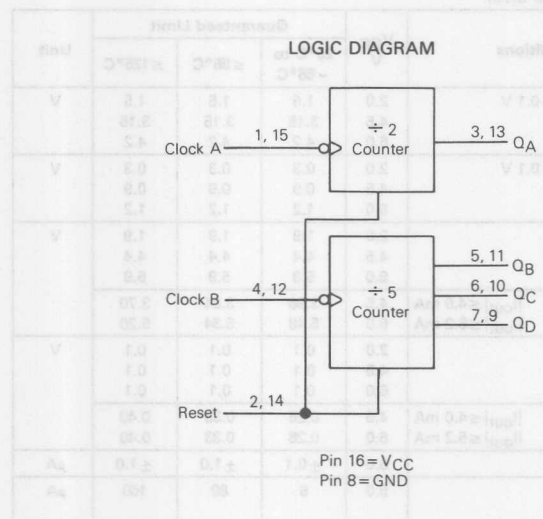
High-Performance Silicon-Gate CMOS

The MC54/74HC390 is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

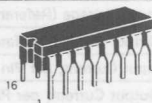
This device consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five section. The divide-by-two and divide-by-five counters have separate clock inputs, and can be cascaded to implement various combinations of $\div 2$ and/or $\div 5$ up to a $\div 100$ counter.

Flip-flops internal to the counters are triggered by high-to-low transitions of the clock input. A separate, asynchronous reset is provided for each 4-bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390.

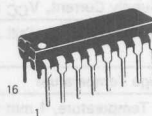
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates



MC54/74HC390



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

Clock A _a	1	16	V _{CC}
Reset a	2	15	Clock A _b
Q _{Aa}	3	14	Reset b
Clock B _a	4	13	Q _{Ab}
Q _{Ba}	5	12	Clock B _b
Q _{Ca}	6	11	Q _{Bb}
Q _{Da}	7	10	Q _{Cb}
GND	8	9	Q _{Db}

FUNCTION TABLE

Clock		Reset	Action
A	B		
X	X	H	Reset $\div 2$ and $\div 5$
\neg	X	L	Increment $\div 2$
X	\neg	L	Increment $\div 5$

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC390

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	5.4	4.4	3.6	MHz
		4.5	27	22	18	
		6.0	32	26	21	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock A to QA (Figures 1 and 3)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock A to QC (QA connected to Clock B) (Figures 1 and 3)	2.0	290	365	435	ns
		4.5	58	73	87	
		6.0	49	62	74	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock B to QB (Figures 1 and 3)	2.0	130	165	195	ns
		4.5	26	33	39	
		6.0	22	28	33	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock B to QC (Figures 1 and 3)	2.0	185	230	280	ns
		4.5	37	46	56	
		6.0	31	39	48	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock B to QD (Figures 1 and 3)	2.0	130	165	195	ns
		4.5	26	33	39	
		6.0	22	28	33	
t _{PHL}	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Counter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$	pF
		35	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock A or Clock B (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _w	Minimum Pulse Width, Clock A, Clock B (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC390

PIN DESCRIPTIONS

INPUTS

CLOCK A (PINS 1, 15) and CLOCK B (PINS 4, 15) — Clock A is the clock input to the $\div 2$ counter; Clock B is the clock input to the $\div 5$ counter. The internal flip-flops are toggled by high-to-low transitions of the clock input.

CONTROL INPUTS

RESET (PINS 2, 14) — Asynchronous reset. A high at the Reset input prevents counting, resets the internal flip-flops, and forces Q_A through Q_D low.

OUTPUTS

Q_A (PINS 3, 13) — Output of the $\div 2$ counter.
 Q_B, Q_C, Q_D (PINS 5, 6, 7, 9, 10, 11) — Outputs of the $\div 5$ counter. Q_D is the most significant bit. Q_A is the least significant bit when the counter is connected for BCD output as in Figure 4. Q_B is the least significant bit when the counter is operating in the bi-quinary mode as in Figure 5.

SWITCHING WAVEFORMS

FIGURE 1

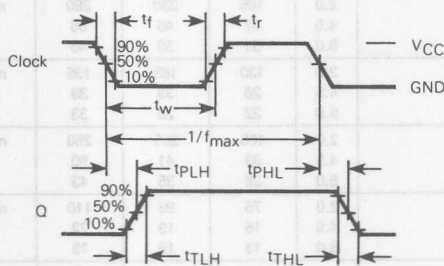


FIGURE 2

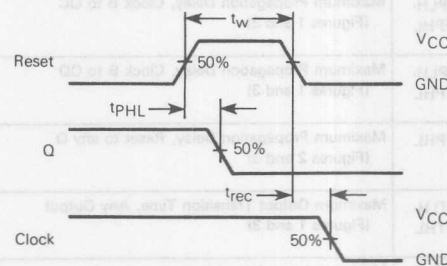
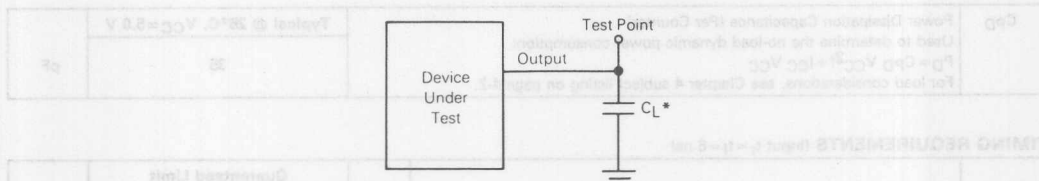


FIGURE 3 — TEST CIRCUIT



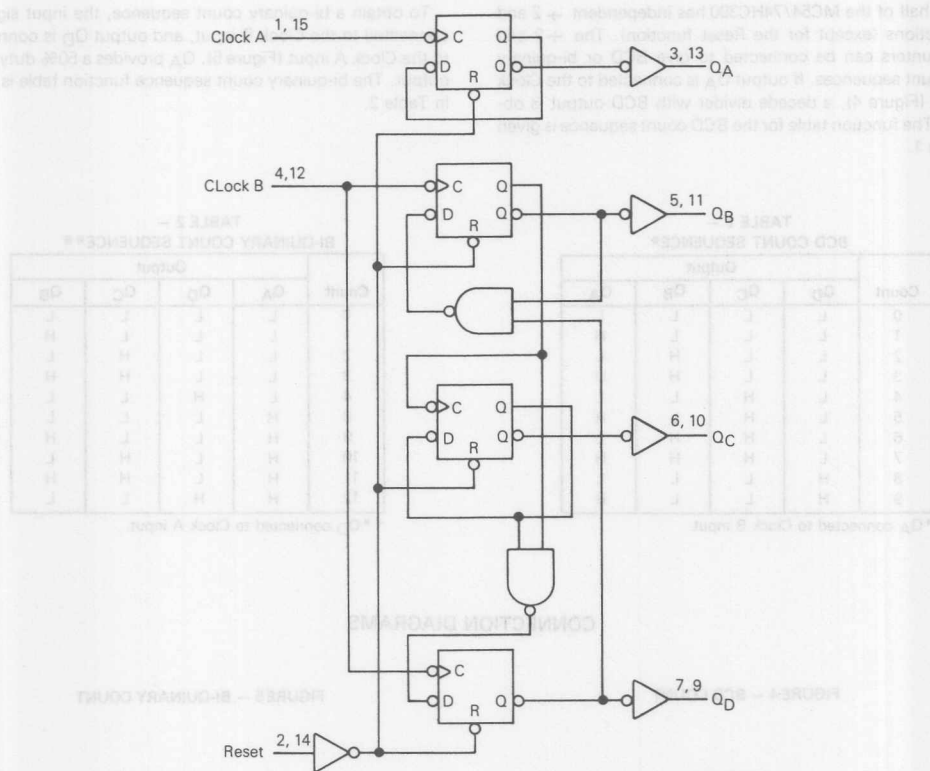
* Includes all probe and jig capacitance.

Symbol	Parameter	Unit	Typical Value	Maximum Value
t_{rec}	Minimum Recovery Time, Reset to Clock A or Clock B (Figure 2)	ns	10	15
t_w	Minimum Pulse Width, Clock A, Clock B (Figure 1)	ns	10	15
t_w	Minimum Pulse Width, Reset (Figure 2)	ns	10	15
t_{PLH}	Propagation Delay, Low-to-High, Clock A, Clock B (Figure 1)	ns	10	15
t_{PLH}	Propagation Delay, Low-to-High, Reset (Figure 2)	ns	10	15
t_{PLH}	Propagation Delay, High-to-Low, Clock A, Clock B (Figure 1)	ns	10	15
t_{PLH}	Propagation Delay, High-to-Low, Reset (Figure 2)	ns	10	15
t_{TLH}	Turn-On Time, Clock A, Clock B (Figure 1)	ns	10	15
t_{TLH}	Turn-On Time, Reset (Figure 2)	ns	10	15
t_{TLH}	Turn-Off Time, Clock A, Clock B (Figure 1)	ns	10	15
t_{TLH}	Turn-Off Time, Reset (Figure 2)	ns	10	15

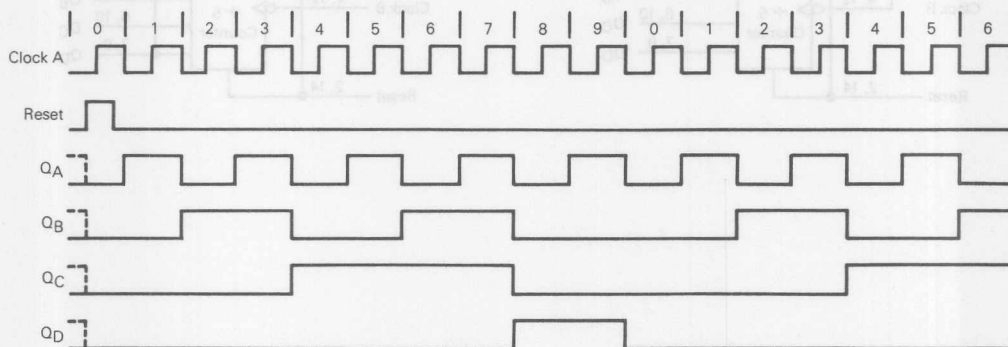
NOTE: Information on typical parameter values can be found in Chapter 4, section 4.1 on page 4-1.

MC54/74HC390

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM (QA Connected to Clock B)



MC54/74HC390

APPLICATIONS INFORMATION

Each half of the MC54/74HC390 has independent $\div 2$ and $\div 5$ sections (except for the Reset function). The $\div 2$ and $\div 5$ counters can be connected to give BCD or bi-quinary (2-5) count sequences. If output Q_A is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The function table for the BCD count sequence is given in Table 1.

To obtain a bi-quinary count sequence, the input signal is connected to the Clock B input, and output Q_D is connected to the Clock A input (Figure 5). Q_A provides a 50% duty cycle output. The bi-quinary count sequence function table is given in Table 2.

TABLE 1 —
BCD COUNT SEQUENCE*

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

* Q_A connected to Clock B input.

TABLE 2 —
BI-QUINARY COUNT SEQUENCE**

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L

** Q_D connected to Clock A input.

CONNECTION DIAGRAMS

FIGURE 4 — BCD COUNT

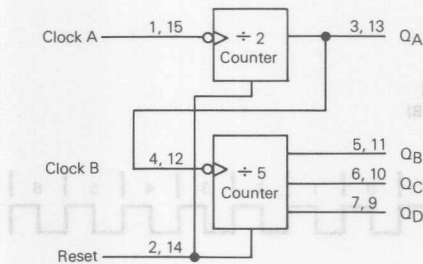
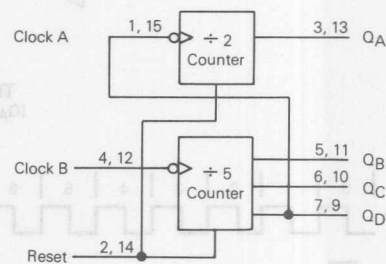


FIGURE 5 — BI-QUINARY COUNT



Dual 4-Stage Binary Ripple Counter

High-Performance Silicon-Gate CMOS

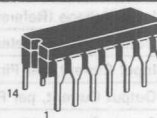
The MC54/74HC393 is identical in pinout to the LS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit binary ripple counters with parallel outputs from each counter stage. A $\rightarrow 256$ counter can be obtained by cascading the two binary counters.

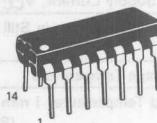
Internal flip-flops are triggered by high-to-low transitions of the clock input. Reset for the counters is asynchronous and active-high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the HC393.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 236 FETs or 59 Equivalent Gates

MC54/74HC393



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

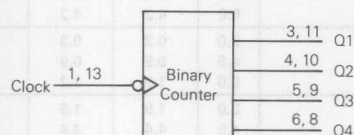
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

Clock a	1	14	V_{CC}
Reset a	2	13	Clock b
Q1 _a	3	12	Reset b
Q2 _a	4	11	Q1 _b
Q3 _a	5	10	Q2 _b
Q4 _a	6	9	Q3 _b
GND	7	8	Q4 _b

LOGIC DIAGRAM



Pin 14 = V_{CC}
Pin 7 = GND

FUNCTION TABLE

Inputs		Outputs
Clock	Reset	
X	H	L
H	L	No Change
L	L	No Change
\uparrow	L	No Change
\downarrow	L	Advance to Next State

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC393

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0 4.5 6.0	5.4 27 32	4.4 22 26	3.6 18 21	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q2 (Figures 1 and 3)	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q3 (Figures 1 and 3)	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q4 (Figures 1 and 3)	2.0 4.5 6.0	290 58 49	365 73 62	435 87 74	ns
t _{PHL}	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0 4.5 6.0	165 33 28	205 41 35	250 50 43	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Counter) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC393

PIN DESCRIPTIONS

INPUTS

CLOCK (PINS 1, 13) — Clock input. The internal flip-flops are toggled and the counter state advances on high-to-low transitions of the clock input.

CONTROL INPUTS

RESET (PINS 2, 12) — Active-high, asynchronous reset. A

separate reset is provided for each counter. A high at the Reset input prevents counting and forces all four outputs low.

OUTPUTS

Q1, Q2, Q3, Q4 (PINS 3, 4, 5, 6, 8, 9, 10, 11) — Parallel binary outputs. Q4 is the most significant bit.

SWITCHING WAVEFORMS

FIGURE 1

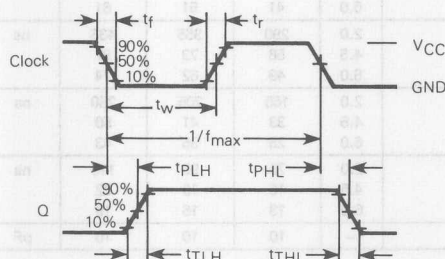


FIGURE 2

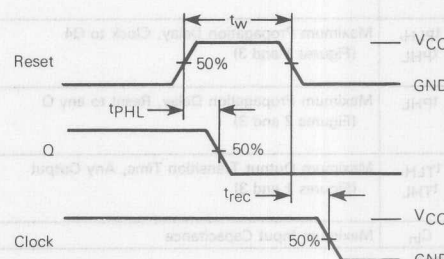
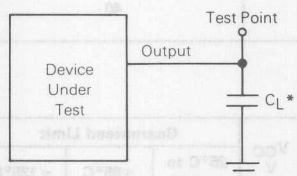
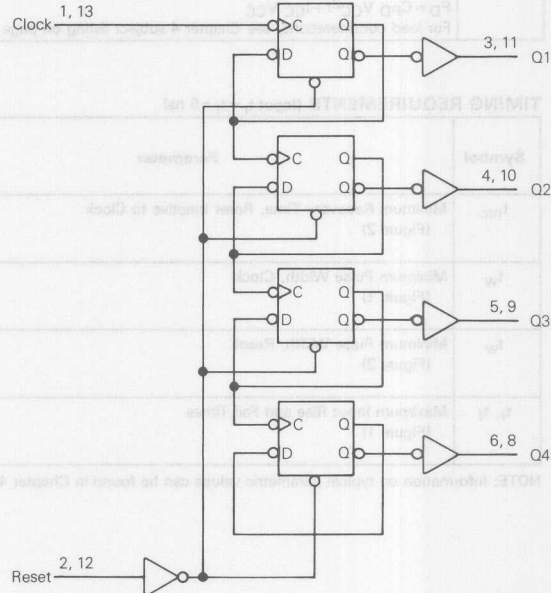


FIGURE 3 — TEST CIRCUIT

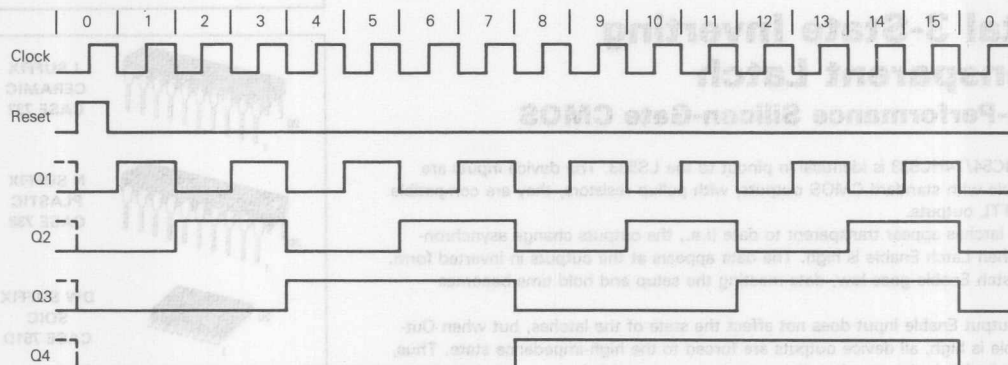


* Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



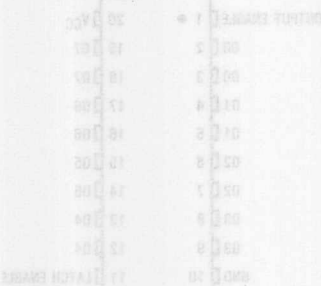
COUNT SEQUENCE

Count	Outputs			
	Q4	Q3	Q2	Q1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

ORDERING INFORMATION

MC54HC393DW Plastic
MC54HC393C Ceramic
MC54HC393CZ SOIC

PIN ASSIGNMENT



FUNCTION TABLE

Output	Q	Q	Q	Q
Q	Q	Q	Q	Q
L	H	H	H	H
L	L	H	H	H
L	L	L	H	H
L	L	L	L	H
L	L	L	L	L

X = don't care
Z = high impedance

Octal 3-State Inverting Transparent Latch

High-Performance Silicon-Gate CMOS

The MC54/74HC533 is identical in pinout to the LS533. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

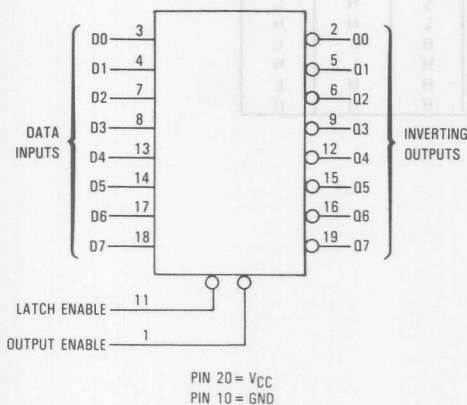
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. The data appears at the outputs in inverted form. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

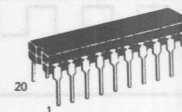
The HC533 is identical in function to the HC563, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HC373, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 256 FETs or 64 Equivalent Gates

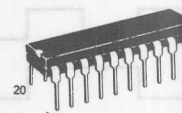
LOGIC DIAGRAM



MC54/74HC533



J SUFFIX
 CERAMIC
 CASE 732



N SUFFIX
 PLASTIC
 CASE 738



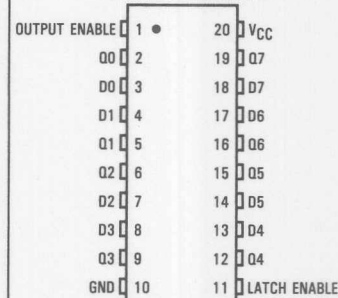
DW SUFFIX
 SOIC
 CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

T_A = -55° to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	L
L	H	L	H
L	L	X	no change
H	X	X	Z

X = don't care
 Z = high impedance

MC54/74HC533

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		41	

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
t _h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t _w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

SWITCHING WAVEFORMS

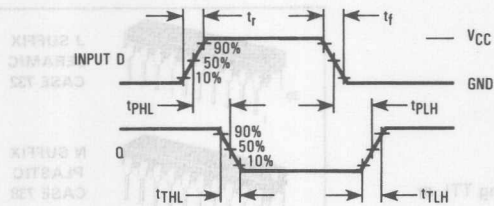


Figure 1

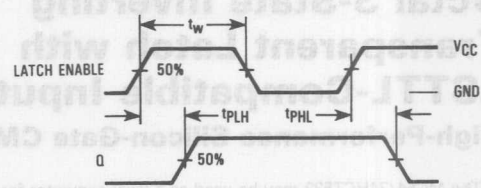


Figure 2

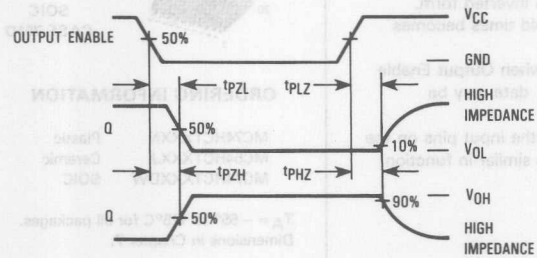


Figure 3

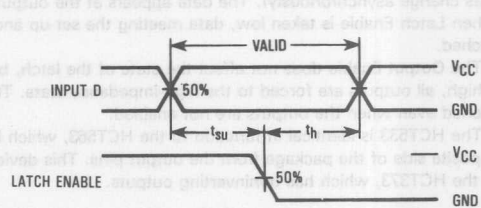
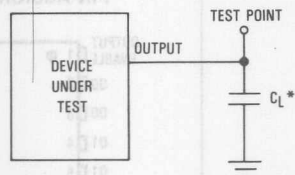
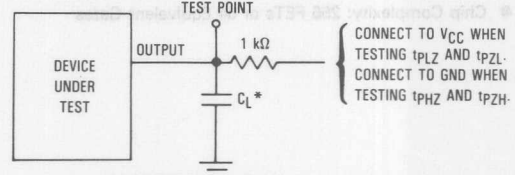


Figure 4



*Includes all probe and jig capacitance.

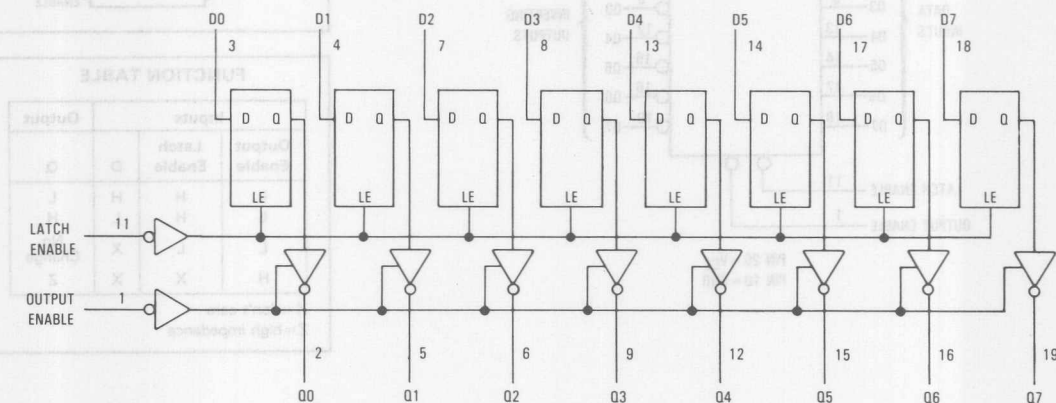
Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



MC54/74HCT533

Octal 3-State Inverting Transparent Latch with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT533 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

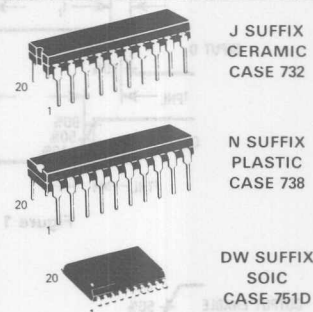
The HCT533 is identical in pinout to the LS533.

When Latch Enable is high, these latches appear transparent to data (i.e., the outputs change asynchronously). The data appears at the outputs in inverted form. When Latch Enable is taken low, data meeting the set-up and hold times becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT533 is identical in function to the HCT563, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT373, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 256 FETs or 64 Equivalent Gates

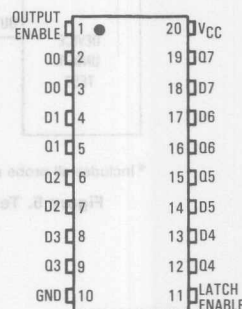


ORDERING INFORMATION

MC74HCTXXXN Plastic
MC54HCTXXXJ Ceramic
MC74HCTXXXDW SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

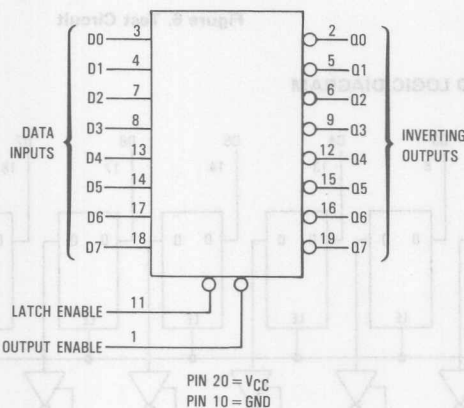


FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	L
L	H	L	H
L	L	X	No Change
H	X	X	Z

X = don't care
Z = high impedance

LOGIC DIAGRAM



MC54/74HCT533

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu A$	5.5	8	80	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu A$	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT533

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	35	44	53	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	35	44	53	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	35	44	53	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

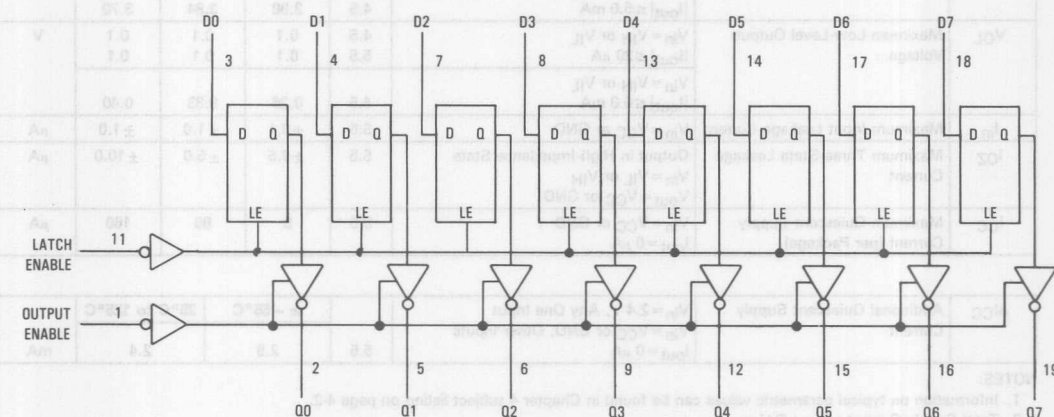
C_{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	pF
		65	

TIMING REQUIREMENTS ($V_{CC}=5.0\text{ V} \pm 10\%$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	20	25	30	ns
t_h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	5	6	8	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

EXPANDED LOGIC DIAGRAM



SWITCHING WAVEFORMS

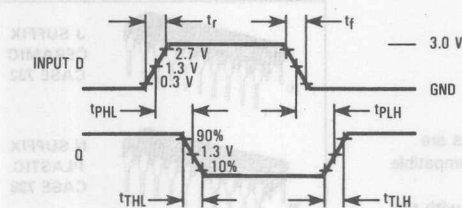


Figure 1

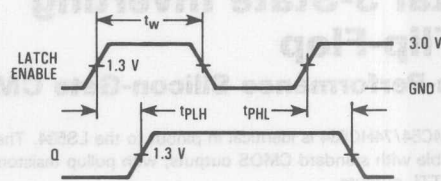


Figure 2

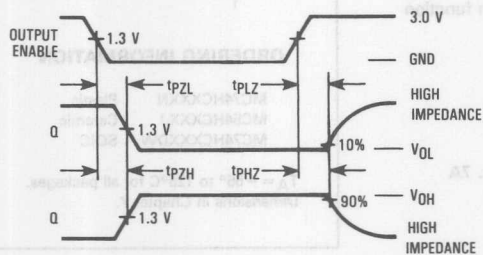


Figure 3

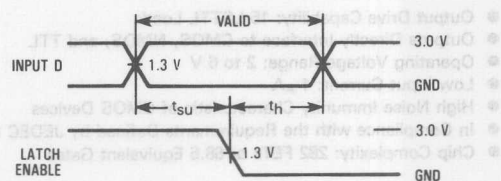
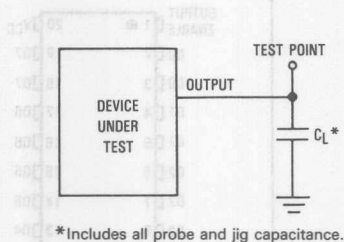
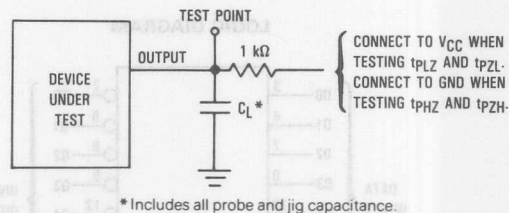


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

FUNCTION TABLE			
Output Enable	Output Clock	Input D	Output Q
L	H	0	L
L	L	1	L
H	X	0	L
H	X	1	H
X	X	X	X

X=don't care
Z=high impedance

Octal 3-State Inverting D Flip-Flop

High-Performance Silicon-Gate CMOS

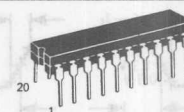
The MC54/74HC534 is identical in pinout to the LS534. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

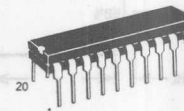
The HC534 is identical in function to the HC564, which has the input pins on the opposite side of the package from the output pins. The device is similar in function to the HC374, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 282 FETs or 68.5 Equivalent Gates

MC54/74HC534



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



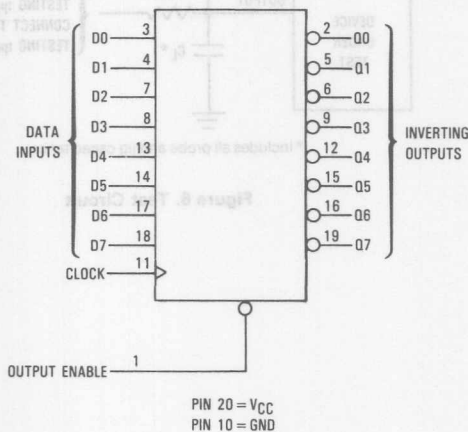
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

OUTPUT ENABLE	1	20	V_{CC}
Q0	2	19	Q7
Q1	3	18	Q6
Q2	4	17	Q5
Q3	5	16	Q4
Q4	6	15	Q3
Q5	7	14	Q2
Q6	8	13	Q1
Q7	9	12	Q0
GND	10	11	CLOCK

FUNCTION TABLE

Output Enable	Inputs		Output Q
	Clock	D	
L		H	L
L		L	H
L	L, H,	X	No Change
H	X	X	Z

X = don't care
Z = high impedance

MC54/74HC534

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	180	225	270	ns
		4.5	36	45	54	
		6.0	31	38	46	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

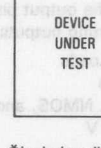
- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	25	30	40	ns
		4.5	5	6	8	
		6.0	5	6	7	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.



*Includes all
Fig

*Includes all
Fig

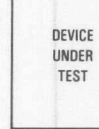
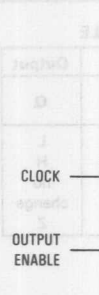


Figure 5. Test Circuit

Figure 1. Test circuit.



MC54/74HCT534

Octal 3-State Inverting D Flip-Flop with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

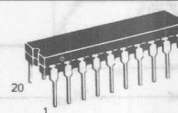
The MC54/74HCT534 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT534 is identical in pinout to the LS534.

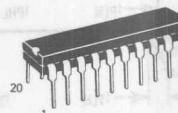
Data meeting the setup and hold time is clocked, in inverted form, to the outputs with the rising edge of Clock. The Output Enable does not affect the state of the flip-flops, but when Output Enable is high, the outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HCT534 is identical in function to the HCT564, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT374, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 229 FETs or 57 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



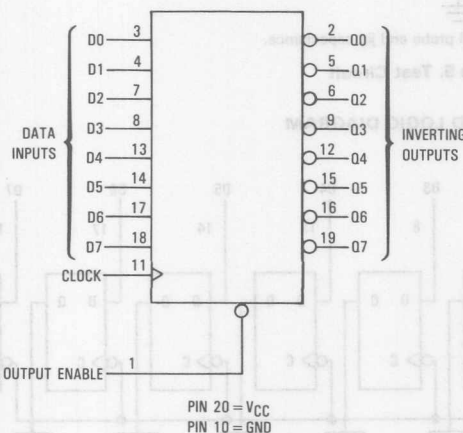
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

OUTPUT ENABLE	1	20	V_{CC}
Q0	2	19	Q7
Q0	3	18	Q7
Q1	4	17	Q6
Q1	5	16	Q6
Q2	6	15	Q5
Q2	7	14	Q5
Q3	8	13	Q4
Q3	9	12	Q4
GND	10	11	CLOCK

FUNCTION TABLE

Output Enable	Inputs		Output
	Clock	D	
L		H	L
L		L	H
L	L, H, \nearrow	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MC54/74HCT534

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	−1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	−0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C

Ceramic DIP: −10 mW/°C from 100° to 125°C

SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	−55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} − 0.1 V I _{out} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} − 0.1 V I _{out} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5 5.5	3.98 0.1	3.84 0.1	3.70 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5	8	80	160	μA

ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5	≥ −55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = I_{CC} + ΣΔI_{CC}.

MC54/74HCT534

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_I=50\text{ pF}$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	25	31	38	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	35	44	53	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	35	44	53	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	35	44	53	ns
t _{TLH} , t _{TLH}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	12	15	18	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop)	Typical @ 25°C, V _{CC} = 5.0 V	
	Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4 subject listing on page 4-2.	65	pF

TIMING REQUIREMENTS ($V_{CC}=5.0\text{ V} \pm 10\%$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t _{SU}	Minimum Setup Time, Data to Clock (Figure 3)	10	13	15	ns
t _H	Minimum Hold Time, Clock to Data (Figure 3)	5	5	5	ns
t _W	Minimum Pulse Width, Clock (Figure 1)	16	20	24	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

SWITCHING WAVEFORMS

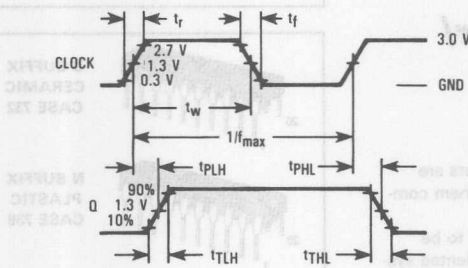


Figure 1

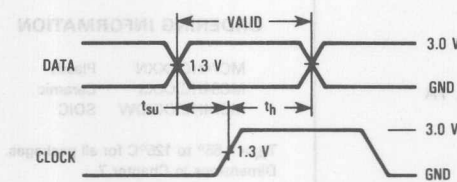


Figure 3

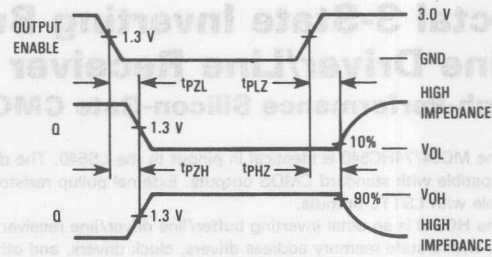
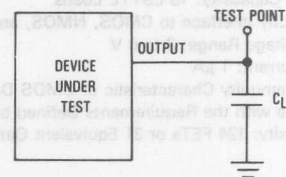
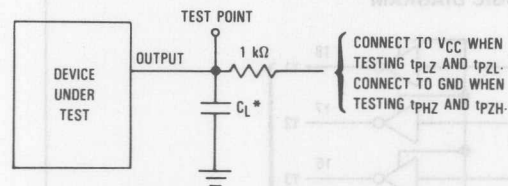


Figure 2



*Includes all probe and jig capacitance.

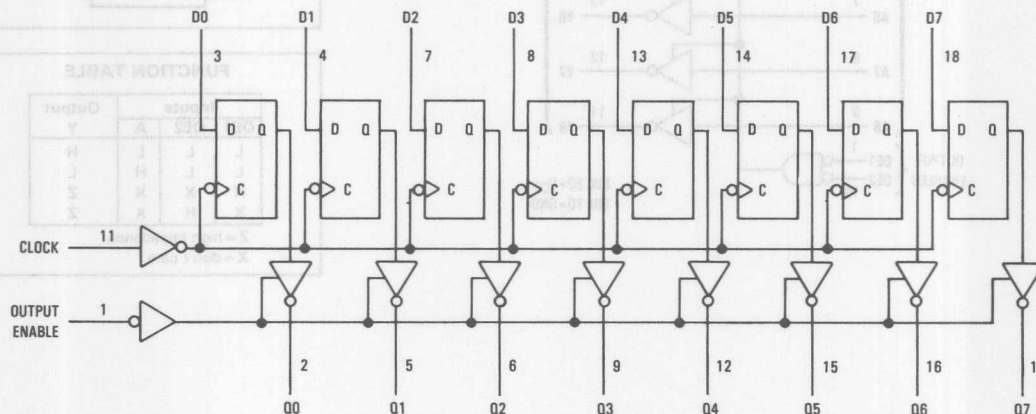
Figure 4. Test Circuit



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

EXPANDED LOGIC DIAGRAM



Octal 3-State Inverting Buffer/ Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

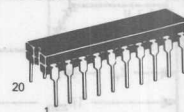
The MC54/74HC540 is identical in pinout to the LS540. The device inputs are compatible with standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

The HC540 is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

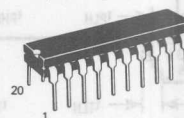
The HC540 is similar in function to the HC541, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 124 FETs or 31 Equivalent Gates

MC54/74HC540



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



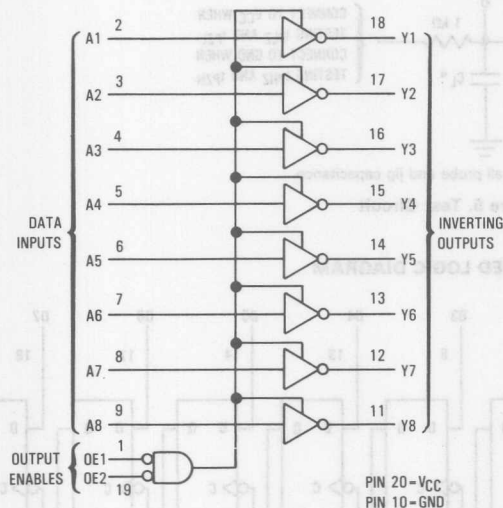
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENTS

OE1	1	20	VCC
A1	2	19	OE2
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

FUNCTION TABLE

Inputs			Output
OE1	OE2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = high impedance
X = don't care

MC54/74HC540

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC540

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

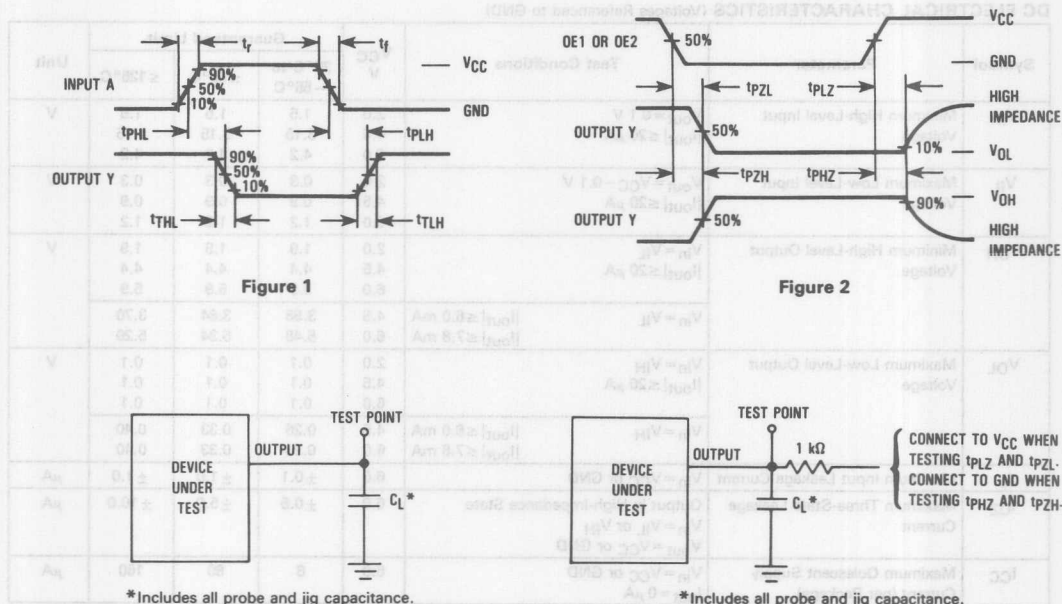
Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		35	pF

SWITCHING WAVEFORMS



PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

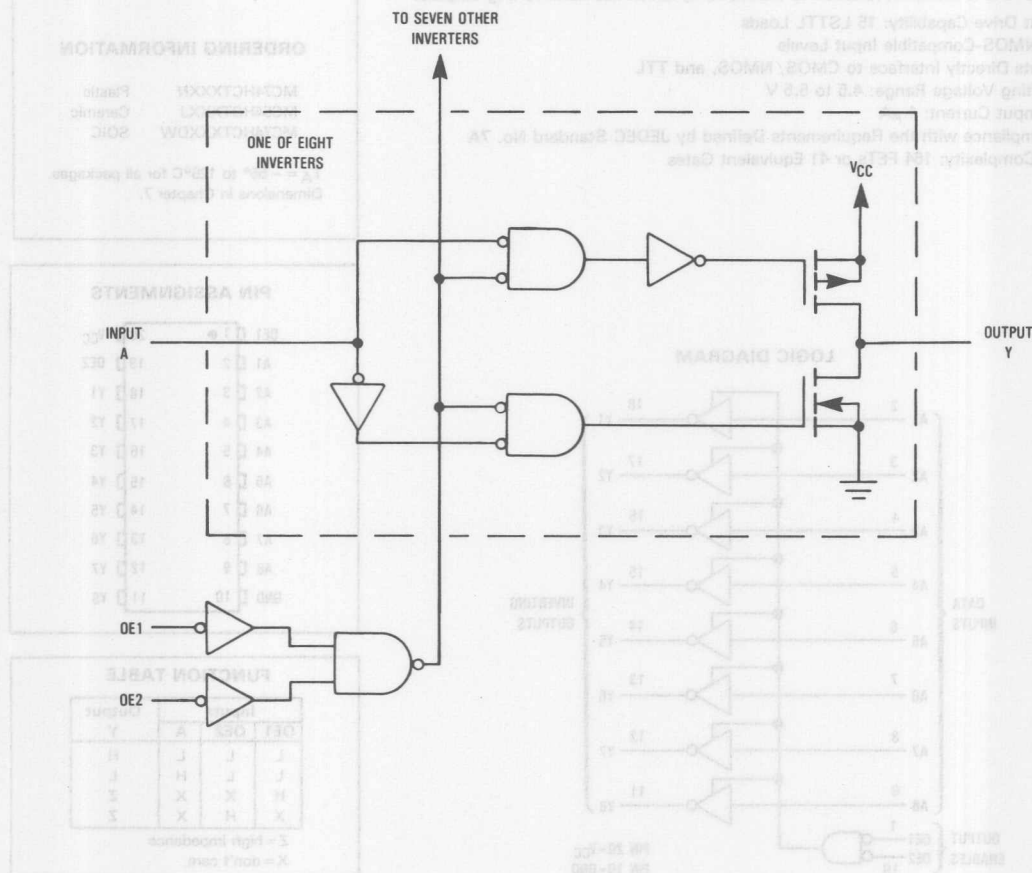
OE1, OE2 (PINS 1, 19) — Output enables (active-low). When a low voltage is applied to both of these pins, the outputs

are enabled and the device functions as an inverter. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output enable pins, these outputs are either inverting outputs or high-impedance outputs.

LOGIC DETAIL



Octal 3-State Inverting Buffer/ Line Driver/Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

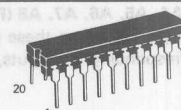
The MC54/74HCT540 is identical in pinout to the LS540. This device may be used as a level converter for interfacing TTL or NMOS to High-Speed CMOS inputs.

The HCT540 is an octal inverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

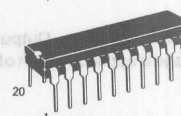
The HCT540 is similar in function to the HCT541, which has noninverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 164 FETs or 41 Equivalent Gates

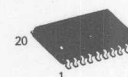
MC54/74HCT540



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



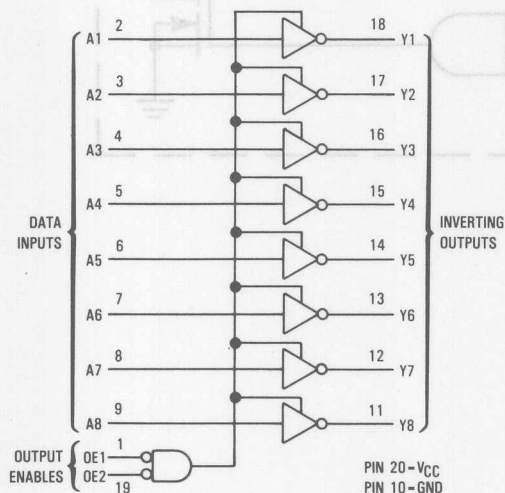
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCTXXXN Plastic
MC54HCTXXXJ Ceramic
MC74HCTXXXDW SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENTS

OE1	1	20	V_{CC}
A1	2	19	OE2
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

FUNCTION TABLE

Inputs			Output
OE1	OE2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = high impedance
X = don't care

MC54/74HCT540

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu A$	5.5	8	80	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu A$	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS (VCC=5.0 V ± 10%, CL=50 pF, input tr=0.5 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
tPLH, tPHL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	30	38	45	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	35	44	53	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	45	56	68	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
Cin	Maximum Input Capacitance	10	10	10	pF
Cout	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC=5.0 V	pF
		50	

SWITCHING WAVEFORMS

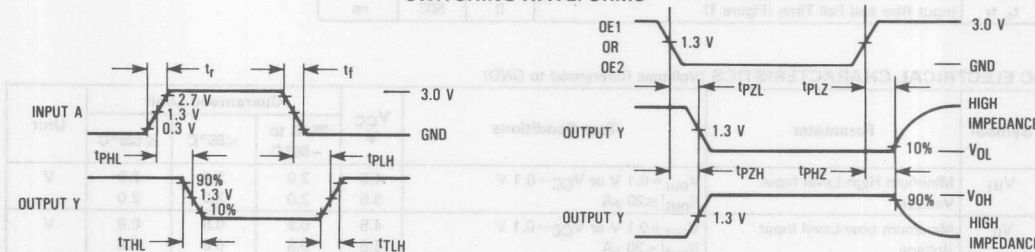
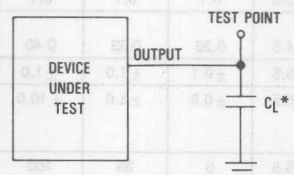


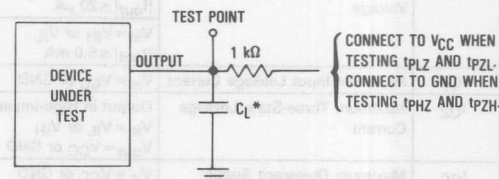
Figure 1

Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

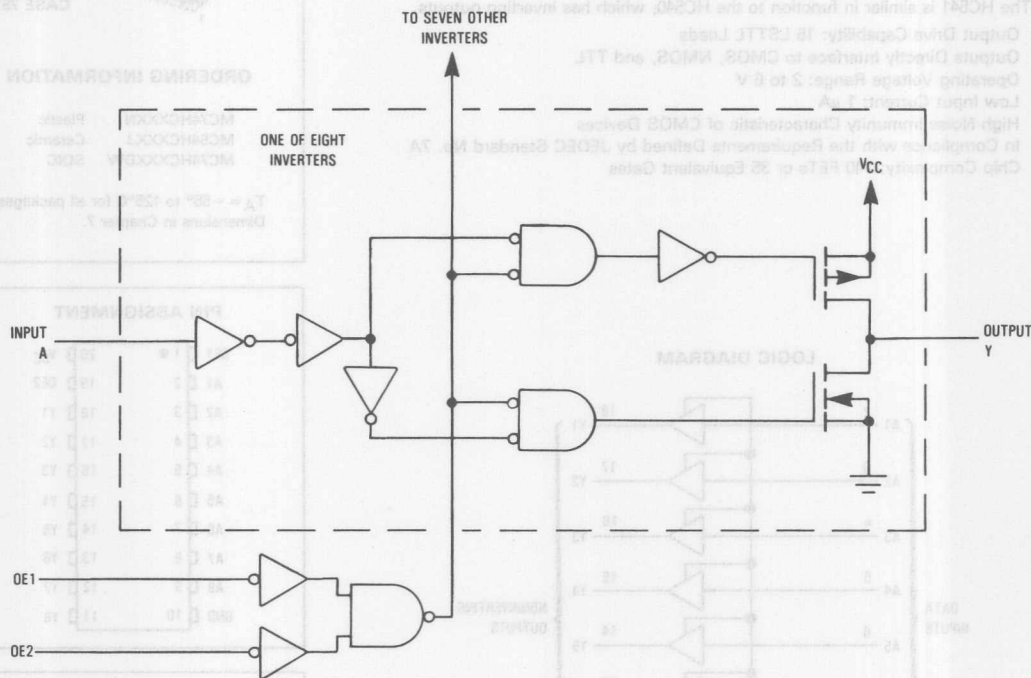
INPUTS

are enabled and the device functions as an inverter. When a high level is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either inverting outputs or high impedance outputs.

ONE OF EIGHT
INVERTERS



MC54/74HC541

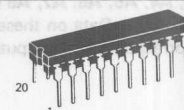
Octal 3-State Noninverting Buffer/Line Driver/Line Receiver High-Performance Silicon-Gate CMOS

The MC54/74HC541 is identical in pinout to the LS541. The device inputs are compatible with standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

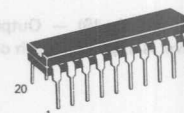
The HC541 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HC541 is similar in function to the HC540, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 140 FETs or 35 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



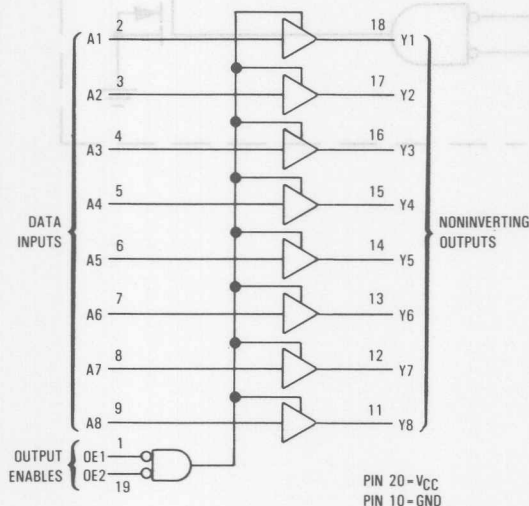
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

OE1	1	20	V_{CC}
A1	2	19	OE2
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

FUNCTION TABLE

Inputs			Output
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = high impedance
X = don't care

MC54/74HC541

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IL}$ $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μ A
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	6.0	8	80	160	μ A

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	
		35	pF

SWITCHING WAVEFORMS

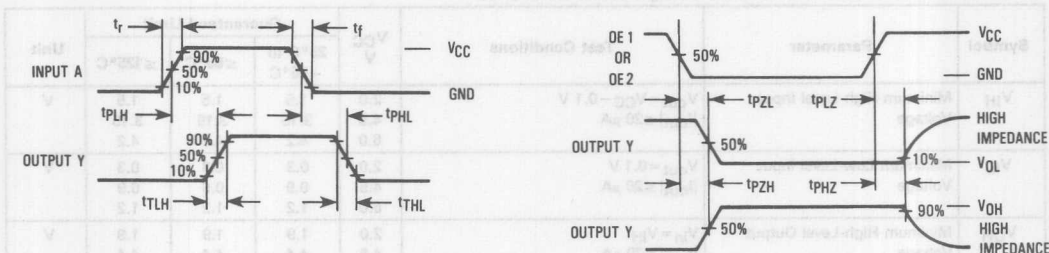
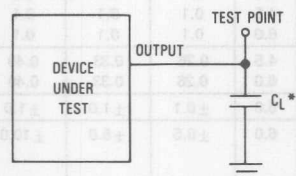
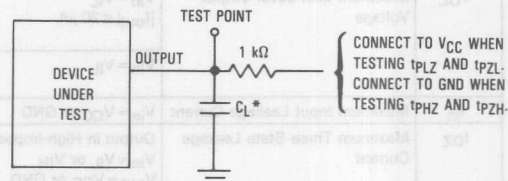


Figure 1

Figure 2



*Includes all probe and jig capacitance.



*Includes all probe and jig capacitance.

Figure 3. Test Circuit

Figure 4. Test Circuit

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

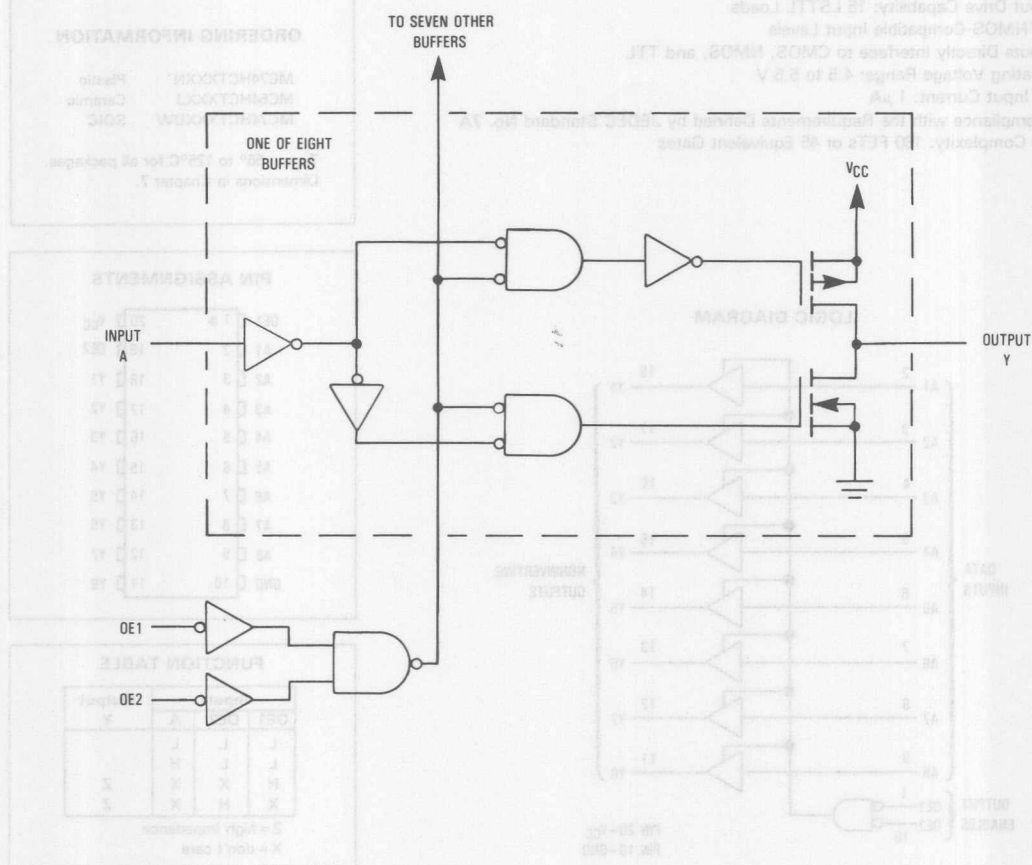
OE1, OE2 (PINS 1, 19) — Output enables (active-low). When a low level is applied to both of these pins, the outputs

are enabled and the device functions as a noninverting buffer. When a high level is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high impedance outputs.

LOGIC DETAIL



MC54/74HCT541

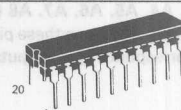
Octal 3-State Noninverting Buffer/Line Driver/Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT541 is identical in pinout to the LS541. The device may be used as a level converter for interfacing TTL or NMOS to High-Speed CMOS inputs.

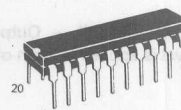
The HCT541 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HCT541 is similar in function to the HCT540, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 180 FETs or 45 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



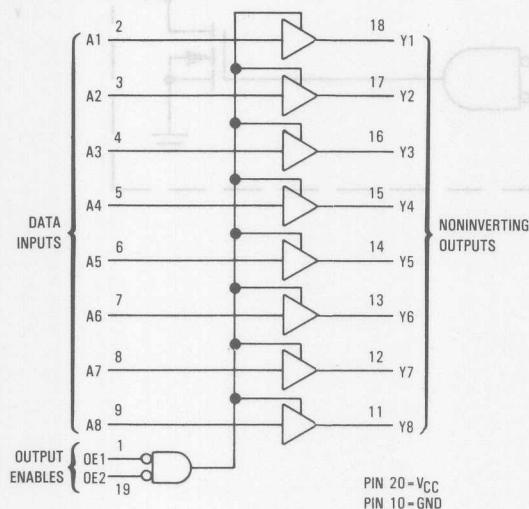
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENTS

OE1	1	20	V_{CC}
A1	2	19	OE2
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

FUNCTION TABLE

Inputs			Output
OE1	OE2	A	Y
L	L	L	
L	L	H	
H	X	X	Z
X	H	X	Z

Z = high impedance
X = don't care

MC54/74HCT541

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5 5.5	3.98 0.1	3.84 0.1	3.70 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5 5.5	0.26 0.1	0.33 0.1	0.40 0.1	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or } GND$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or } GND, \text{ Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	30	38	45	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	35	44	53	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	45	56	68	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	pF
		50	

SWITCHING WAVEFORMS

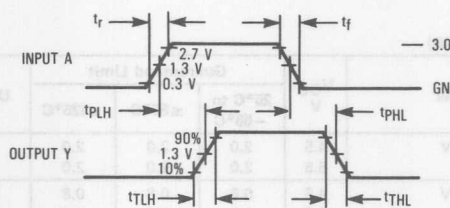


Figure 1

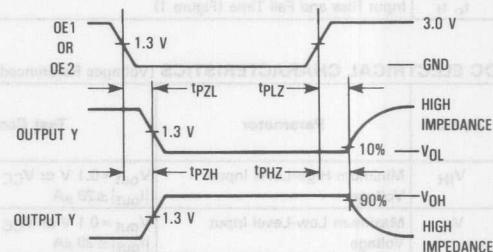
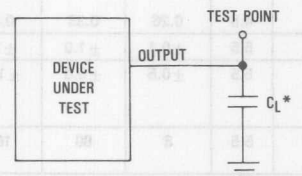
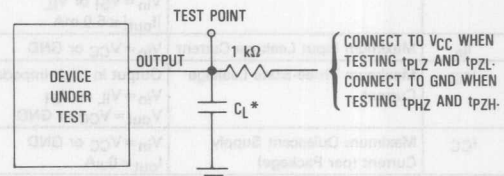


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

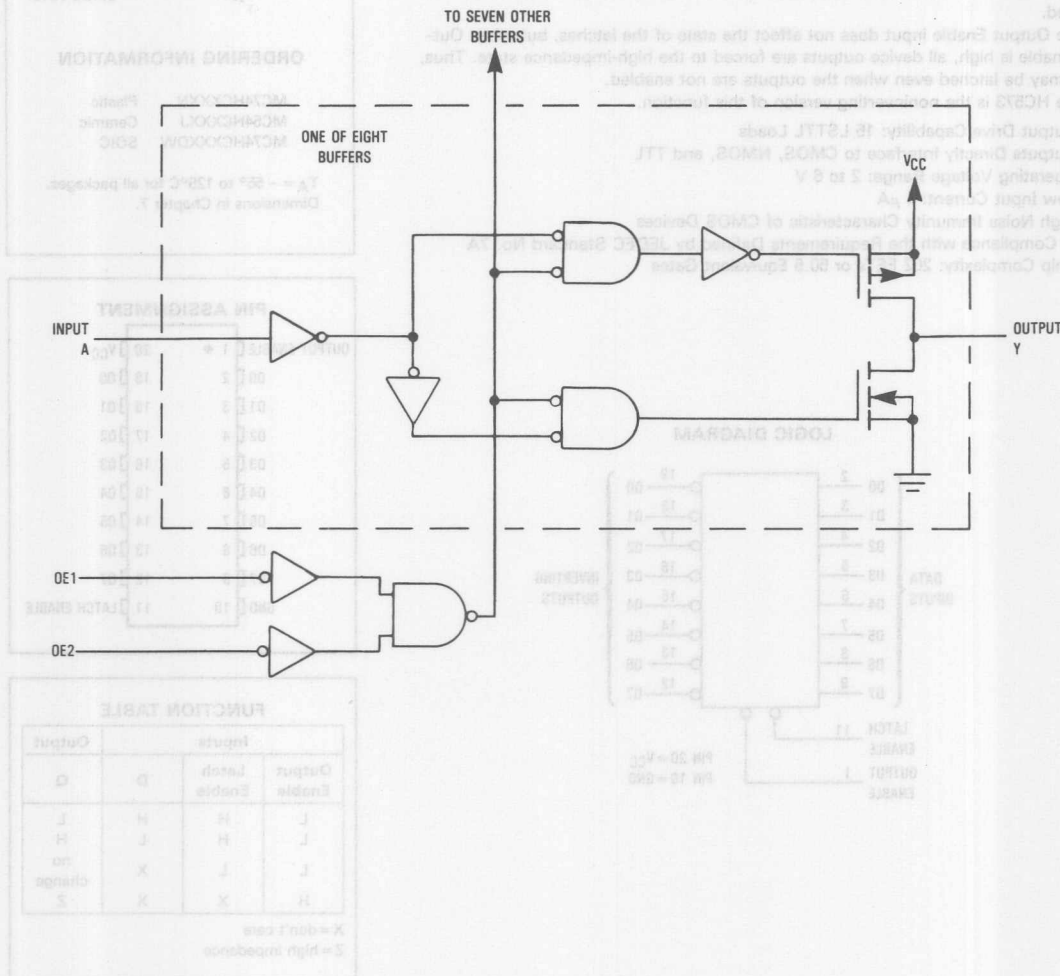
OE1, OE2 (PINS 1, 19) — Output enables (active low). When a low level is applied to both of these pins, the outputs

are enabled and the device functions as a noninverting buffer. When a high level is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high impedance outputs.

LOGIC DETAIL



Octal 3-State Inverting Transparent Latch

High-Performance Silicon-Gate CMOS

The MC54/74HC563 is identical in pinout to the LS563. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is identical in function to the HC533 but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

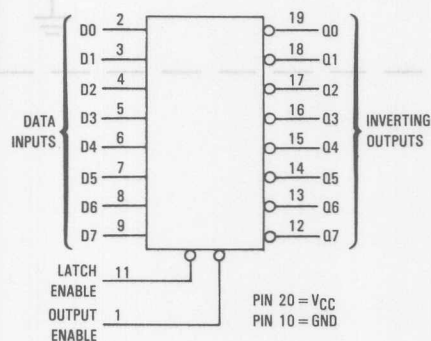
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. The data appears at the outputs in inverted form. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

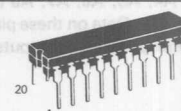
The HC573 is the noninverting version of this function.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates

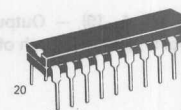
LOGIC DIAGRAM



MC54/74HC563



J SUFFIX
 CERAMIC
 CASE 732



N SUFFIX
 PLASTIC
 CASE 738



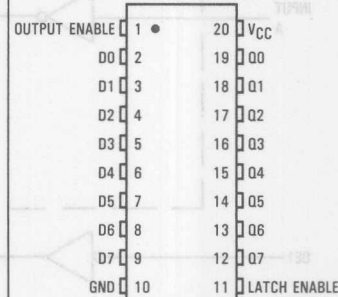
DW SUFFIX
 SOIC
 CASE 751D

ORDERING INFORMATION

MC74HCXXXN Plastic
 MC54HCXXXJ Ceramic
 MC74HCXXXDW SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	L
L	H	L	H
L	L	X	no change
H	X	X	Z

X = don't care
 Z = high impedance

MC54/74HC563

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V _{in} ,V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V _{CC}	V
T _A	Operating Temperature, All Package Types		− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		37	

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t _h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t _w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC563

SWITCHING WAVEFORMS

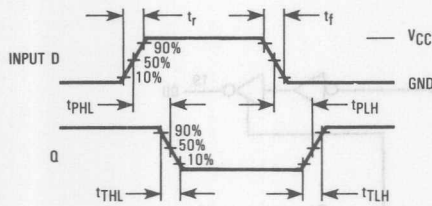


Figure 1

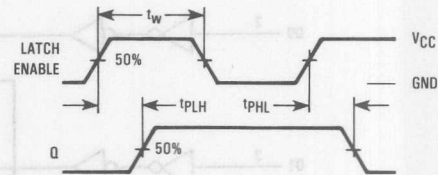


Figure 2

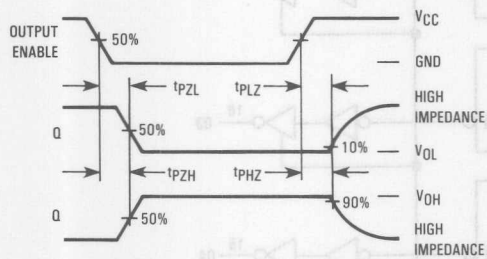


Figure 3

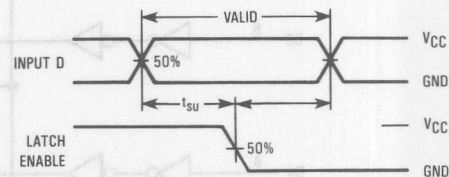
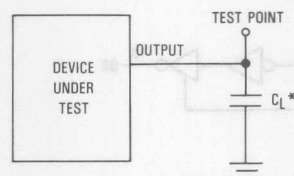
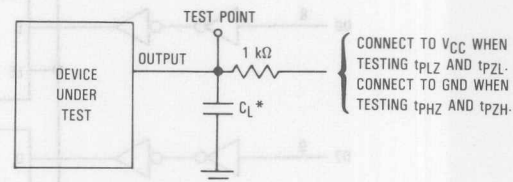


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

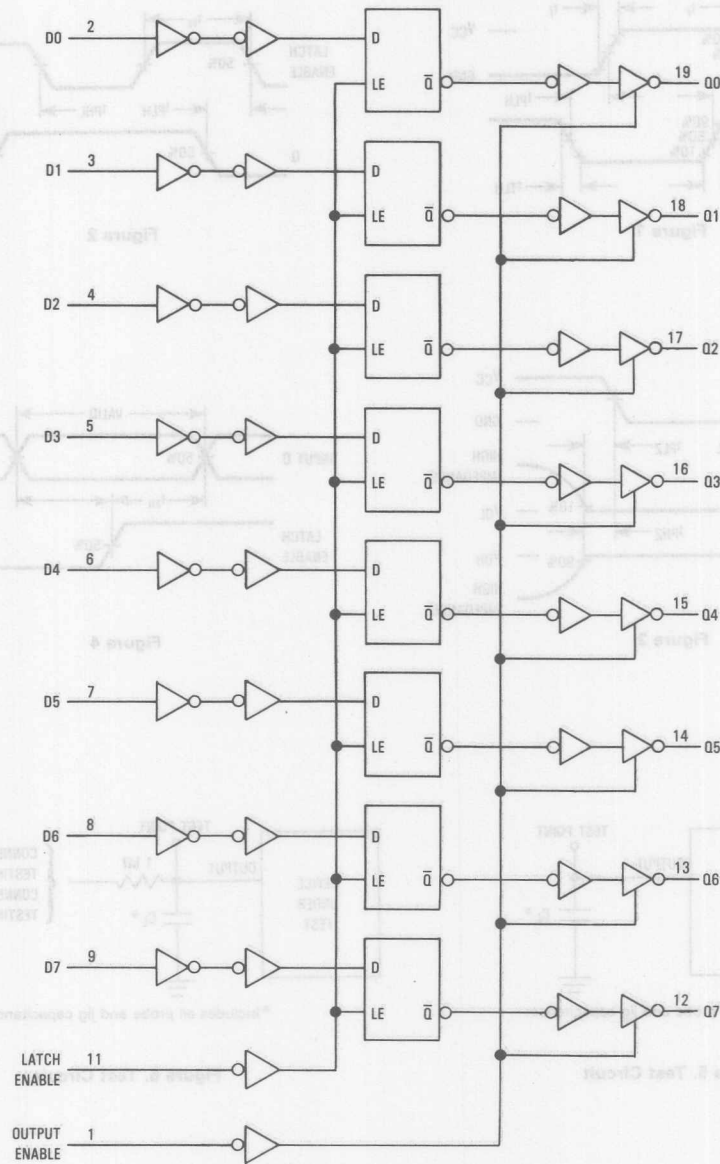


*Includes all probe and jig capacitance.

Figure 6. Test Circuit

MC54/74HC563

EXPANDED LOGIC DIAGRAM



5

Octal 3-State Inverting D Flip-Flop

High-Performance Silicon-Gate CMOS

The MC54/74HC564 is identical in pinout to the LS564. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

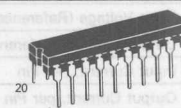
This device is identical in function to the HC534 but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

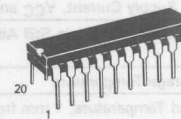
The HC564 is the inverting version of the HC574.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 282 FETs or 70.5 Equivalent Gates

MC54/74HC564



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



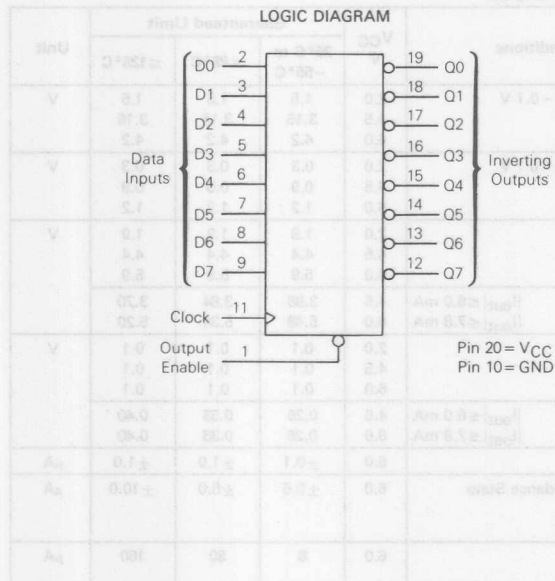
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Output Enable	1	20	V_{CC}
D0	2	19	Q0
D1	3	18	Q1
D2	4	17	Q2
D3	5	16	Q3
D4	6	15	Q4
D5	7	14	Q5
D6	8	13	Q6
D7	9	12	Q7
GND	10	11	Clock

FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L		H	L
L		L	H
L	L, H,	X	no change
H	X	X	Z

X = don't care
Z = high impedance

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC564

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		38	

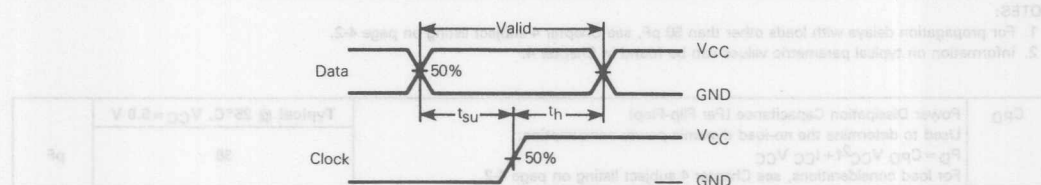
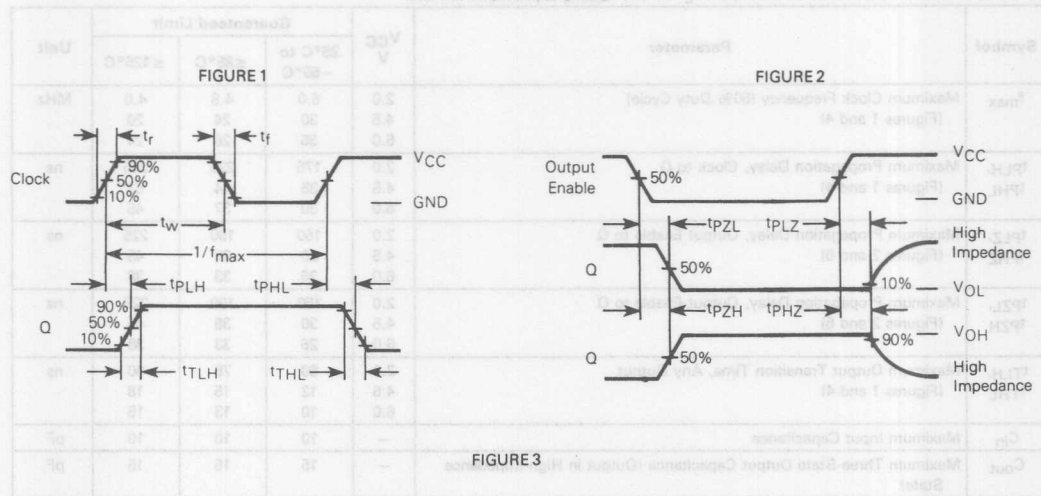
TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

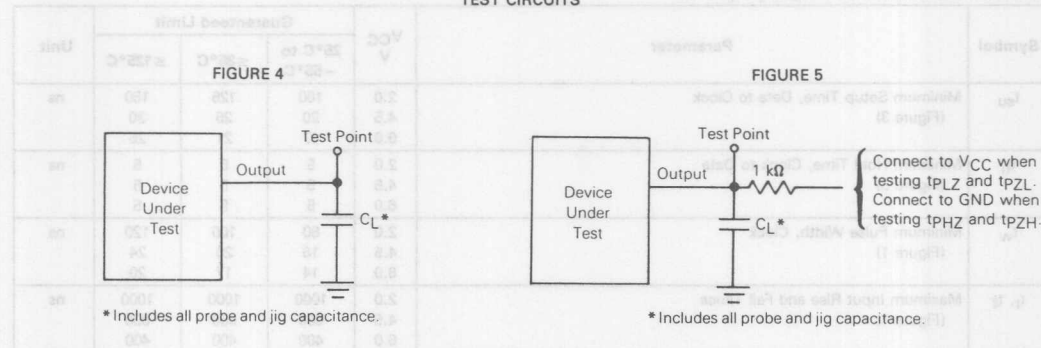
NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC564

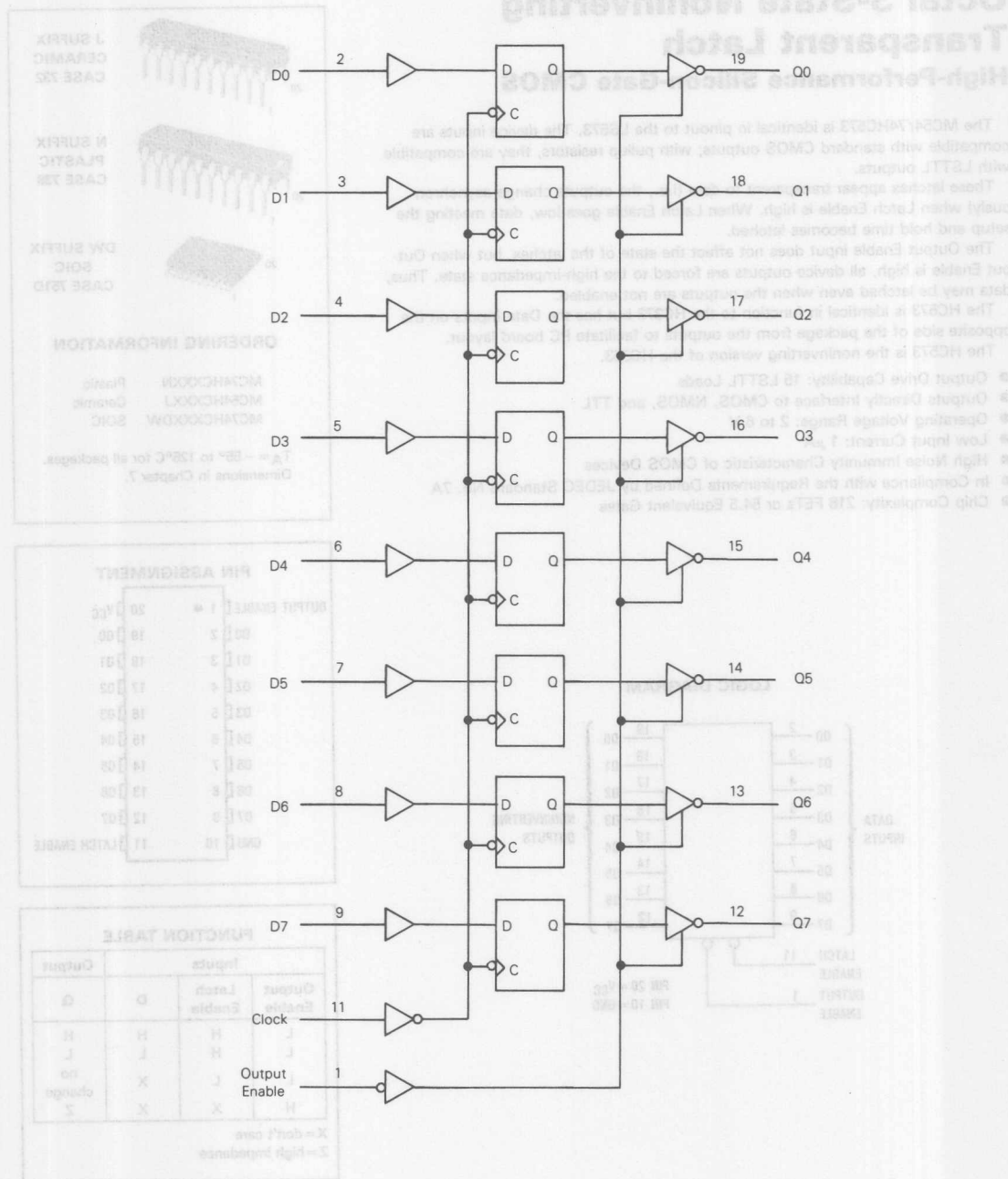
SWITCHING WAVEFORMS



TEST CIRCUITS



EXPANDED LOGIC DIAGRAM



Octal 3-State Noninverting Transparent Latch

High-Performance Silicon-Gate CMOS

The MC54/74HC573 is identical in pinout to the LS573. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

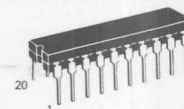
The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC573 is identical in function to the HC373 but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

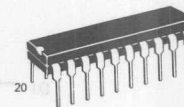
The HC573 is the noninverting version of the HC563.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates

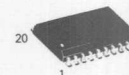
MC54/74HC573



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



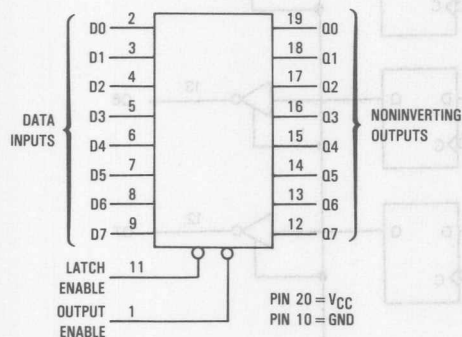
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXN Plastic
MC54HCXXJ Ceramic
MC74HCXXDW SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

OUTPUT ENABLE	1	20	V_{CC}
D0	2	19	Q0
D1	3	18	Q1
D2	4	17	Q2
D3	5	16	Q3
D4	6	15	Q4
D5	7	14	Q5
D6	8	13	Q6
D7	9	12	Q7
GND	10	11	LATCH ENABLE

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MC54/74HC573

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} ,V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC573

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	
		37	pF

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
t _h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC573

SWITCHING WAVEFORMS

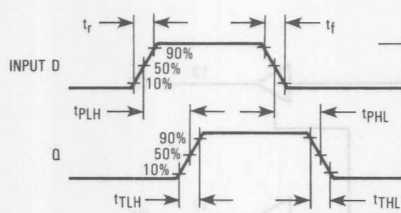


Figure 1

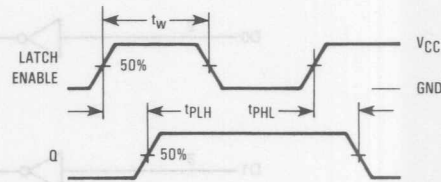


Figure 2

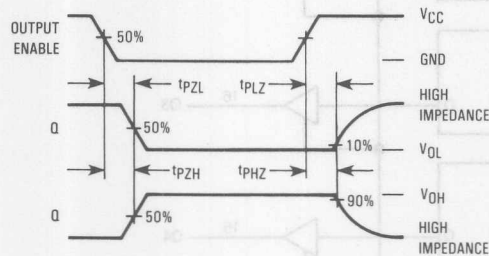


Figure 3

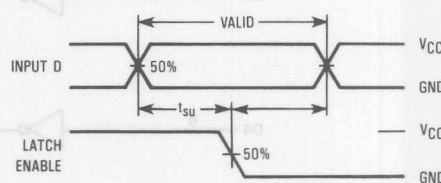
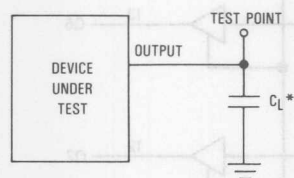
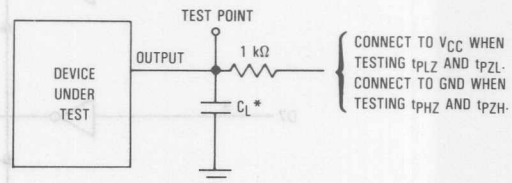


Figure 4



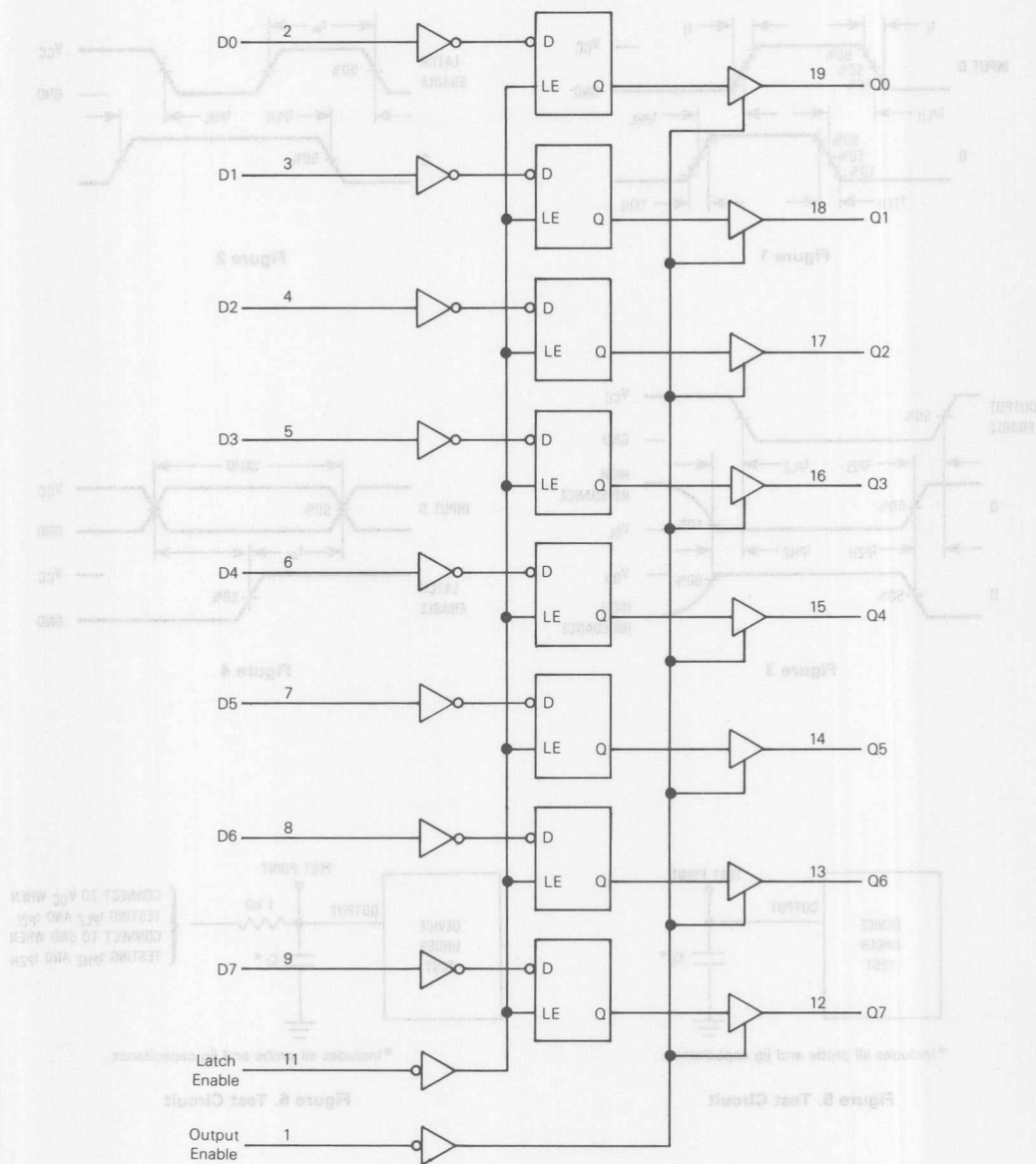
*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit



MC54/74HC574

Octal 3-State Noninverting D Flip-Flop High-Performance Silicon-Gate CMOS

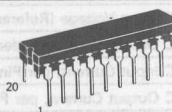
The MC54/74HC574 is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

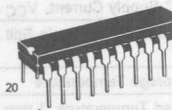
The HC574 is identical in function to the HC374 but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC574 is the noninverting version of the HC564.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 732**



**N SUFFIX
PLASTIC
CASE 738**



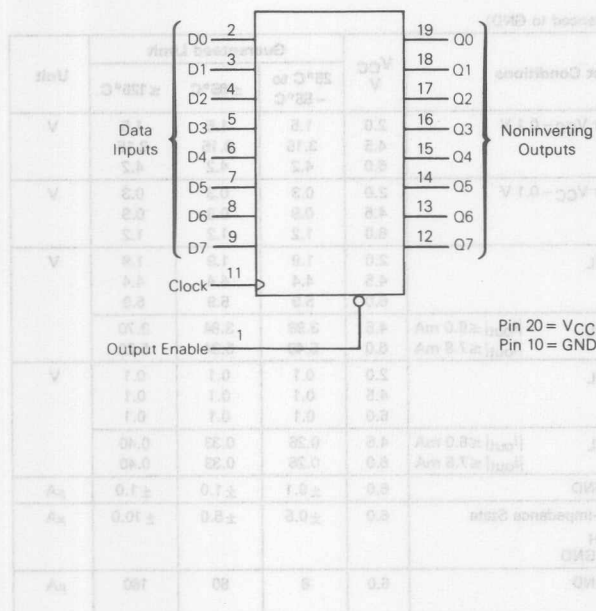
**DW SUFFIX
SOIC
CASE 751D**

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Output Enable	1	20	VCC
D0	2	19	Q0
D1	3	18	Q1
D2	4	17	Q2
D3	5	16	Q3
D4	6	15	Q4
D5	7	14	Q5
D6	8	13	Q6
D7	9	12	Q7
GND	10	11	Clock

FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L		H	H
L		L	L
L	L, H,	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC574

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

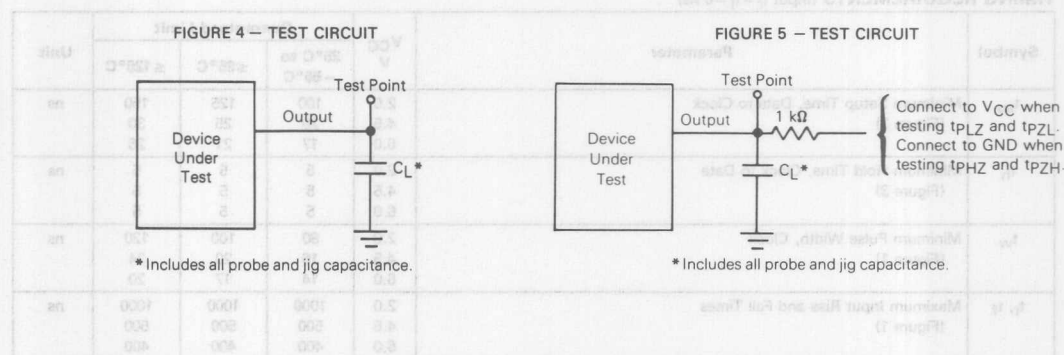
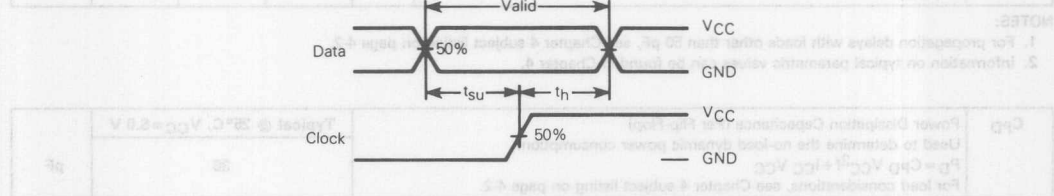
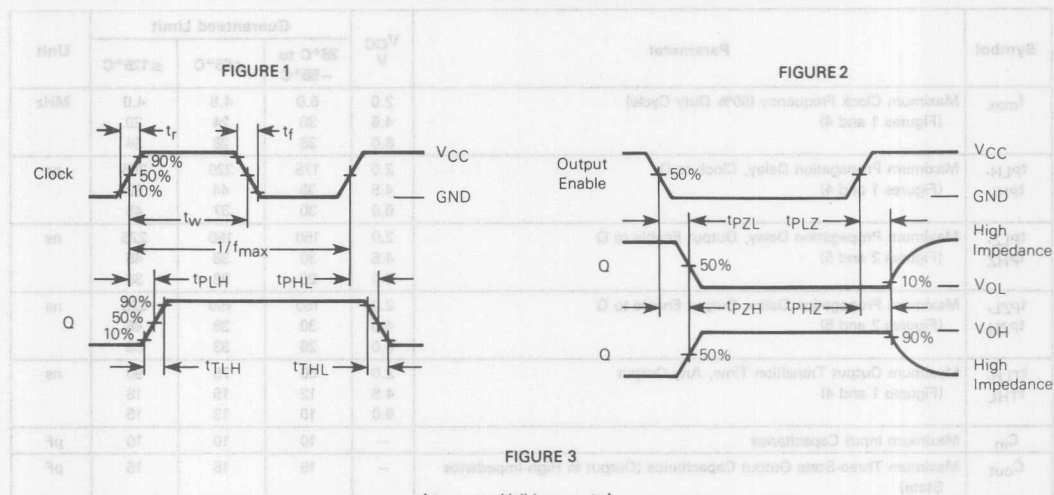
- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$	pF
		38	

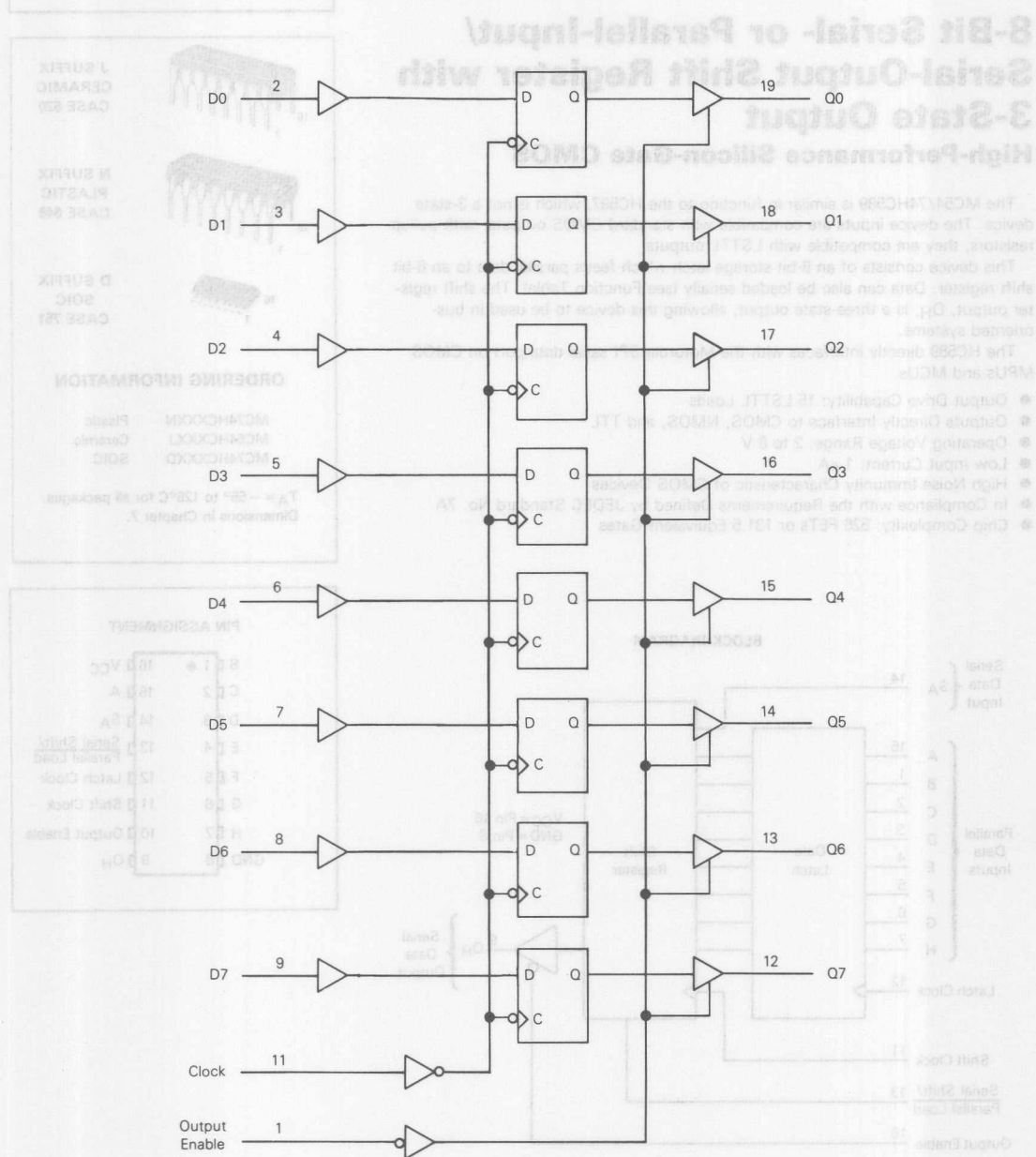
TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.



EXPANDED LOGIC DIAGRAM



MC54/74HC589

8-Bit Serial- or Parallel-Input/ Serial-Output Shift Register with 3-State Output

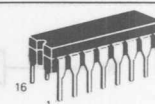
High-Performance Silicon-Gate CMOS

The MC54/74HC589 is similar in function to the HC597, which is not a 3-state device. The device inputs are compatible with standard TTL outputs; with pullup resistors, they are compatible with LSTTL outputs.

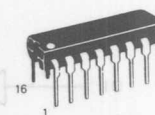
This device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table). The shift register output, Q_H , is a three-state output, allowing this device to be used in bus-oriented systems.

The HC589 directly interfaces with the Motorola SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates



J SUFFIX
 CERAMIC
 CASE 620



N SUFFIX
 PLASTIC
 CASE 648



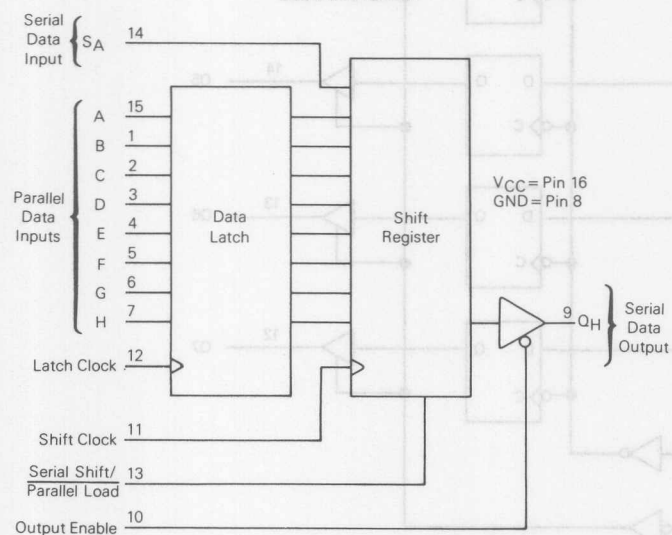
D SUFFIX
 SOIC
 CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

BLOCK DIAGRAM



PIN ASSIGNMENT

B	1	16	VCC
C	2	15	A
D	3	14	S _A
E	4	13	Serial Shift/ Parallel Load
F	5	12	Latch Clock
G	6	11	Shift Clock
H	7	10	Output Enable
GND	8	9	Q _H

MC54/74HC589

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC} = 2.0$ V	0	1000	
	$V_{CC} = 4.5$ V	0	500	
	$V_{CC} = 6.0$ V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _H (Figures 1 and 8)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to Q _H (Figures 2 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q _H (Figures 4 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q _H (Figures 3 and 9)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q _H (Figures 3 and 9)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	pF
		50	

MC54/74HC589

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, A-H to Latch Clock (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Serial Data Input S_A to Shift Clock (Figure 6)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Latch Clock to A-H (Figure 5)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input S_A (Figure 6)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_h	Minimum Hold Time, Shift Clock to Serial Shift/Parallel Load (Figure 7)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Output Enable	Serial Shift/Parallel Load	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A-H	Data Latch Contents	Shift Register Contents	Output Q_H
Force output into high-impedance state	H	X	X	X	X	X	X	X	Z
Load parallel data into data latch	L	H		L, H,	X	a-h	a-h	U	U
Transfer latch contents to shift register	L	L	L, H,	X	X	X	U	$LR_N \rightarrow SR_N$	LR_H
Contents of input latch and shift register are unchanged	L	H	L, H,	L, H,	X	X	U	U	U
Load parallel data into data latch and shift register	L	L		X	X	a-h	a-h	a-h	h
Shift serial data into shift register	L	H	X		D	X	*	$SR_A = D;$ $SR_N \rightarrow SR_N + 1$	$SR_G \rightarrow SR_H$
Load parallel data in data latch and shift serial data into shift register	L	H			D	a-h	a-h	$SR_A = D;$ $SR_N \rightarrow SR_N + 1$	$SR_G \rightarrow SR_H$

LR = latch register contents

SR = shift register contents

a-h = data at parallel data inputs A-H

D = data (L, H) at serial data input S_A

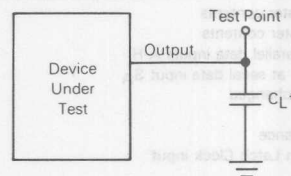
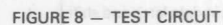
U = remains unchanged

X = don't care

Z = high impedance

* = depends on Latch Clock input

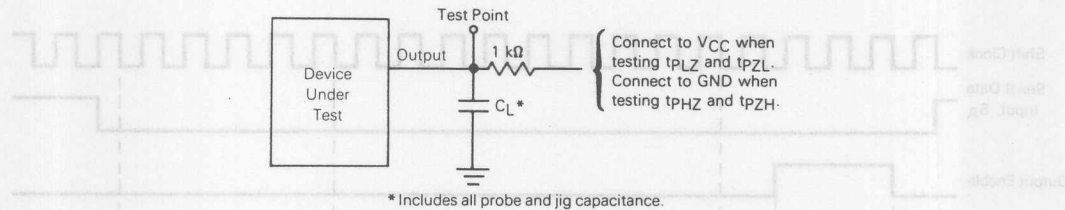
SWITCHING WAVEFORMS



* Includes all probe and jig capacitance.

MC54/74HC589

FIGURE 9 — TEST CIRCUIT



PIN DESCRIPTIONS

DATA INPUTS

A, B, C, D, E, F, G, H (PINS 15, 1, 2, 3, 4, 5, 6, 7) — Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

SA (PIN 14) — Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

CONTROL INPUTS

SERIAL SHIFT/PARALLEL LOAD (PIN 13) — Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

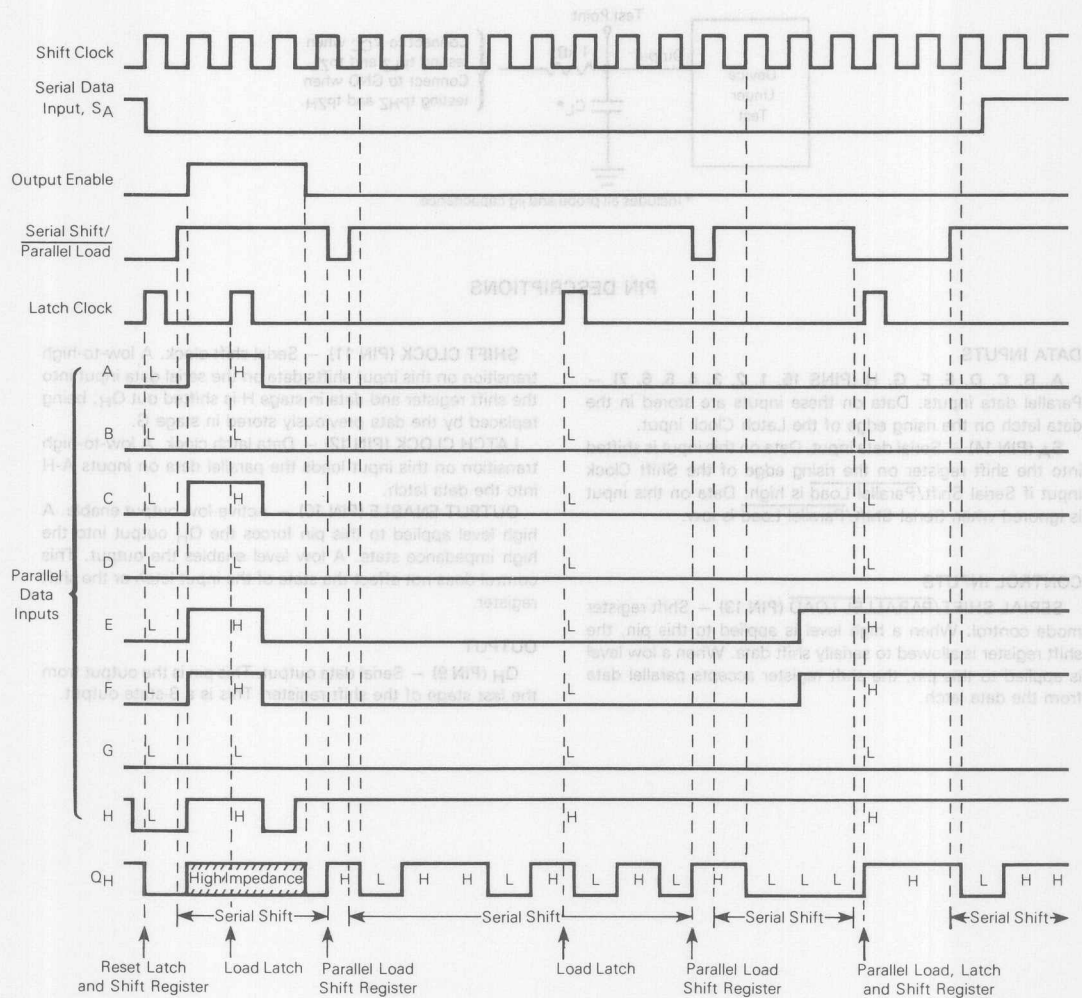
SHIFT CLOCK (PIN 11) — Serial shift clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

LATCH CLOCK (PIN 12) — Data latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the data latch.

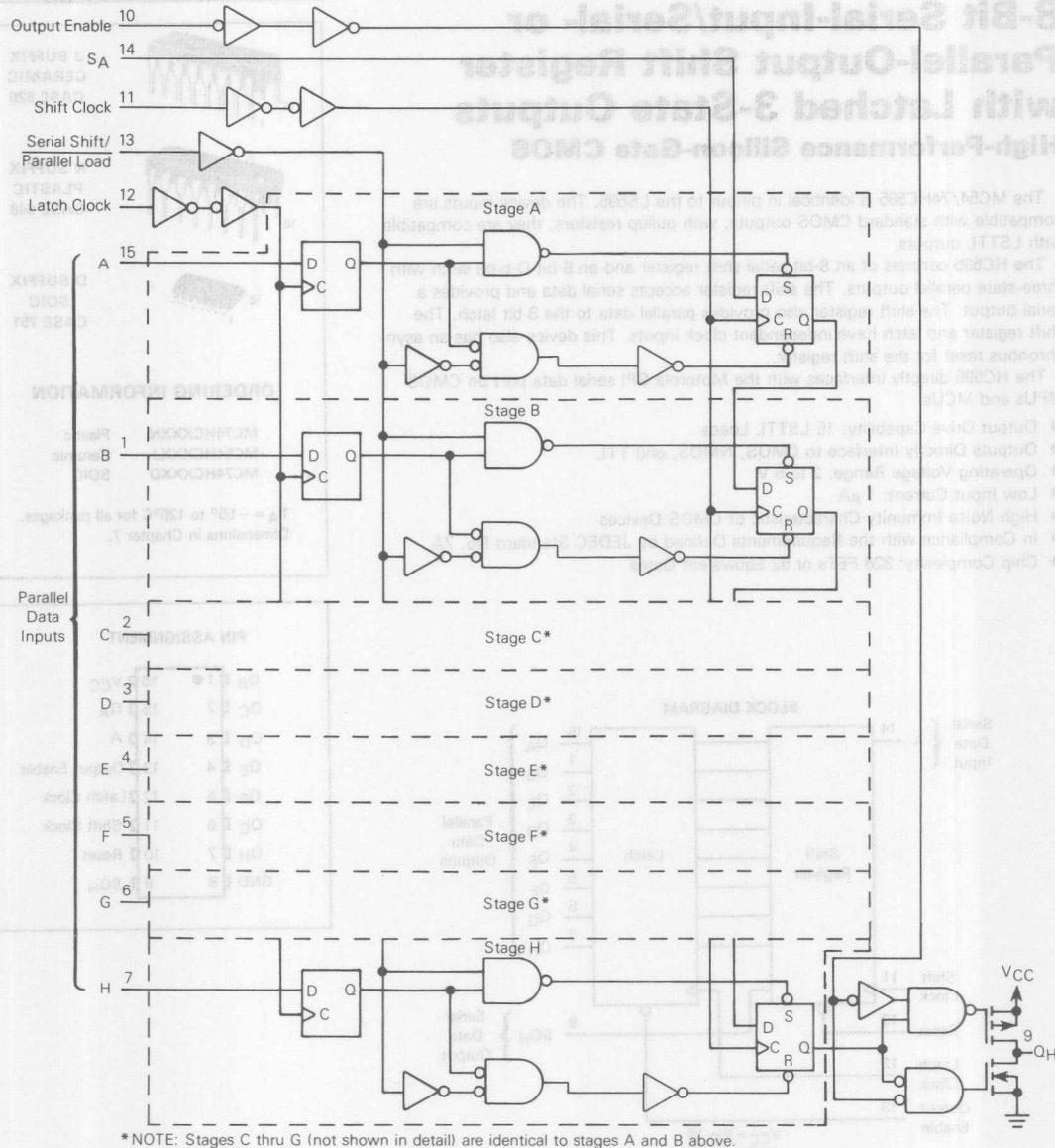
OUTPUT ENABLE (PIN 10) — Active-low output enable. A high level applied to this pin forces the Q_H output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

OUTPUT

QH (PIN 9) — Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.



LOGIC DETAIL



8-Bit Serial-Input/Serial- or Parallel-Output Shift Register with Latched 3-State Outputs

High-Performance Silicon-Gate CMOS

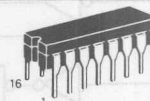
The MC54/74HC595 is identical in pinout to the LS595. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC595 consists of an 8-bit serial shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

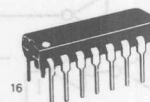
The HC595 directly interfaces with the Motorola SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates

MC54/74HC595



J SUFFIX
 CERAMIC
 CASE 620



N SUFFIX
 PLASTIC
 CASE 648



D SUFFIX
 SOIC
 CASE 751

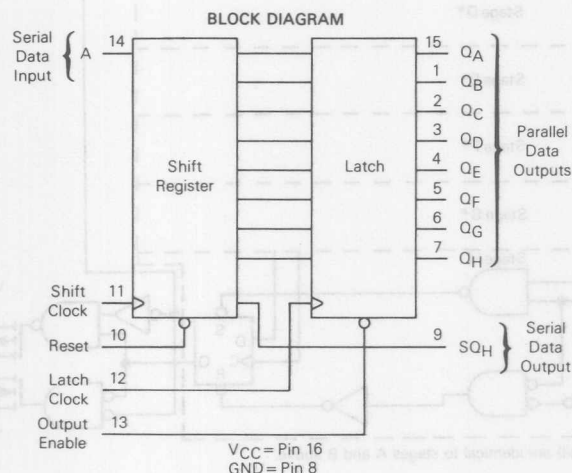
ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT

Q _B	1	16	V _{CC}
Q _C	2	15	Q _A
Q _D	3	14	A
Q _E	4	13	Output Enable
Q _F	5	12	Latch Clock
Q _G	6	11	Shift Clock
Q _H	7	10	Reset
GND	8	9	SQ _H



MC54/74HC595

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage, Q_A - Q_H	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage, Q_A - Q_H	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V

5

Symbol	Parameter	Test Conditions	V _{CC} V	25°C to -55°C	≤85°C	≤125°C	Unit
V _{OH}	Minimum High-Level Output Voltage, S _{QH}	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V _{OL}	Maximum Low-Level Output Voltage, S _{QH}	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	3.98	3.84	3.70	V
			6.0	5.48	5.34	5.20	
			6.0	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	2.0	0.1	0.1	0.1	μA
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I _{OZ}	Maximum Three-State Leakage Current, Q _A -Q _H	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	0.1	0.1	0.1	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	2.0	8	80	160	μA
			4.5	8	80	160	
			6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to S _{QH} (Figures 1 and 7)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t _{PHL}	Maximum Propagation Delay, Reset to S _{QH} (Figures 2 and 7)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _A -Q _H (Figures 3 and 7)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q _A -Q _H (Figures 4 and 8)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q _A -Q _H (Figures 4 and 8)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A -Q _H (Figures 3 and 7)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t _{TLH} , t _{THL}	Maximum Output Transition Time, S _{QH} (Figures 1 and 7)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q _A -Q _H	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		300	

MC54/74HC595

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ _H	Parallel Outputs Q _A -Q _H
Reset shift register	L	X	X	L, H,	L	L	U	L	U
Shift data into shift register	H	D		L, H,	L	D → SR _A ; SR _N → SR _{N+1}	U	SR _G → SR _H	U
Shift register remains unchanged	H	X	L, H,	L, H,	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H,		L	U	SR _N → LR _N	U	SR _N
Latch register remains unchanged	X	X	X	L, H,	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high-impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents
LR = latch register contents

D = data (L, H) logic level
U = remains unchanged

X = don't care
Z = high impedance

* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS

A (Pin 14) — Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

CONTROL INPUTS

Shift Clock (Pin 11) — Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

Reset (Pin 10) — Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

Latch Clock (Pin 12) — Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

Output Enable (Pin 13) — Active-low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A-Q_H) into the high-impedance state. The serial output is not affected by this control input.

OUTPUTS

Q_A-Q_H (Pins 15, 1, 2, 3, 4, 5, 6, 7) — Noninverted, 3-state, latch outputs.

SQ_H (Pin 9) — Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

MC54/74HC595

SWITCHING WAVEFORMS

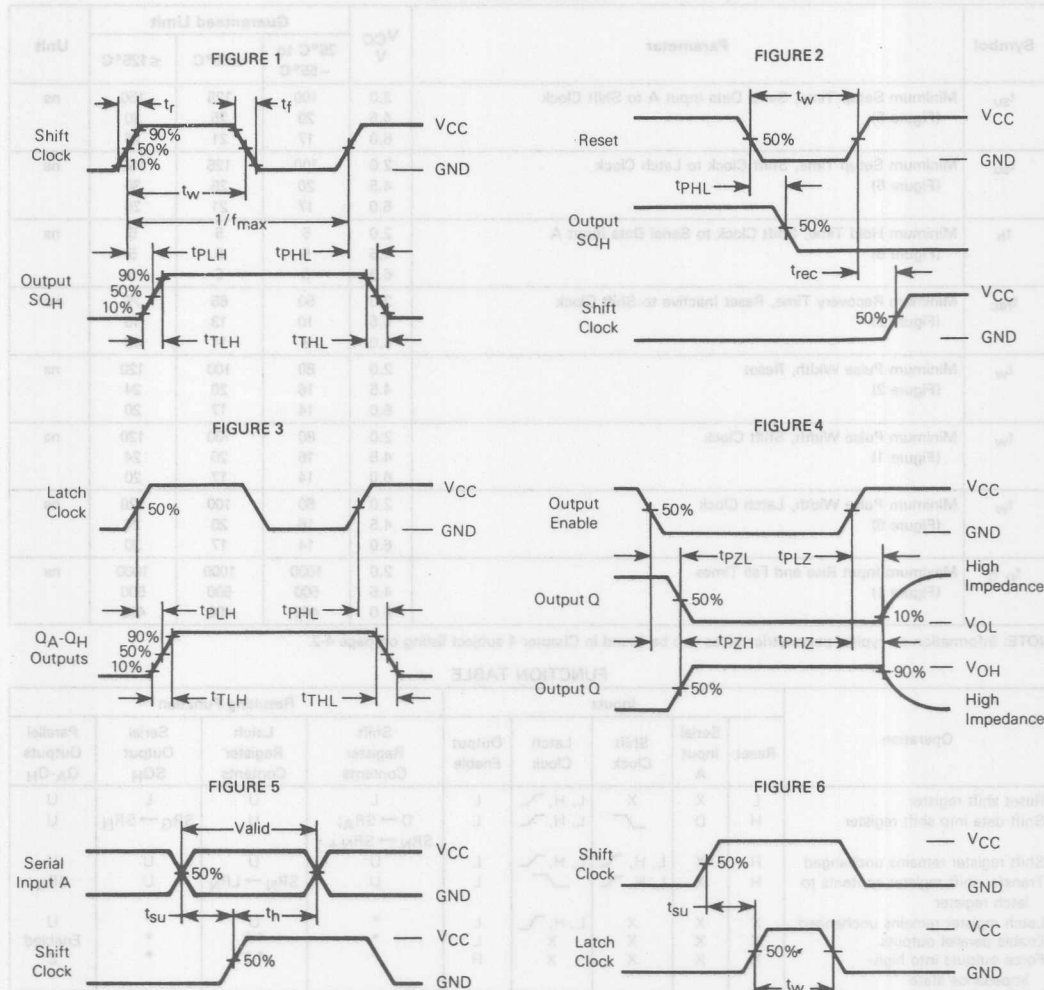


FIGURE 7 — TEST CIRCUIT

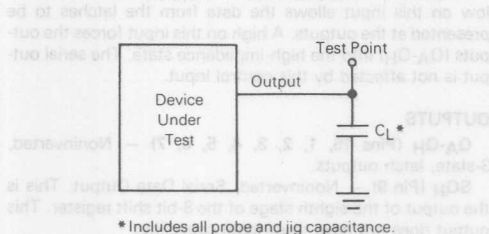
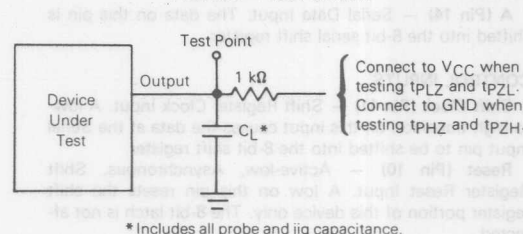
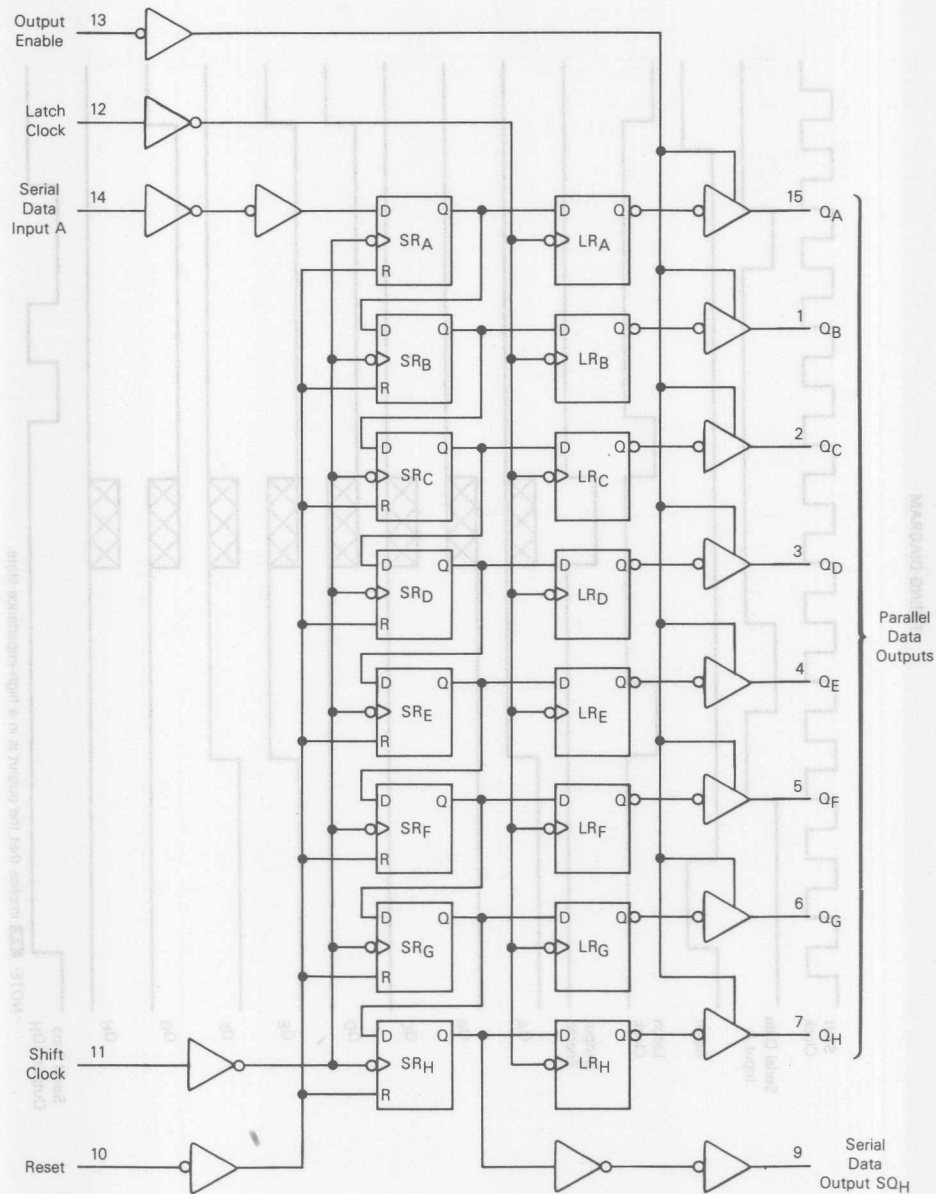


FIGURE 8 — TEST CIRCUIT

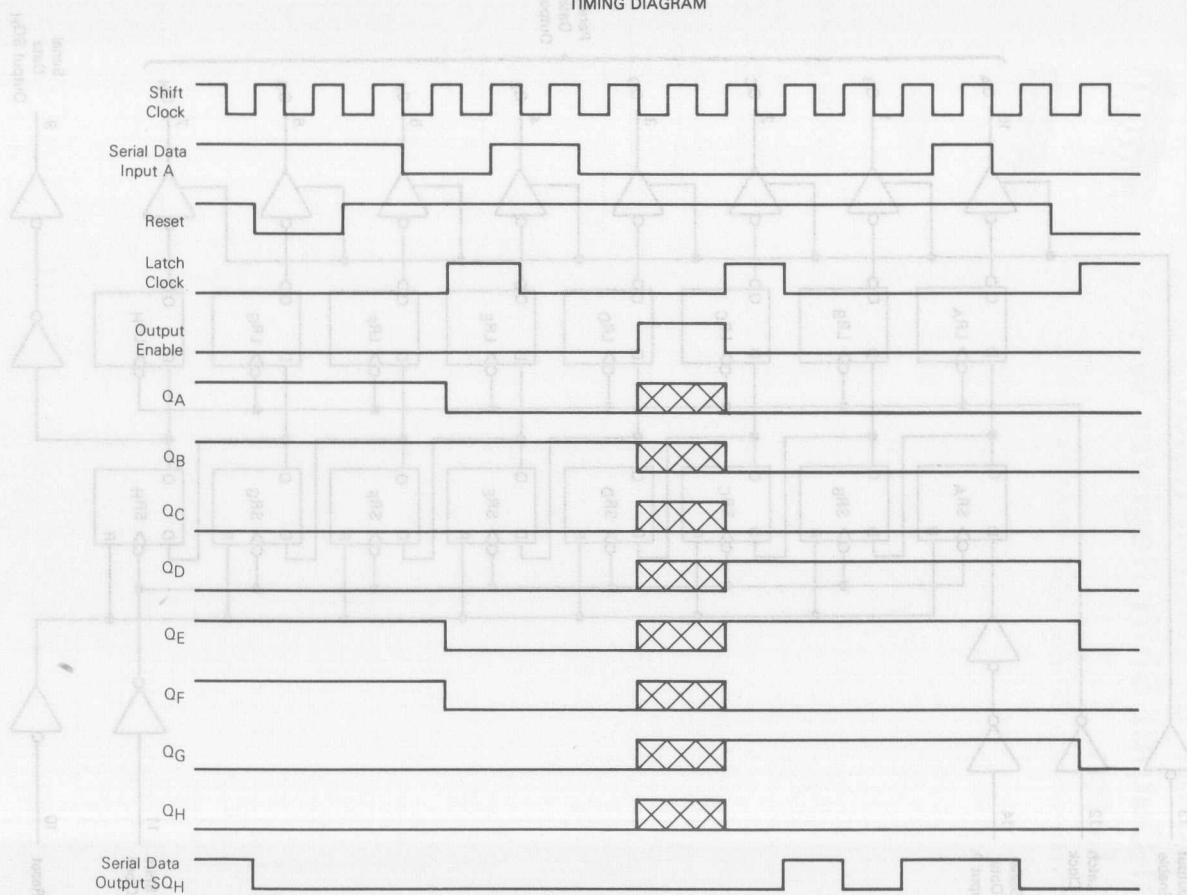


MC54/74HC595

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



8-Bit Serial- or Parallel-Input/ Serial-Output Shift Register With Input Latch

High-Performance Silicon-Gate CMOS

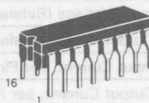
The MC54/74HC597 is identical in pinout to the LS597. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit input latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table).

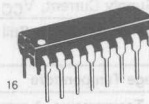
The HC597 is similar in function to the HC589, which is a 3-state device.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 516 FETs or 129 Equivalent Gates

MC54/74HC597



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



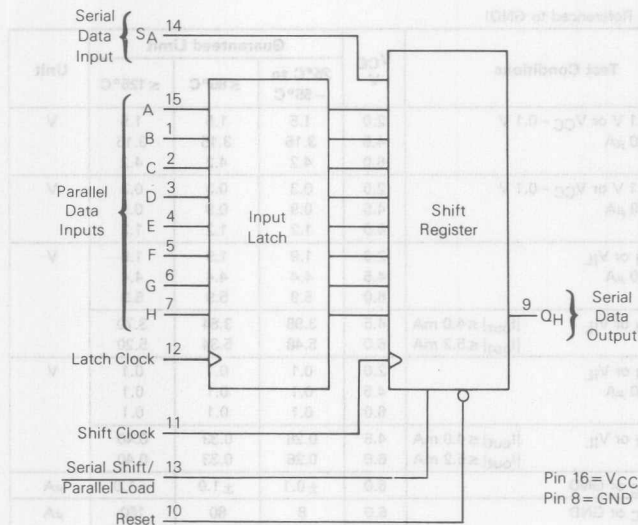
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

BLOCK DIAGRAM



PIN ASSIGNMENT

B	1	16	VCC
C	2	15	A
D	3	14	SA
E	4	13	Serial Shift/ Parallel Load
F	5	12	Latch Clock
G	6	11	Shift Clock
H	7	10	Reset
GND	8	9	QH

5

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} ,V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Typəs	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC597

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _H (Figures 1 and 8)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to Q _H (Figures 2 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q _H (Figures 3 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q _H (Figures 4 and 8)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		50	

PIN DESCRIPTIONS

DATA INPUTS

A, B, C, D, E, F, G, H (PINS 15, 1, 2, 3, 4, 5, 6, 7) — Parallel data inputs. Data on these inputs is stored in the input latch on the rising edge of the Latch Clock input.

S_A (PIN 14) — Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

CONTROL INPUTS

SERIAL SHIFT/PARALLEL LOAD (PIN 13) — Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the input latch, and serial shifting is inhibited.

RESET (PIN 10) — Asynchronous, Active-low shift register reset. A low level applied to this input resets the shift register to a low level, but does not change the data in the input latch.

SHIFT CLOCK (PIN 11) — Serial shift register clock. A low-to-high transition on this input shifts data on the Serial Data Input into the shift register and data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

LATCH CLOCK (PIN 12) — Latch clock. A low-to-high transition on this input loads the parallel data on inputs A-H into the input latch.

OUTPUT

Q_H (PIN 9) — Serial data output. This pin is the output from the last stage of the shift register.

		V	20°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Parallel Data Inputs A-H to Latch Clock (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Serial Data Input S_A to Shift Clock (Figure 6)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Latch Clock to Parallel Data Inputs A-H (Figure 5)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input S_A (Figure 6)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_w	Minimum Pulse Width, Latch Clock and Shift Clock (Figures 1 and 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 3)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Reset	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A-H	Latch Contents	Shift Register Contents	Output Q_H
Reset shift register	L	X	L, H,	X	X	X	U	L	L
Reset shift register; load parallel data into data latch	L	X		X	X	a-h	a-h	L	L
Load parallel data into data latch	H	H		L, H	X	a-h	a-h	U	U
Transfer latch contents to shift register	H	L	L, H	X	X	X	U	$LR_N \rightarrow SR_N$	LR_H
Contents of data latch and shift register are unchanged	H	H	L, H,	L, H,	X	X	U	U	U
Load parallel data into data latch and shift register	H	L		X	X	a-h	a-h	a-h	h
Shift serial data into shift register	H	H	X		D	X	*	$SR_A = D;$ $SR_N \rightarrow SR_N + 1$ $SR_A = D;$	$SR_G \rightarrow SR_H$
Load parallel data into data latch and shift serial data into shift register	H	H			D	a-h	a-h	$SR_N \rightarrow SR_N + 1$	$SR_G \rightarrow SR_H$

LR = latch register contents

SR = shift register contents

a-h = data at parallel data inputs A-H

D = data (L, H) at serial data input S_A

U = remains unchanged

X = don't care

* = depends on latch clock input

5

MC54/74HC597

SWITCHING WAVEFORMS

FIGURE 1—(Serial Shift/Parallel Load = L)

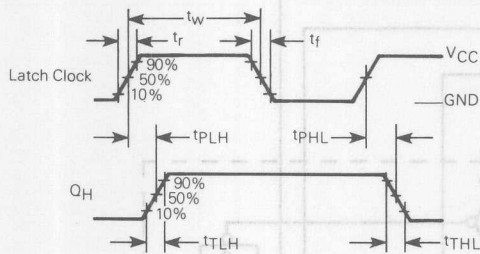


FIGURE 2—(Serial Shift/Parallel Load = H)

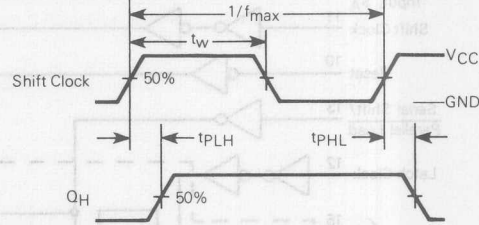


FIGURE 3

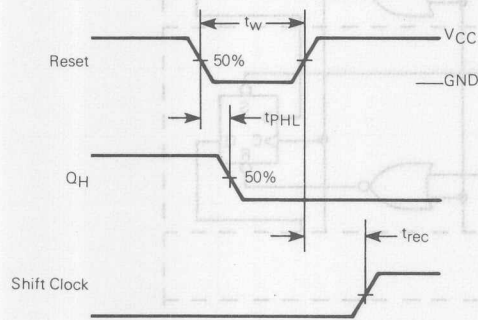


FIGURE 4

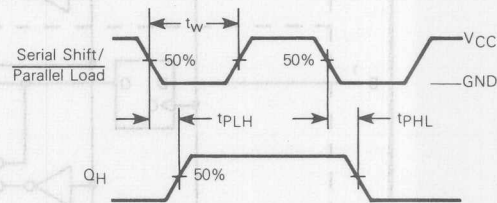


FIGURE 5

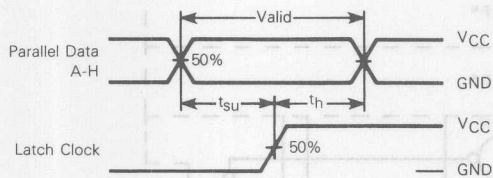


FIGURE 6

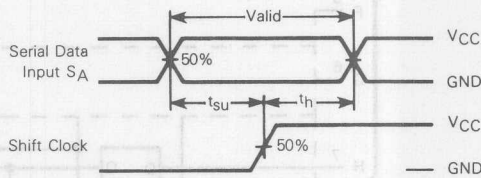


FIGURE 7

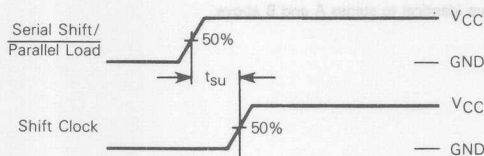
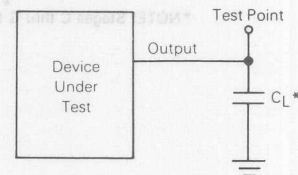


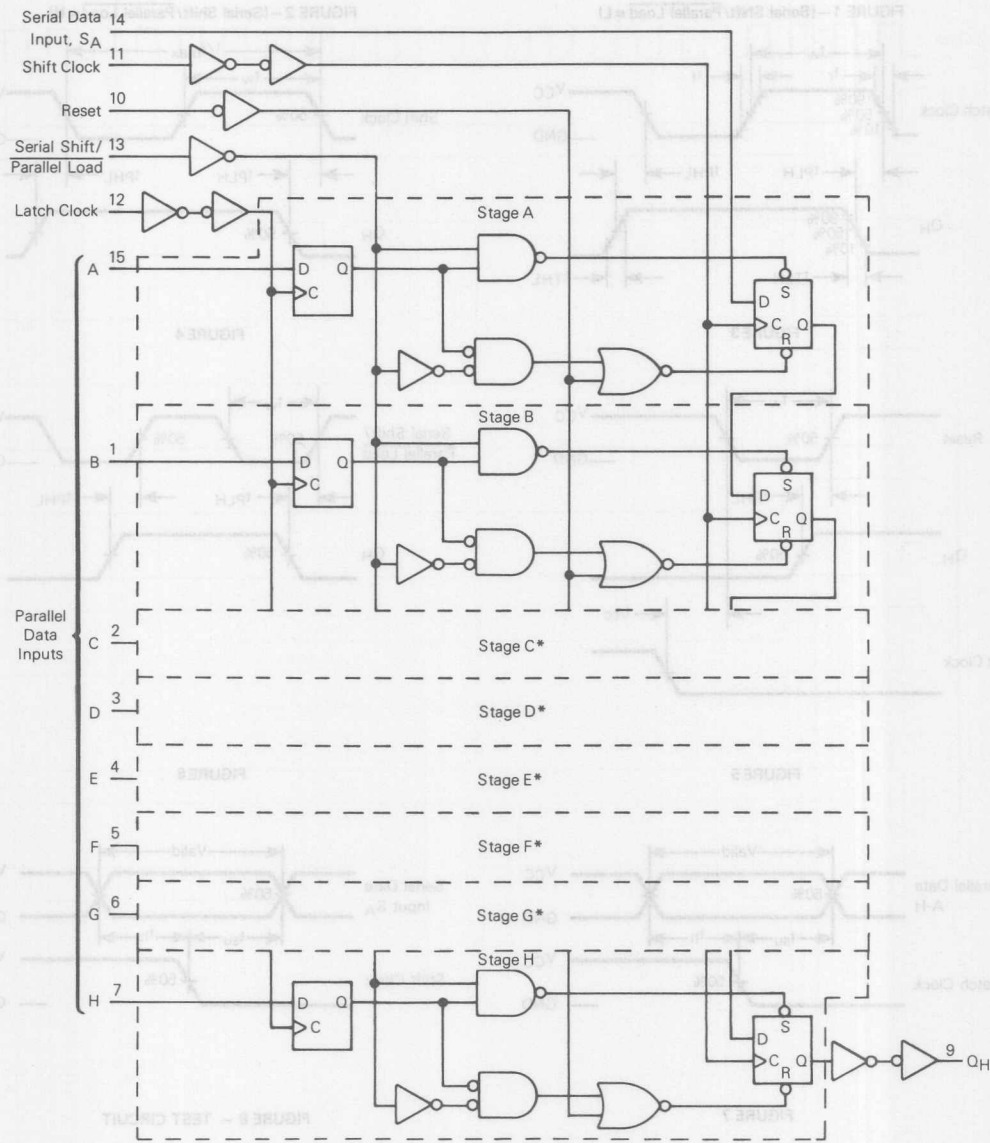
FIGURE 8 — TEST CIRCUIT



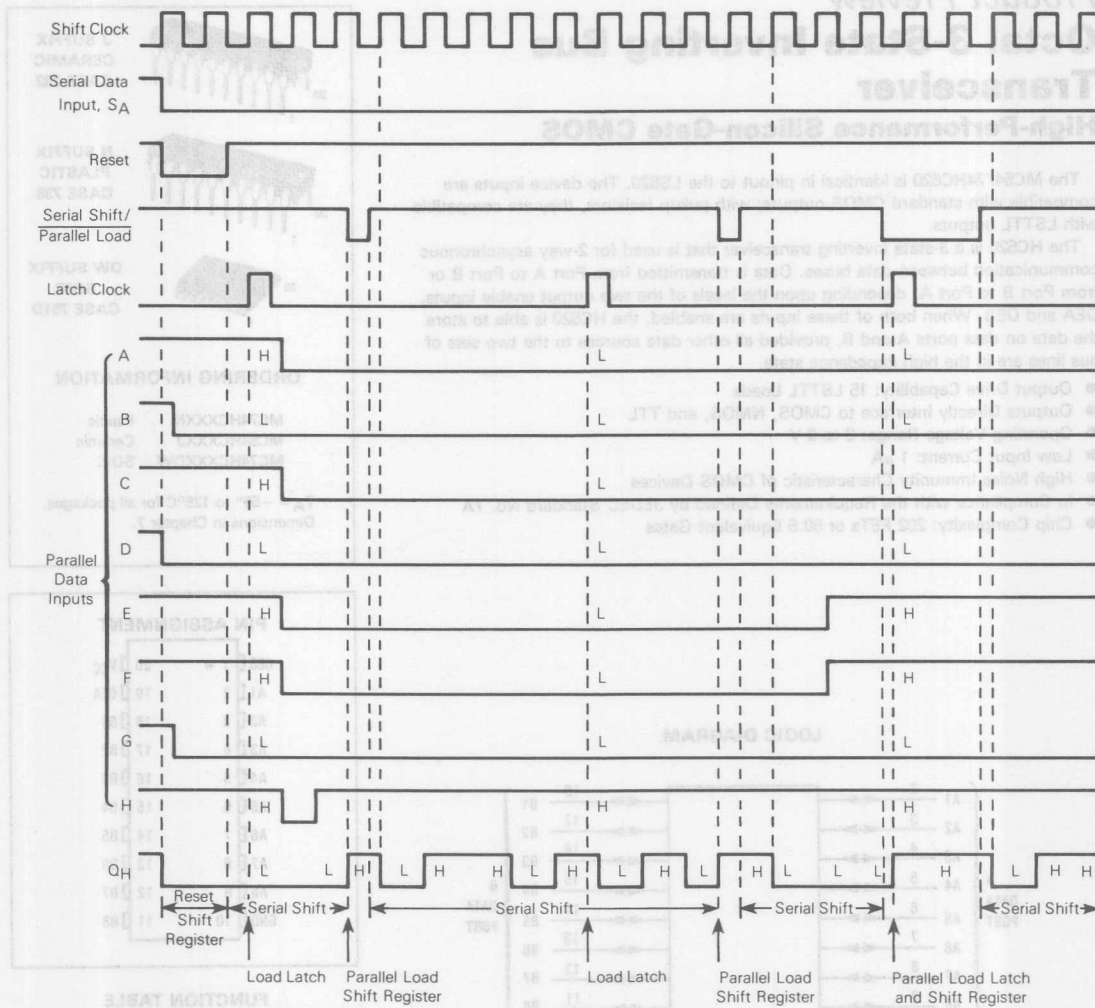
* Includes all probe and jig capacitance.

MC54/74HC597

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



5

Question	Output Enable	Output Enable
Q _A to Port A (inverted)	L	L
Q _B to Port B (inverted)	H	H
Q _C to Port C (inverted)	H	L
Q _D to Port D (inverted)	L	H
Q _E to Port E (inverted)	L	L
Q _F to Port F (inverted)	H	H
Q _G to Port G (inverted)	L	L
Q _H to Port H (inverted)	H	H

Product Preview

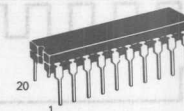
Octal 3-State Inverting Bus Transceiver

High-Performance Silicon-Gate CMOS

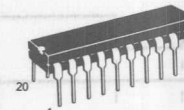
The MC54/74HC620 is identical in pinout to the LS620. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC620 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. Data is transmitted from Port A to Port B or from Port B to Port A, depending upon the levels of the two output enable inputs, OEA and OEB. When both of these inputs are enabled, the HC620 is able to store the data on data ports A and B, provided all other data sources to the two sets of bus lines are in the high impedance state.

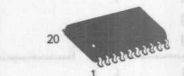
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



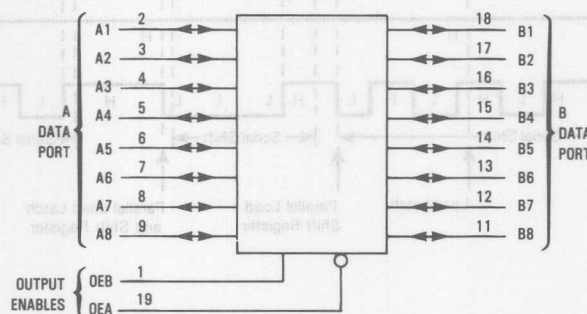
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 20 = V_{CC}
PIN 10 = GND

PIN ASSIGNMENT

OEB	1	20	V_{CC}
A1	2	19	OEA
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Output Enables		Operation
OEB	OEA	
L	L	Data transmitted from Port B to Port A (inverted)
H	H	Data transmitted from Port A to Port B (inverted)
L	H	Buses isolated (High-Impedance State)
H	L	Data transmitted from Port B to Port A (inverted) and from Port A to Port B (inverted)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74HC620

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin 1 or 19	± 20	mA
$I_{I/O}$	DC I/O Current, per I/O Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND, Pin 1 or 19}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND, I/O Pins}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC620

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

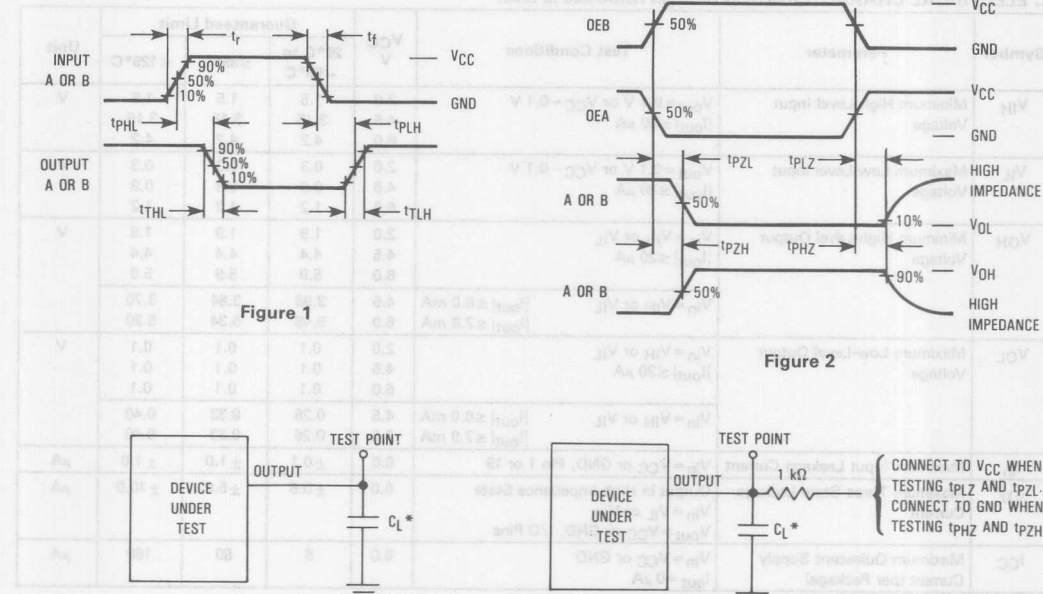
Symbol	Parameter	VCC V	Projected Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	pF
		40	

SWITCHING WAVEFORMS



*Includes all probe and jig capacitance.

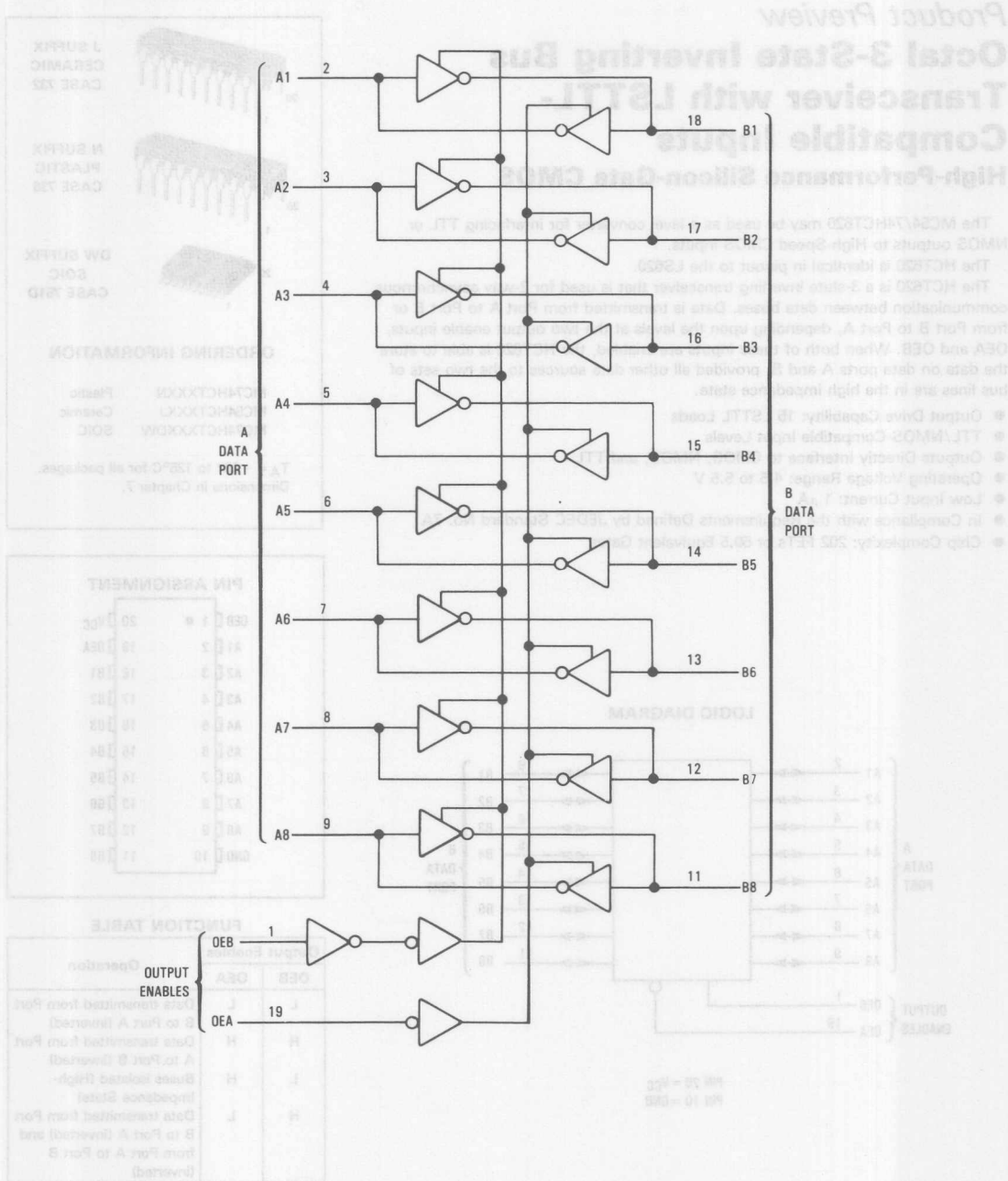
*Includes all probe and jig capacitance.

Figure 3. Test Circuit

Figure 4. Test Circuit

MC54/74HC620

EXPANDED LOGIC DIAGRAM



Product Preview

Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

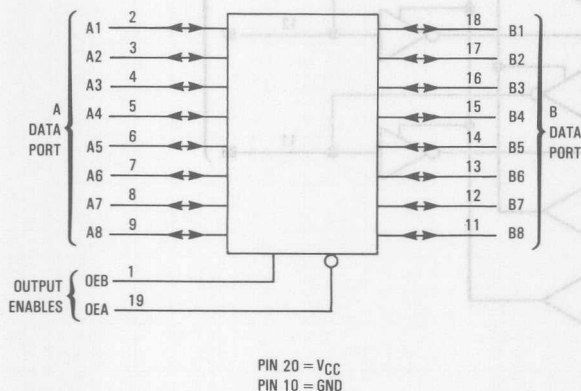
The MC54/74HCT620 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT620 is identical in pinout to the LS620.

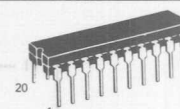
The HCT620 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. Data is transmitted from Port A to Port B or from Port B to Port A, depending upon the levels at the two output enable inputs, OEA and OEB. When both of these inputs are enabled, the HCT620 is able to store the data on data ports A and B, provided all other data sources to the two sets of bus lines are in the high impedance state.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates

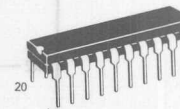
LOGIC DIAGRAM



MC54/74HCT620



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCTXXN	Plastic
MC54HCTXXJ	Ceramic
MC74HCTXXDW	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

OEB	1	20	V _{CC}
A1	2	19	OEA
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Output Enables		Operation
OEB	OEA	
L	L	Data transmitted from Port B to Port A (inverted)
H	H	Data transmitted from Port A to Port B (inverted)
L	H	Buses isolated (High-Impedance State)
H	L	Data transmitted from Port B to Port A (inverted) and from Port A to Port B (inverted)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74HCT620

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to V _{CC} + 1.5	V
V _{I/O}	DC I/O Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin 1 or 19	±20	mA
I _{I/O}	DC I/O Current, per I/O Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA	4.5	0.26	0.33	0.40	
		V _{in} = V _{CC} or GND, Pin 1 or 19	5.5	±0.1	±1.0	±1.0	
I _{in}	Maximum Input Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND, I/O Pins	5.5	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5	8	80	160	μA

ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = I_{CC} + ΣΔI_{CC}.

MC54/74HCT620

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	Projected Limit			Unit
		25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	22	28	33	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)	30	38	45	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)	30	38	45	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF
C _{out}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		45	

SWITCHING WAVEFORMS

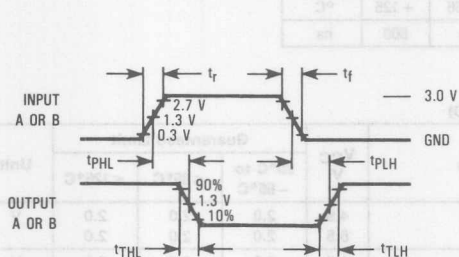


Figure 1

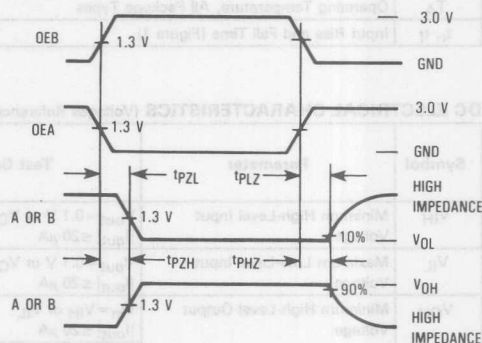
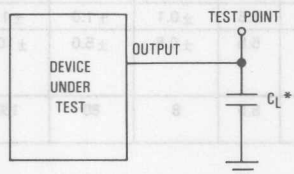
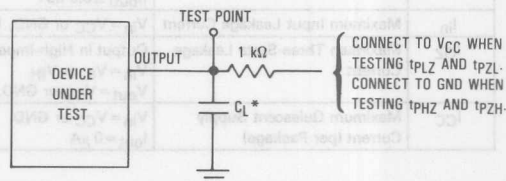


Figure 2



*Includes all probe and jig capacitance.

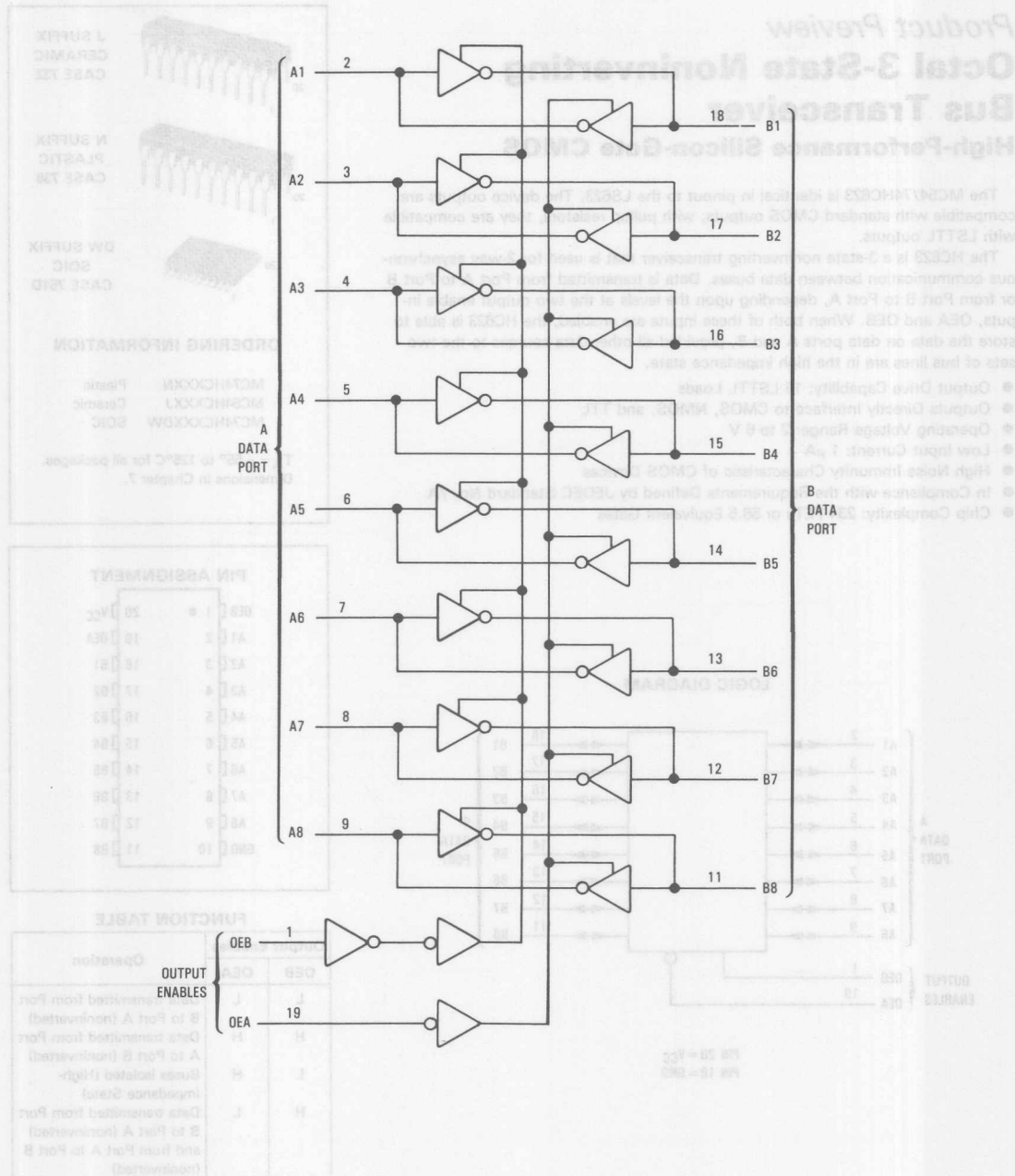
Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



Product Preview

Octal 3-State Noninverting Bus Transceiver

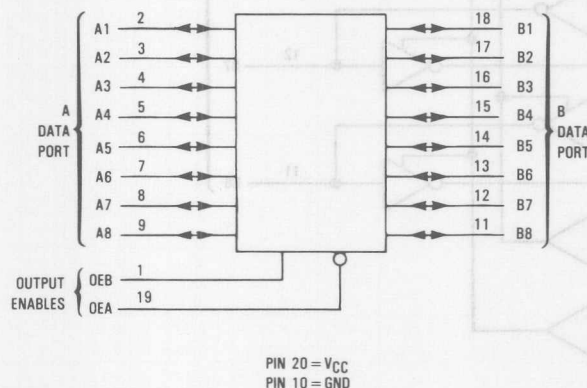
High-Performance Silicon-Gate CMOS

The MC54/74HC623 is identical in pinout to the LS623. The device outputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

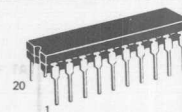
The HC623 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. Data is transmitted from Port A to Port B or from Port B to Port A, depending upon the levels at the two output enable inputs, OEA and OEB. When both of these inputs are enabled, the HC623 is able to store the data on data ports A and B, provided all other data sources to the two sets of bus lines are in the high impedance state.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates

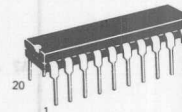
LOGIC DIAGRAM



MC54/74HC623



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN Plastic
MC54HCXXXJ Ceramic
MC74HCXXXDW SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

OEB	1	20	V _{CC}
A1	2	19	OEA
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Output Enables		Operation
OEB	OEA	
L	L	Data transmitted from Port B to Port A (noninverted)
H	H	Data transmitted from Port A to Port B (noninverted)
L	H	Buses isolated (High-Impedance State)
H	L	Data transmitted from Port B to Port A (noninverted) and from Port A to Port B (noninverted)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74HC623

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin 1 or 19	± 20	mA
$I_{I/O}$	DC I/O Current, per I/O Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND, Pin 1 or 19}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND, I/O Pins}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC623

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Projected Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC=5.0 V	pF
		40	

SWITCHING WAVEFORMS

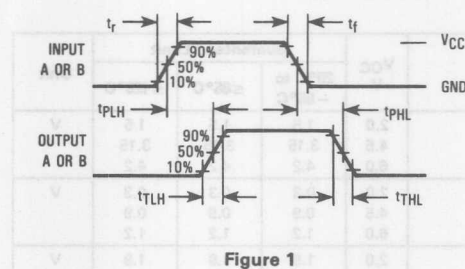


Figure 1

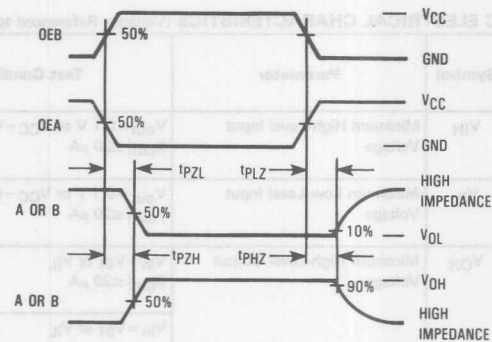
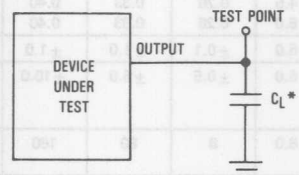
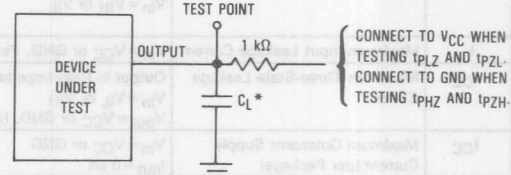


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

Product Preview

Octal 3-State Noninverting Bus Transceiver with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

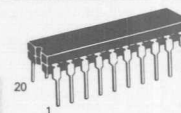
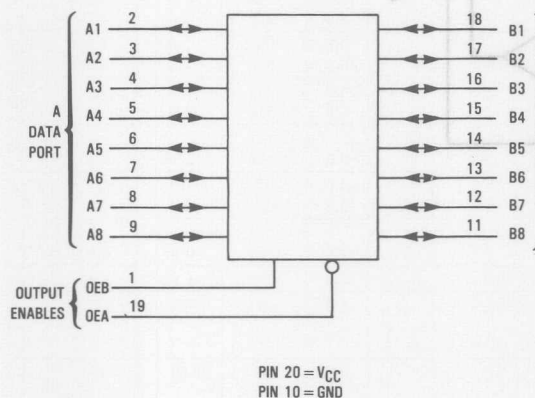
The MC54/74HCT623 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT623 is identical in pinout to the LS623.

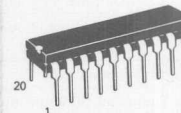
The HCT623 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. Data is transmitted from Port A to Port B or from Port B to Port A, depending upon the levels at the two output enable inputs, OEA and OEB. When both of these inputs are enabled, the HCT623 is able to store the data on data ports A and B, provided all other data sources to the two sets of bus lines are in the high impedance state.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates

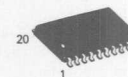
LOGIC DIAGRAM



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

OEB	1	20	V_{CC}
A1	2	19	OEA
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Output Enables		Operation
OEB	OEA	
L	L	Data transmitted from Port B to Port A (noninverted)
H	H	Data transmitted from Port A to Port B (noninverted)
L	H	Buses isolated (High-Impedance State)
H	L	Data transmitted from Port B to Port A (noninverted) and from Port A to Port B (noninverted)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74HCT623

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin 1 or 19	± 20	mA
$I_{I/O}$	DC I/O Current, per I/O Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND, Pin 1 or 19}$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND, I/O Pins}$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C	25°C to 125°C	mA
				2.9	2.4	

NOTES:

1. Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

2. Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT623

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Projected Limit			Unit
		25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	22	28	33	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)	30	38	45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, OEA or OEB to A or B (Figures 2 and 4)	30	38	45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		45	

SWITCHING WAVEFORMS

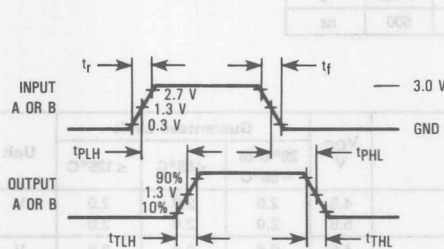


Figure 1

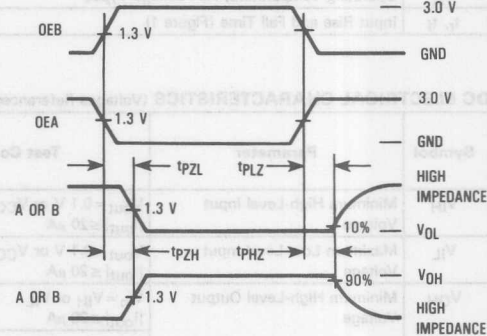
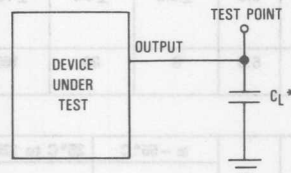
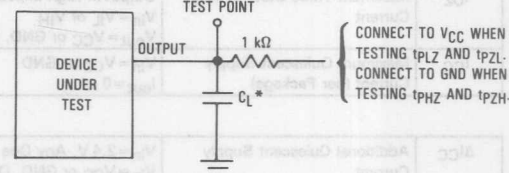


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit

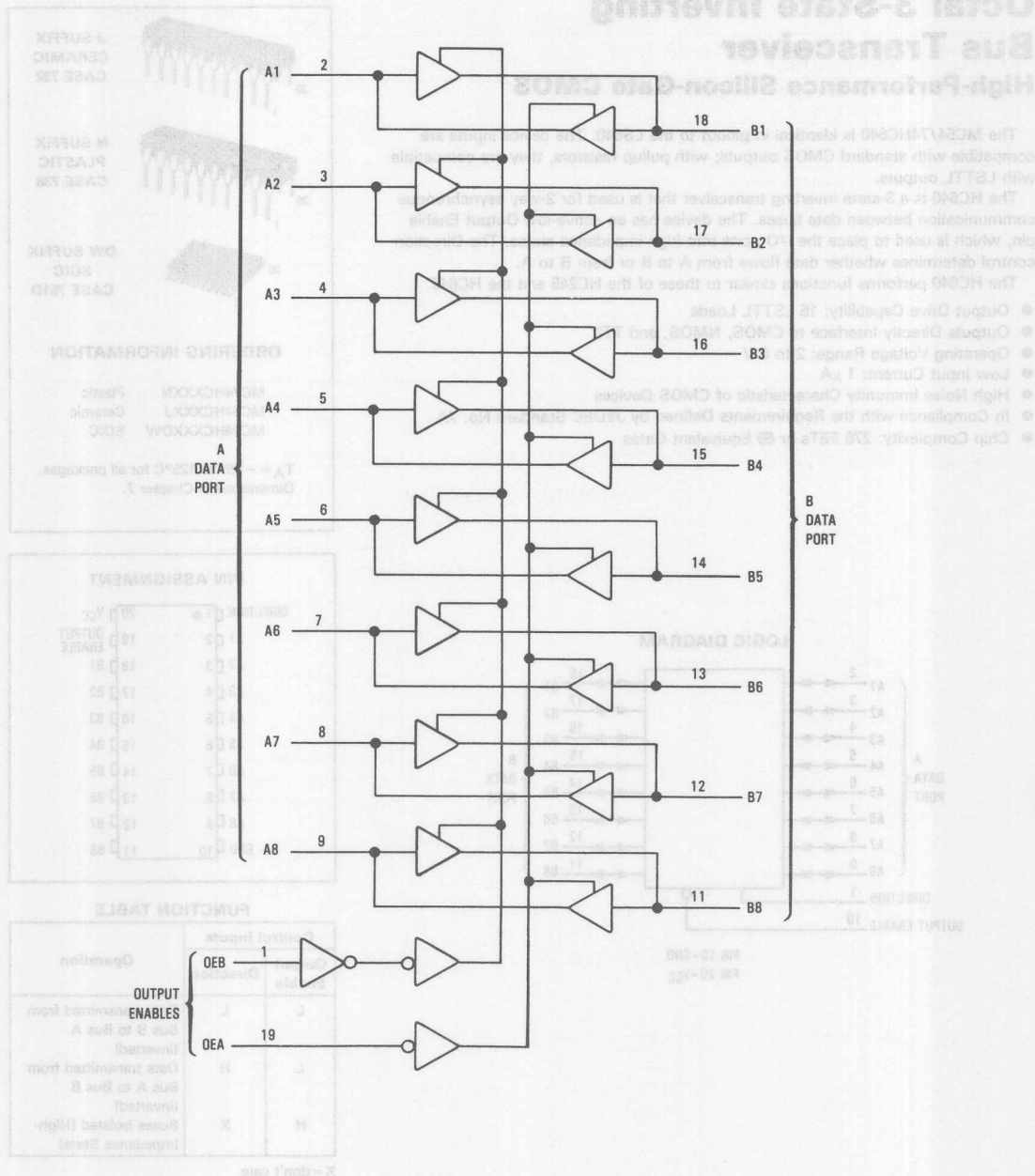


*Includes all probe and jig capacitance.

Figure 4. Test Circuit

MC54/74HCT623

EXPANDED LOGIC DIAGRAM



Octal 3-State Inverting Bus Transceiver

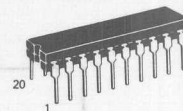
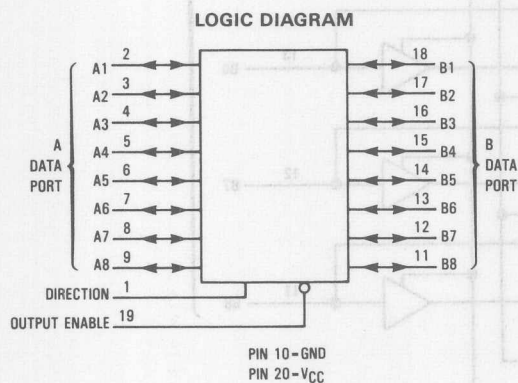
High-Performance Silicon-Gate CMOS

The MC54/74HC640 is identical in pinout to the LS640. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

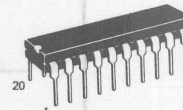
The HC640 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HC640 performs functions similar to those of the HC245 and the HC643.

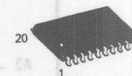
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 276 FETs or 69 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 732**



**N SUFFIX
PLASTIC
CASE 738**



**DW SUFFIX
SOIC
CASE 751D**

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

DIRECTION	1	20	V _{CC}
A1	2	19	OUTPUT ENABLE
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data transmitted from Bus B to Bus A (inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses isolated (High-Impedance State)

X = don't care

MC54/74HC640

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
$I_{I/O}$	DC I/O Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND, Pin 1 or 19}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC640

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance, Pin 1 or 19	—	10	10	10	pF
C_{out}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		40	

SWITCHING WAVEFORMS

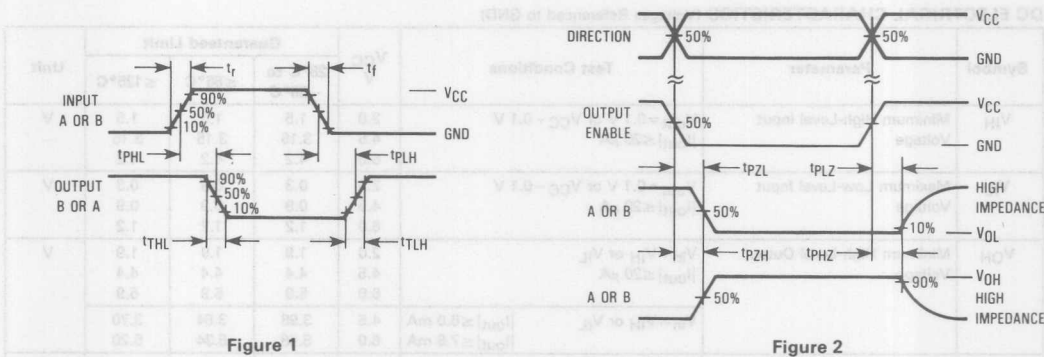
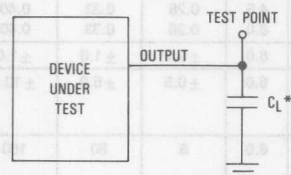


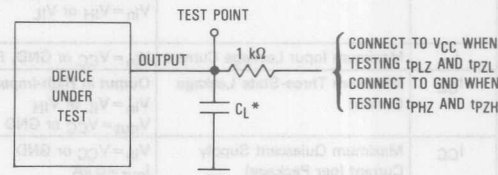
Figure 1

Figure 2



*Includes all probe and jig capacitance

Figure 3. Test Circuit

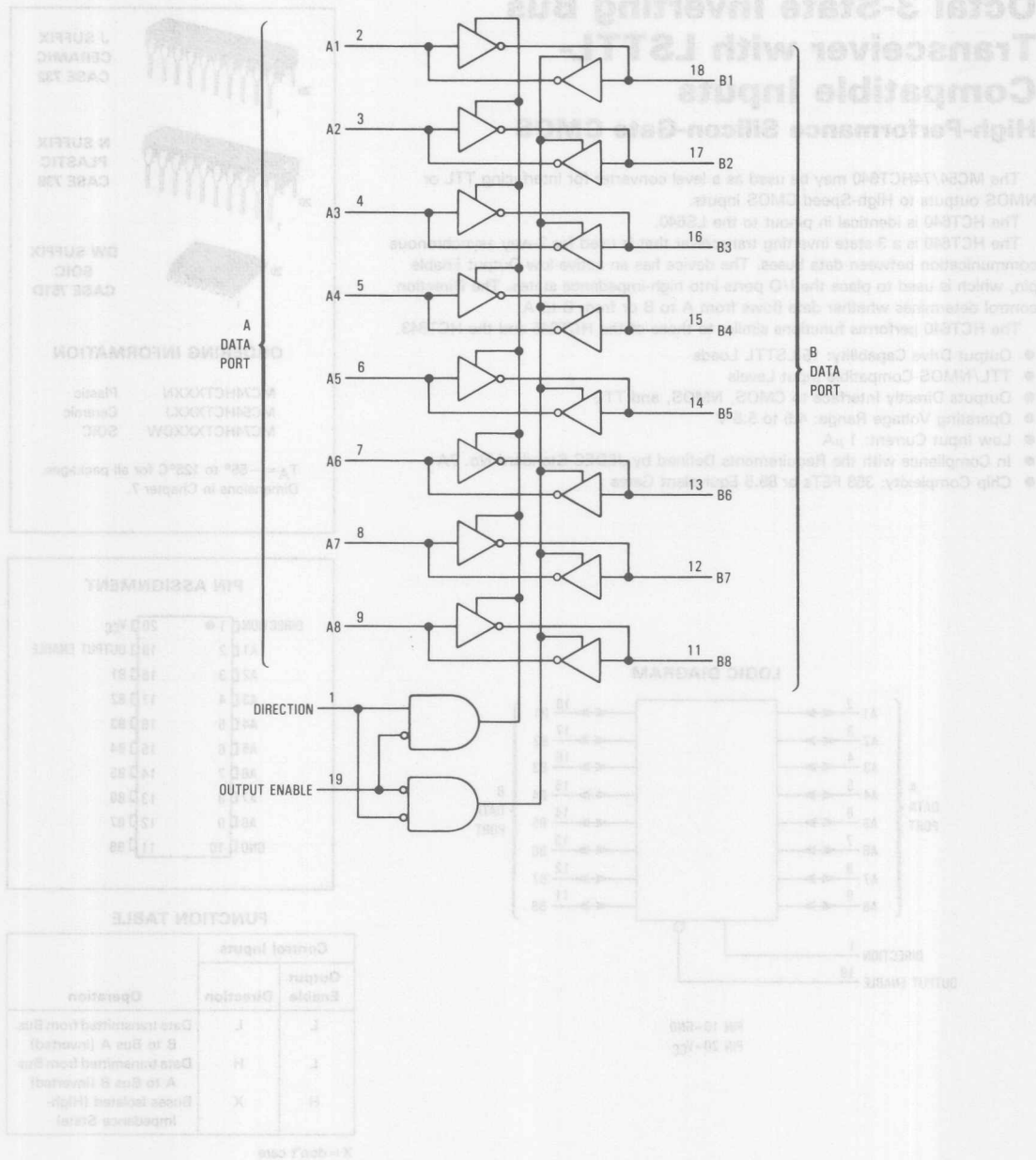


*Includes all probe and jig capacitance

Figure 4. Test Circuit

MC54/74HC640

EXPANDED LOGIC DIAGRAM



Octal 3-State Inverting Bus Transceiver with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

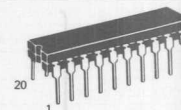
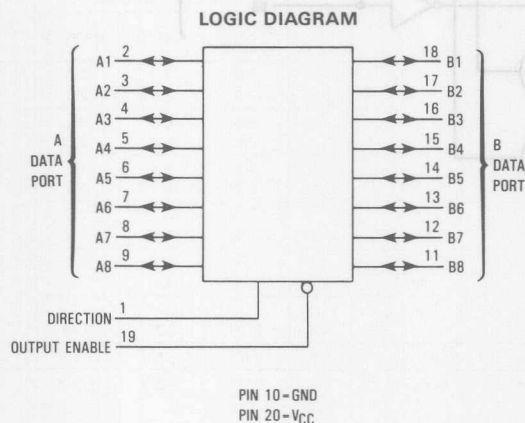
The MC54/74HCT640 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT640 is identical in pinout to the LS640.

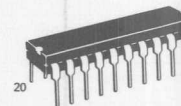
The HCT640 is a 3-state inverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HCT640 performs functions similar to those of the HCT245 and the HCT643.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 358 FETs or 89.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCTXXXN	Plastic
MC54HCTXXXJ	Ceramic
MC74HCTXXXDW	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

DIRECTION	1	20	V _{CC}
A1	2	19	OUTPUT ENABLE
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data transmitted from Bus B to Bus A (inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses Isolated (High-Impedance State)

X = don't care

MC54/74HCT640

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
$I_{I/O}$	DC I/O Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	V
			5.5	0.1	0.1	0.1	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	μA
			5.5	0.1	0.1	0.1	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND, I/O Pins}$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma I_{CC}$.

MC54/74HCT640

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to B or B to A (Figures 1 and 3)	22	28	33	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
t_{TLH} , t_{TLH}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance, Pin 1 or 19	10	10	10	pF
C_{out}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$	pF
		45	

SWITCHING WAVEFORMS

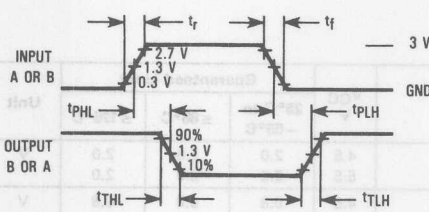


Figure 1

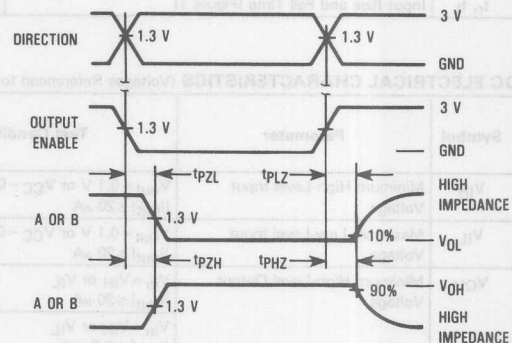
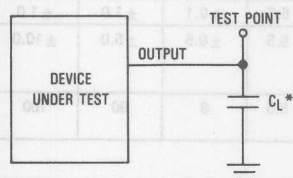
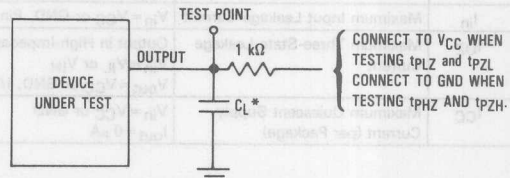


Figure 2



*Includes all probe and jig capacitance.

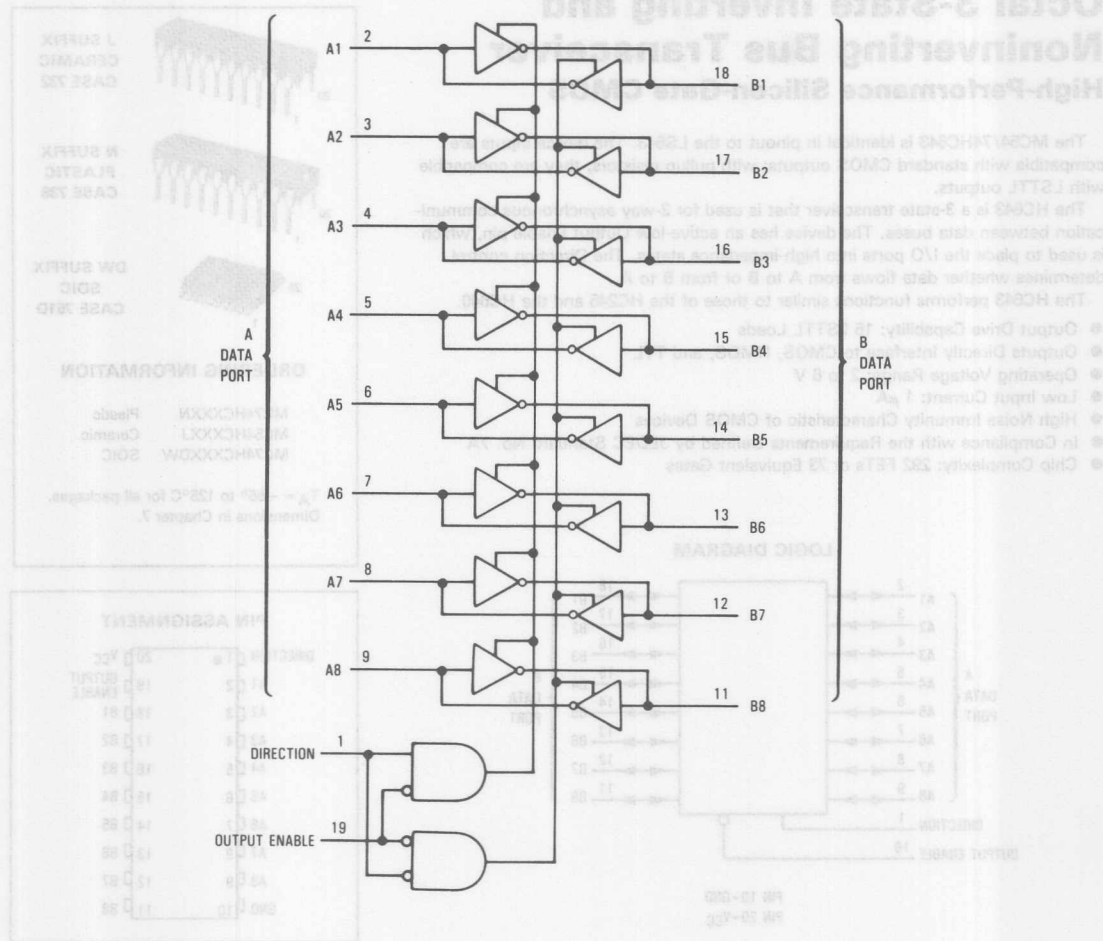
Figure 3. Test Circuit



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



Octal 3-State Inverting and Noninverting Bus Transceiver High-Performance Silicon-Gate CMOS

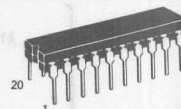
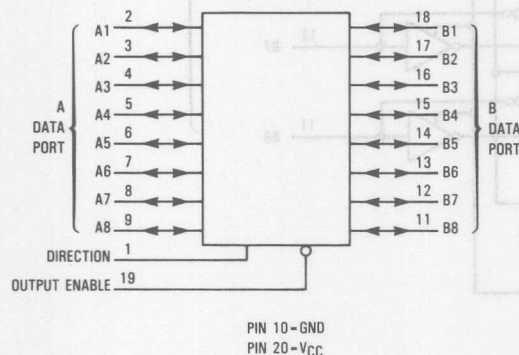
The MC54/74HC643 is identical in pinout to the LS643. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC643 is a 3-state transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

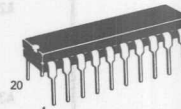
The HC643 performs functions similar to those of the HC245 and the HC640.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 292 FETs or 73 Equivalent Gates

LOGIC DIAGRAM



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

DIRECTION	1	20	V _{CC}
A1	2	19	OUTPUT ENABLE
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data transmitted from Bus B to Bus A (not inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses Isolated (High-Impedance State)

X = don't care

MC54/74HC643

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
$I_{I/O}$	DC I/O Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ 0 $V_{CC} = 4.5 \text{ V}$ 0 $V_{CC} = 6.0 \text{ V}$ 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND, Pin 1 or 19}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC643

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance, Pin 1 or 19	—	10	10	10	pF
C _{out}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

SWITCHING WAVEFORMS

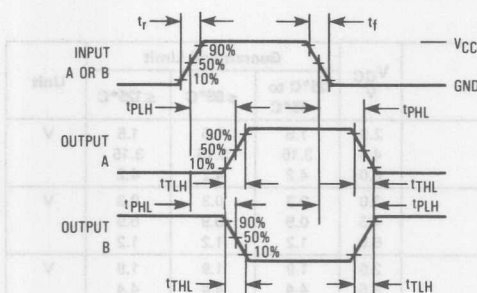


Figure 1

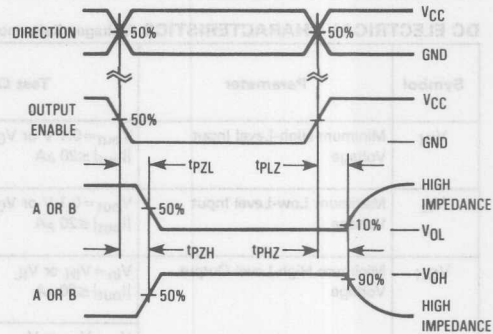
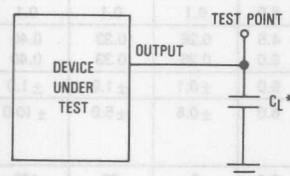
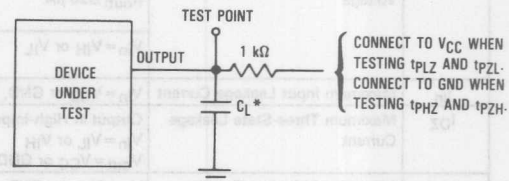


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit

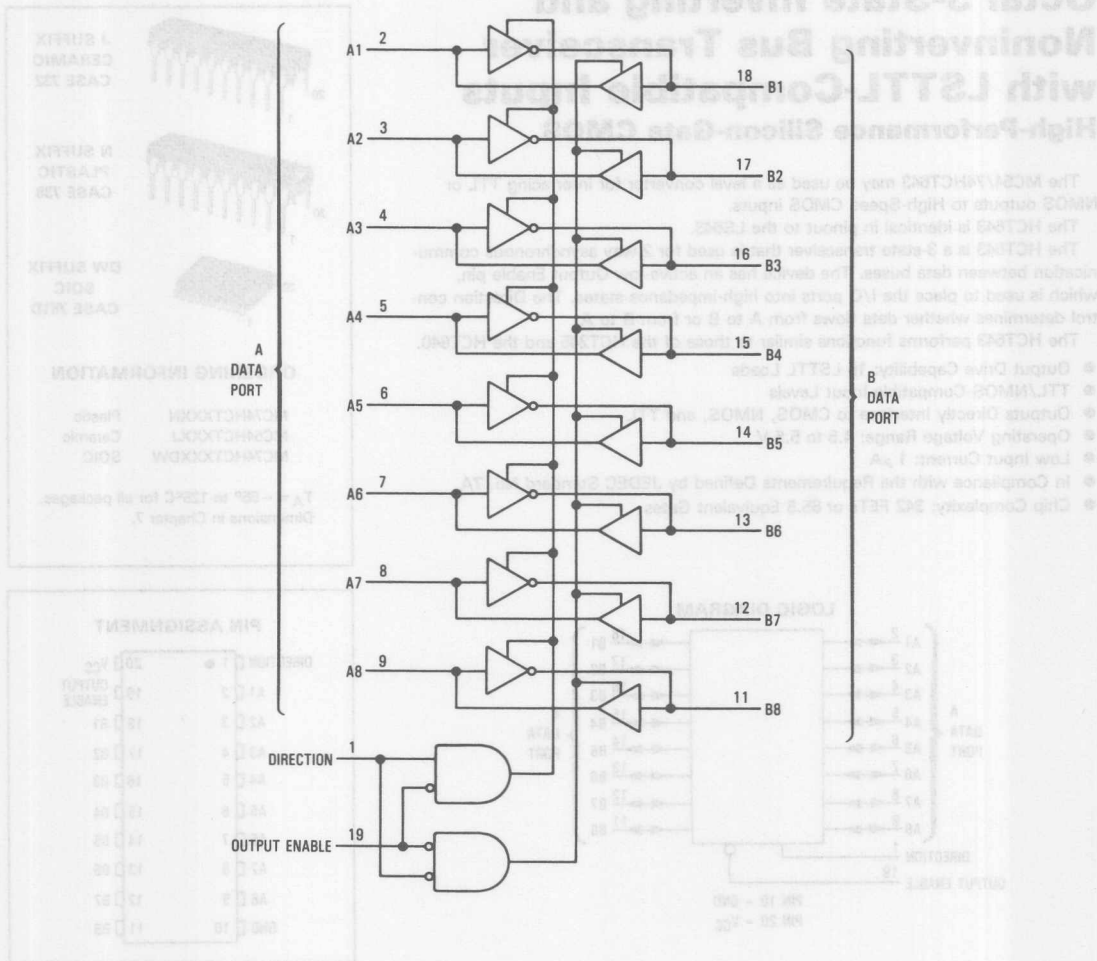


*Includes all probe and jig capacitance.

Figure 4. Test Circuit

MC54/74HC643

EXPANDED LOGIC DIAGRAM



FUNCTION TABLE

Operation	Control Inputs	
	Output Enable	Direction
Data transmitted from Bus B to Bus A (not inverted)	L	L
Data transmitted from Bus A to Bus B (inverted)	L	H
Bus is tri-stated (high-impedance state)	X	X

X = don't care

Octal 3-State Inverting and Noninverting Bus Transceiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

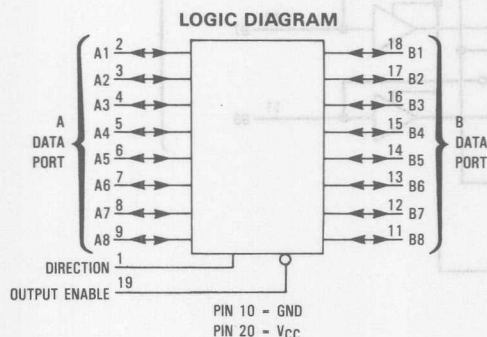
The MC54/74HCT643 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT643 is identical in pinout to the LS643.

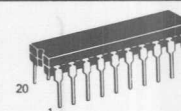
The HCT643 is a 3-state transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

The HCT643 performs functions similar to those of the HCT245 and the HCT640.

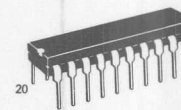
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 342 FETs or 85.5 Equivalent Gates



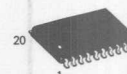
MC54/74HCT643



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



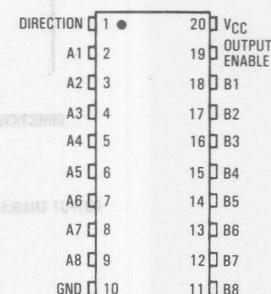
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCTXXN	Plastic
MC54HCTXXJ	Ceramic
MC74HCTXXDW	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data transmitted from Bus B to Bus A (not inverted)
L	H	Data transmitted from Bus A to Bus B (inverted)
H	X	Buses Isolated (high-impedance state)

X = don't care

MC54/74HCT643

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND), Pin 1 or 19	-1.5 to $V_{CC} + 1.5$	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
$I_{I/O}$	DC I/O Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND, Pin 1 or 19}$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND, I/O Pins}$	5.5	± 0.5	± 5.0	± 10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	8	80	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C 2.9	25°C to 125°C 2.4	mA
-----------------	-------------------------------------	--	-----	----------------	----------------------	----

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

MC54/74HCT643

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=6\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to B or B to A (Figures 1 and 3)	22	28	33	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	30	38	45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance, Pin 1 or 19	10	10	10	pF
C_{out}	Maximum Three-State I/O Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Transceiver Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC}=5.0\text{ V}$	pF
		45	

SWITCHING WAVEFORMS

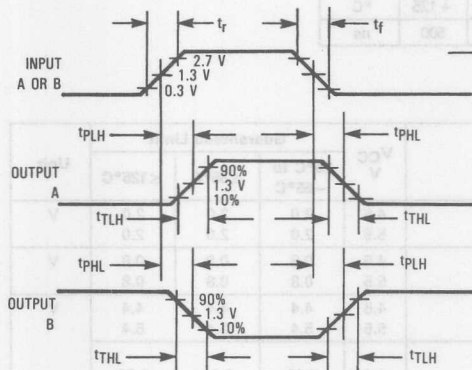


Figure 1

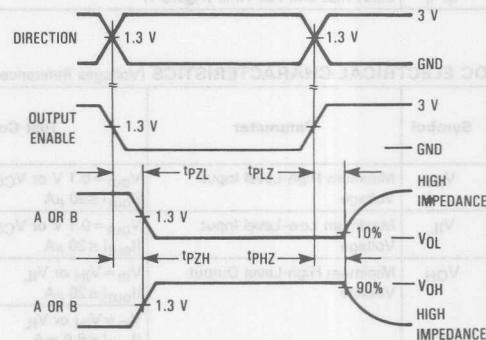
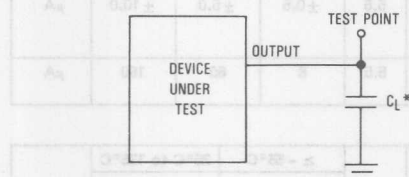
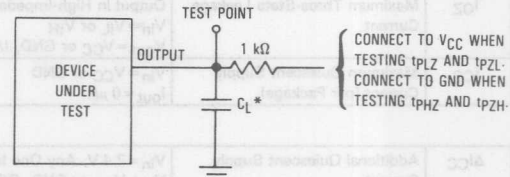


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit

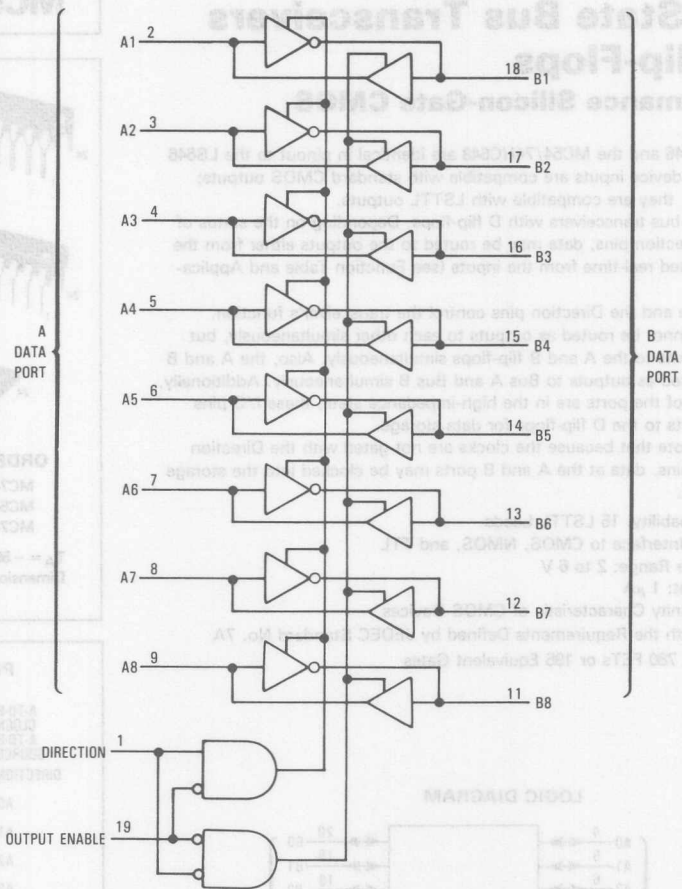


*Includes all probe and jig capacitance.

Figure 4. Test Circuit

MC54/74HCT643

EXPANDED LOGIC DIAGRAM



MC54/74HCT643

ORDERING INFORMATION

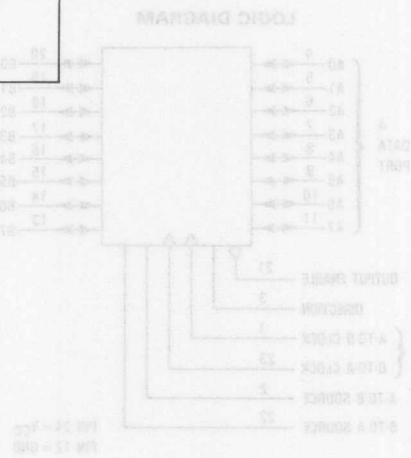
Case Style	Package	Material
MC54/74HCT643W	SOIC	Plastic
MC54/74HCT643C	SOIC	Ceramic
MC54/74HCT643P	SOIC	Plastic

PIN ASSIGNMENT

Pin	Signal	Pin	Signal
1	DIRECTION	18	B1
2	A1	19	B8
3	A2	20	B7
4	A3	21	B6
5	A4	22	B5
6	A5	23	B4
7	A6	24	B3
8	A7	25	B2
9	A8	26	B1
10	OUTPUT ENABLE	27	B8
11		28	B7
12		29	B6
13		30	B5
14		31	B4
15		32	B3
16		33	B2
17		34	B1

FUNCTIONS

- 3-STATE BUFFER
- 3-STATE DRIVER
- 3-STATE INVERTING BUFFER
- 3-STATE INVERTING DRIVER



Octal 3-State Bus Transceivers and D Flip-Flops High-Performance Silicon-Gate CMOS

The MC54/74HC646 and the MC54/74HC648 are identical in pinout to the LS646 and the LS648. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

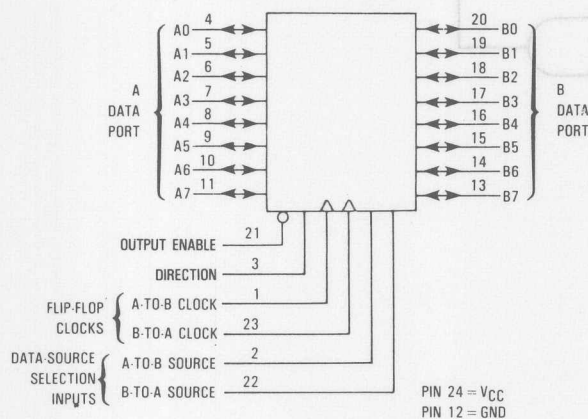
These devices are bus transceivers with D flip-flops. Depending on the status of the Data-Source Selection pins, data may be routed to the outputs either from the flip-flops or transmitted real-time from the inputs (see Function Table and Application Information).

The Output Enable and the Direction pins control the transceiver's function. Bus A and Bus B cannot be routed as outputs to each other simultaneously, but can be routed as inputs to the A and B flip-flops simultaneously. Also, the A and B flip-flops can be routed as outputs to Bus A and Bus B simultaneously. Additionally, when either or both of the ports are in the high-impedance state, these I/O pins may be used as inputs to the D flip-flops for data storage.

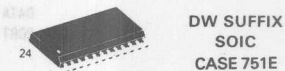
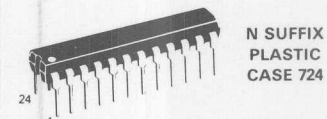
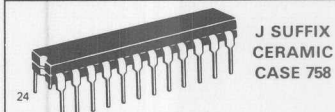
The user should note that because the clocks are not gated with the Direction and Output Enable pins, data at the A and B ports may be clocked into the storage flip-flops at any time.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 780 FETs or 195 Equivalent Gates

LOGIC DIAGRAM



MC54/74HC648



ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

A-TO-B CLOCK	1	24	VCC
A-TO-B SOURCE	2	23	B-TO-A CLOCK
DIRECTION	3	22	B-TO-A SOURCE
A0	4	21	OUTPUT ENABLE
A1	5	20	B0
A2	6	19	B1
A3	7	18	B2
A4	8	17	B3
A5	9	16	B4
A6	10	15	B5
A7	11	14	B6
GND	12	13	B7

HC646 - Noninverting Outputs
HC648 - Inverting Outputs

MC54/74HC646•MC54/74HC648

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{I/O}	DC I/O Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{I/O}	DC I/O Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND (Pins 1, 2, 3, 21, 22, and 23)	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND, I/O Pins	6.0	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC646•MC54/74HC648

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3, 4 and 9)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output B (or Input B to Output A) (Figures 1, 2 and 9)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A-to-B Clock to Output B (or B-to-A Clock to Output A) (Figures 3, 4 and 9)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A-to-B Source to Output B (or B-to-A Source to Output A) (Figures 5, 6 and 9)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Direction or Output Enable to Output A or B (Figures 7, 8 and 10)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Direction or Output Enable to Output A or B (Figures 7, 8 and 10)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 9)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		60	

5

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)













Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Input A to A-to-B Clock (or Input B to B-to-A Clock) (Figures 3 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, A-to-B Clock to Input A (or B-to-A Clock to Input B) (Figures 3 and 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, A-to-B Clock (or B-to-A Clock) (Figures 3 and 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

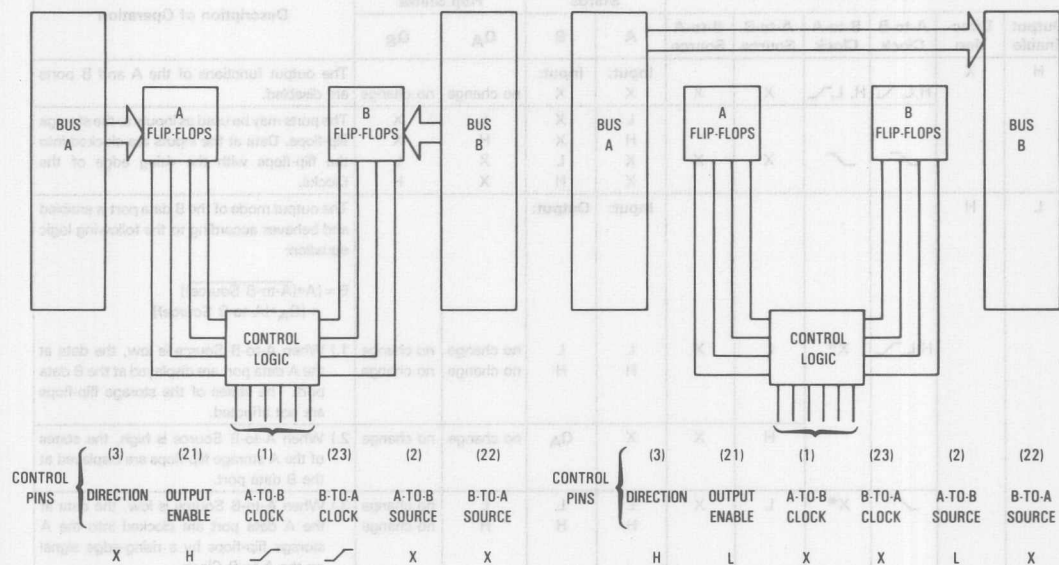
MC54/74HC646•MC54/74HC648

FUNCTION TABLE - HC646

(The Function Table for the HC648 is the same as this, but with the outputs inverted)

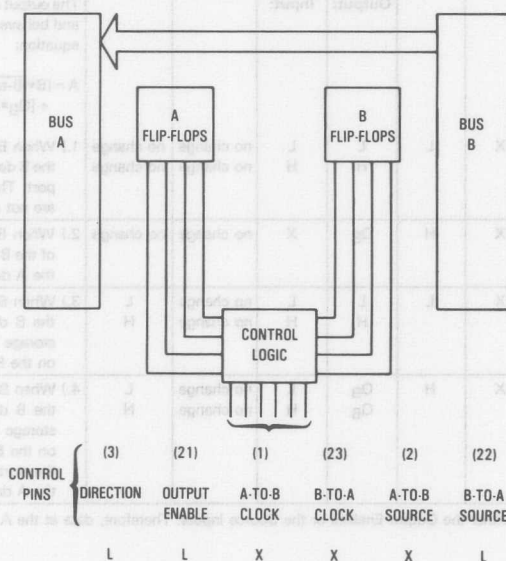
Control Inputs						Data Port Status		Storage Flip-Flop States		Description of Operation
Output Enable	Direction	A-to-B Clock	B-to-A Clock	A-to-B Source	B-to-A Source	A	B	Q _A	Q _B	
H	X	H, L, 	H, L, 	X	X	Input: X	Input: X	no change	no change	The output functions of the A and B ports are disabled.
				X	X	L	X	L	X	The ports may be used as inputs to the storage flip-flops. Data at the inputs are clocked into the flip-flops with the rising edge of the Clocks.
				X	X	H	X	H	X	
				X	X	X	H	X	H	
L	H	H, L, 	X*	L	X	Input: L	Output: L	no change	no change	<p>The output mode of the B data port is enabled and behaves according to the following logic equation:</p> $B = [A \cdot (\overline{A\text{-to-B Source}})] + [Q_A \cdot (A\text{-to-B Source})]$ <p>1.) When A-to-B Source is low, the data at the A data port are displayed at the B data port. The states of the storage flip-flops are not affected.</p>
				H	X	X	Q _A	no change	no change	
				L	X	L	L	L	no change	
				H	X	H	H	H	no change	
			X*	L	X	L	L	L	no change	<p>2.) When A-to-B Source is high, the states of the A storage flip-flops are displayed at the B data port.</p> <p>3.) When A-to-B Source is low, the data at the A data port are clocked into the A storage flip-flops by a rising-edge signal on the A-to-B Clock.</p>
				H	X	H	H	H	no change	
				L	X	L	Q _A	L	no change	
				H	X	H	Q _A	H	no change	
L	L	X*	H, L, 	X	L	Output: L	Input: L	no change	no change	<p>The output mode of the A data port is enabled and behaves according to the following logic equation:</p> $A = [B \cdot (\overline{B\text{-to-A Source}})] + [Q_B \cdot (B\text{-to-A Source})]$ <p>1.) When B-to-A Source is low, the data at the B data port are displayed at the A data port. The states of the storage flip-flops are not affected.</p>
				X	H	Q _B	X	no change	no change	
				X	L	L	L	L	no change	
				X	H	H	H	H	no change	
			X*	X	L	L	L	L	no change	<p>2.) When B-to-A Source is high, the states of the B storage flip-flops are displayed at the A data port.</p> <p>3.) When B-to-A Source is low, the data at the B data port are clocked into the B storage flip-flops by a rising-edge signal on the B-to-A Clock.</p>
				X	H	H	H	H	no change	
				X	L	Q _B	L	no change	L	
				X	H	Q _B	H	no change	H	

*The clocks are not internally gated with either the Output Enables or the Source inputs. Therefore, data at the A and B ports may be clocked into the storage flip-flops at any time.



Data Storage From A and/or B Bus

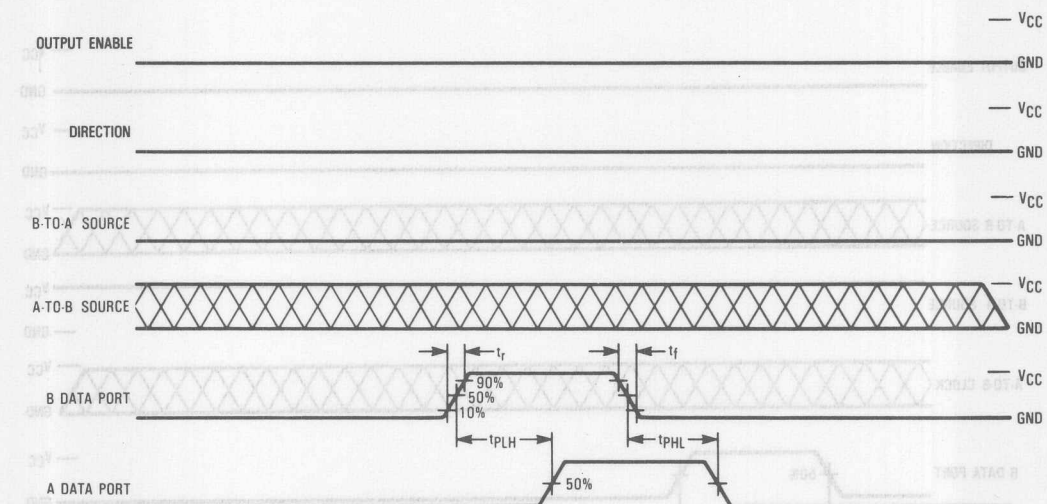
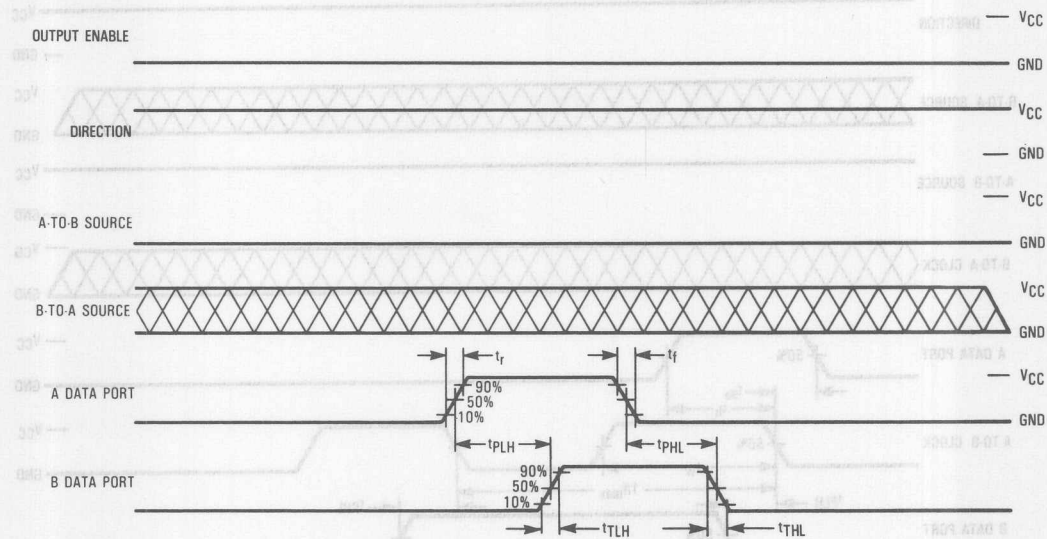
Real-Time Transfer From Bus A to Bus B



Real-Time Transfer From Bus B to Bus A

MC54/74HC646•MC54/74HC648

TIMING DIAGRAMS AND SWITCHING DIAGRAMS — HC646 (The Diagrams For The HC648 Are The Same As Below, But With The Outputs Inverted)



NOTE:  = Don't Care State

MC54/74HC646•MC54/74HC648

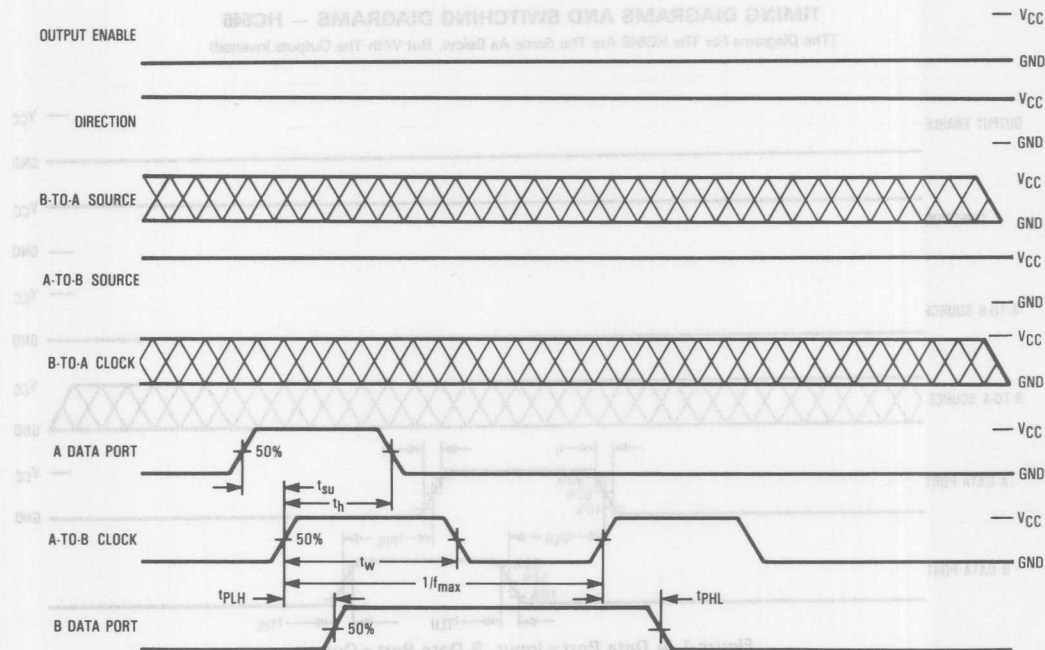


Figure 3. A Data Port = Input, B Data Port = Output

5

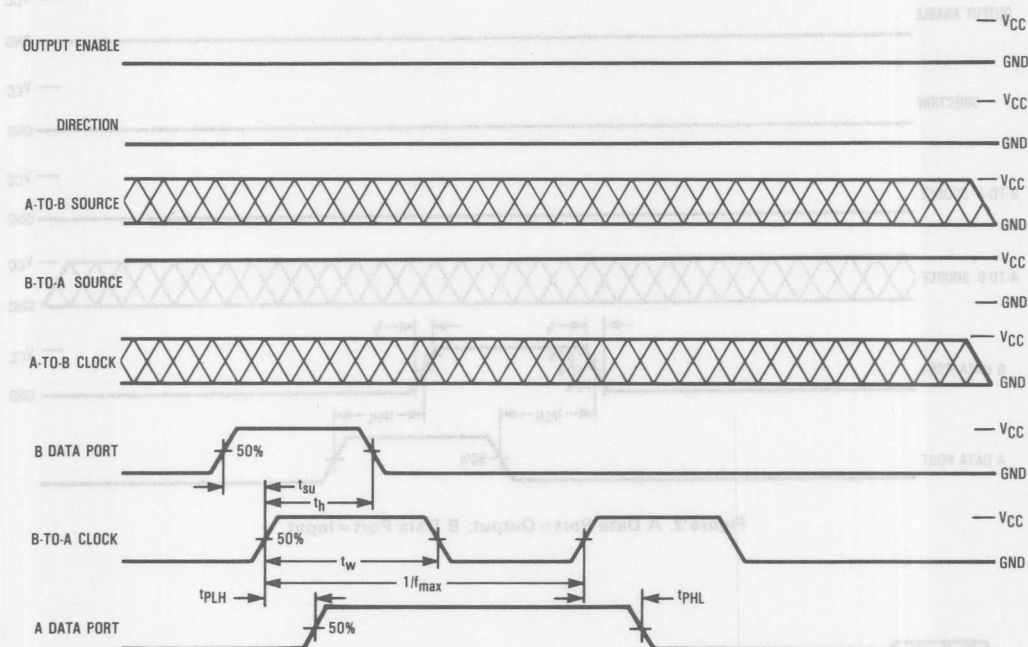
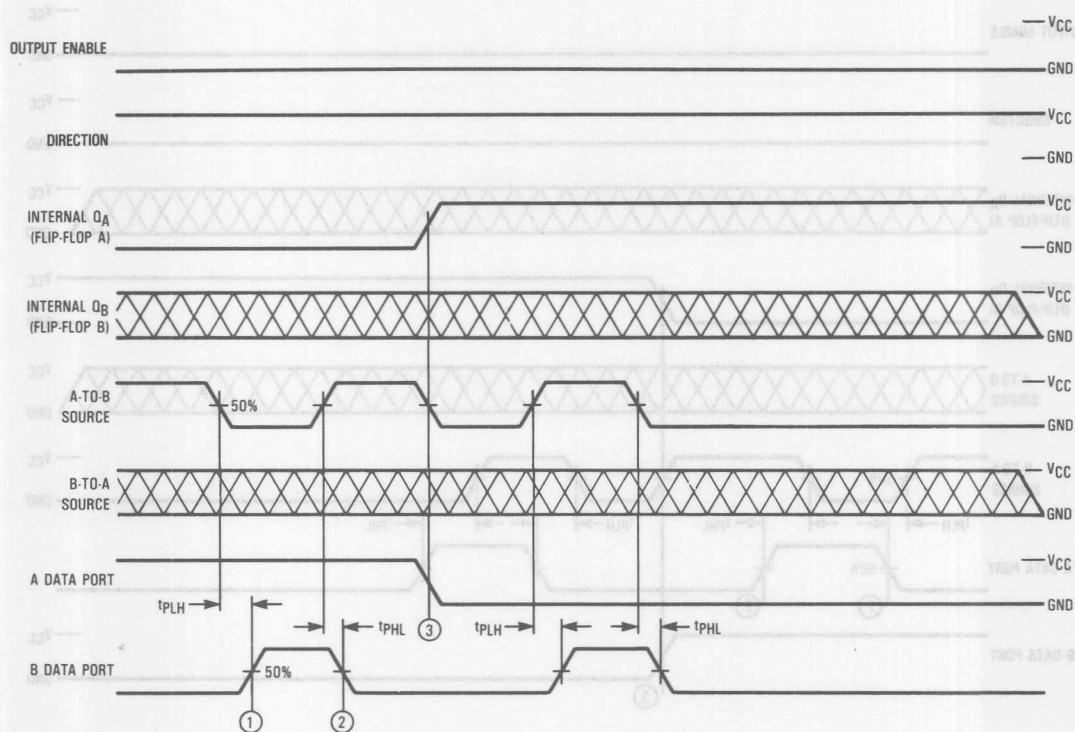


Figure 4. B Data Port = Input, A Data Port = Output

MC54/74HC646•MC54/74HC648



NOTES:

1. B Data Port (output) changes from the level of the storage flip-flop, Q_A , to the level of A Data Port (input).
2. B Data Port (output) changes from the level of A Data Port (input) to the level of the storage flip-flop, Q_A .
3. The A storage flip-flop, A-to-B Source, and A Data Port (input) have simultaneously changed states.

Figure 5. A Data Port = Input, B Data Port = Output

5

PIN DESCRIPTIONS

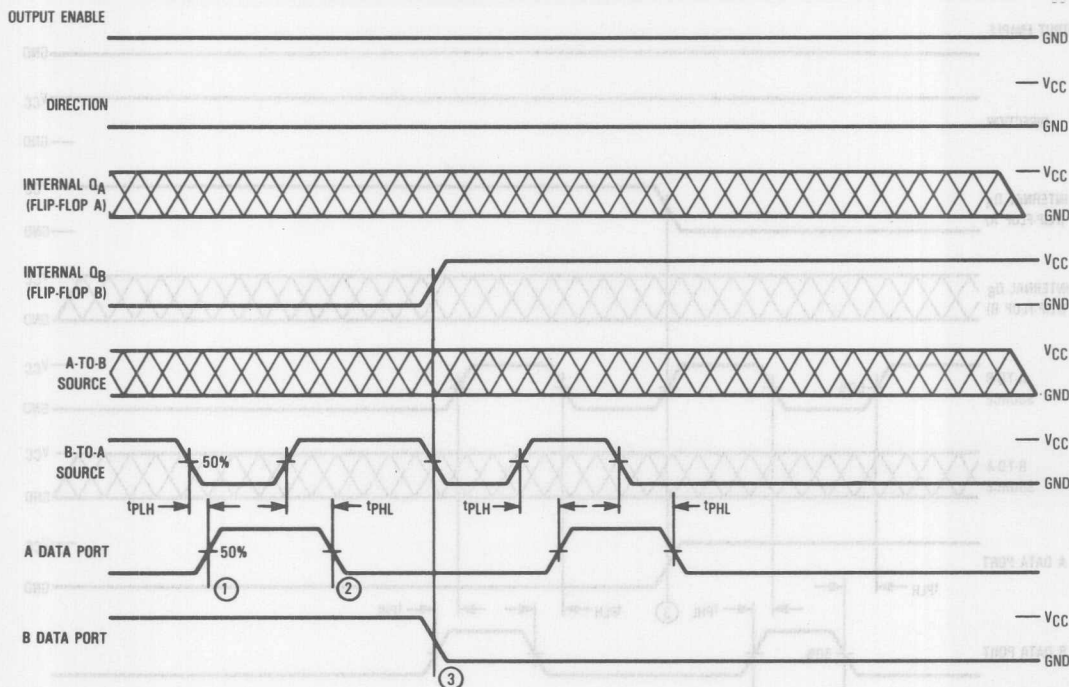
ports are inputs and the B data ports are outputs. When DIRECTION is low, the A data ports are outputs and the B data ports are inputs.

A-TO-B CLOCK, B-TO-A CLOCK (PINS 1, 23) — Clocks
for the internal D flip-flops. With a low-to-high transition on the appropriate Clock pin, data on the A (or B) inputs are clocked into the internal A (or B) flip-flops. These clocks are not internally gated with the Output Enable or the Direction pin. Therefore data at the A and B pins may be clocked into the storage flip-flops at any time.

A-TO-B SOURCE, B-TO-A SOURCE (PINS 2, 22) — Data-
source selection pins. Depending upon the state of these pins (see the Function Table), data at the outputs may come either from the inputs or from the D flip-flops.

INPUTS/OUTPUTS
A0-A7 (PINS 4-11) and B0-B7 (PINS 20-27) — A and B data ports. These pins may function either as inputs to or outputs from the transceivers.

CONTROL INPUTS
OUTPUT ENABLE (PIN 21) — Active-low output enable.
When this pin is low, the outputs are enabled and function normally. When this pin is high, the A and B data ports are in high-impedance state. See the Function Table.
DIRECTION (PIN 2) — Data direction control. When the Output Enable pin is low, this control pin determines the direction of data flow. When Direction is high, the A data



NOTES:

1. A Data Port (output) changes from the level of the storage flip-flop, Q_B , to the level of B Data Port (input).
2. A Data Port (output) changes from the level of B Data Port (input) to the level of storage flip-flop, Q_B .
3. The B storage flip-flop, B-to-A Source, and B Data Port (input) have simultaneously changed states for the purpose of this example. A Data Port (output) is now displaying the voltage level of B Data Port (input).

5

Figure 6. A Data Port = Output, B Data Port = Input

PIN DESCRIPTIONS

INPUTS/OUTPUTS

A0-A7 (PINS 4-11) and B0-B7 (PINS 20-27) — A and B data ports. These pins may function either as inputs to or outputs from the transceivers.

CONTROL INPUTS

OUTPUT ENABLE (PIN 21) — Active-low output enable. When this pin is low, the outputs are enabled and function normally. When this pin is high, the A and B data ports are in high-impedance states. See the Function Table.

DIRECTION (PIN 3) — Data direction control. When the Output Enable pin is low, this control pin determines the direction of data flow. When Direction is high, the A data

ports are inputs and the B data ports are outputs. When Direction is low, the A data ports are outputs and the B data ports are inputs.

A-TO-B CLOCK, B-TO-A CLOCK (PINS 1, 23) — Clocks for the internal D flip-flops. With a low-to-high transition on the appropriate Clock pin, data on the A (or B) inputs are clocked into the internal A (or B) flip-flops. These clocks are not internally gated with the Output Enable or the Direction pins, therefore data at the A and B pins may be clocked into the storage flip-flops at any time.

A-TO-B SOURCE, B-TO-A SOURCE (PINS 2, 22) — Data-source selection pins. Depending upon the states of these pins (see the Function Table), data at the outputs may come either from the inputs or from the D flip-flops.

MC54/74HC646•MC54/74HC648

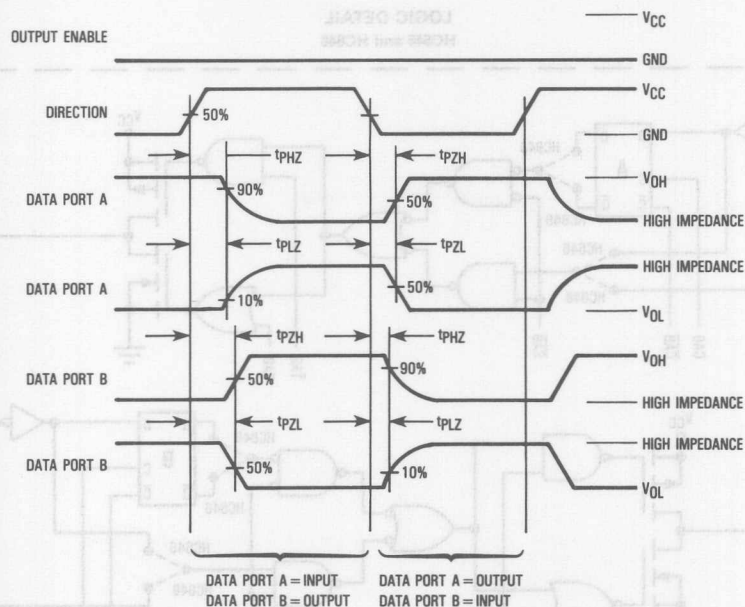


Figure 7

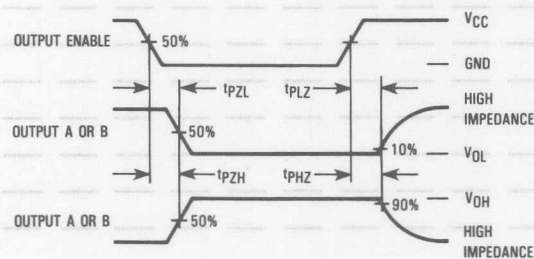
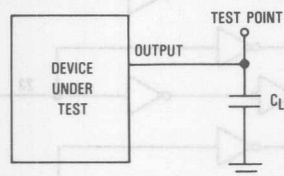
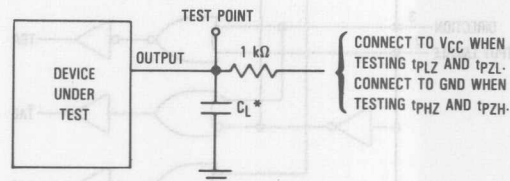


Figure 8



*Includes all probe and jig capacitance.

Figure 9. Test Circuit

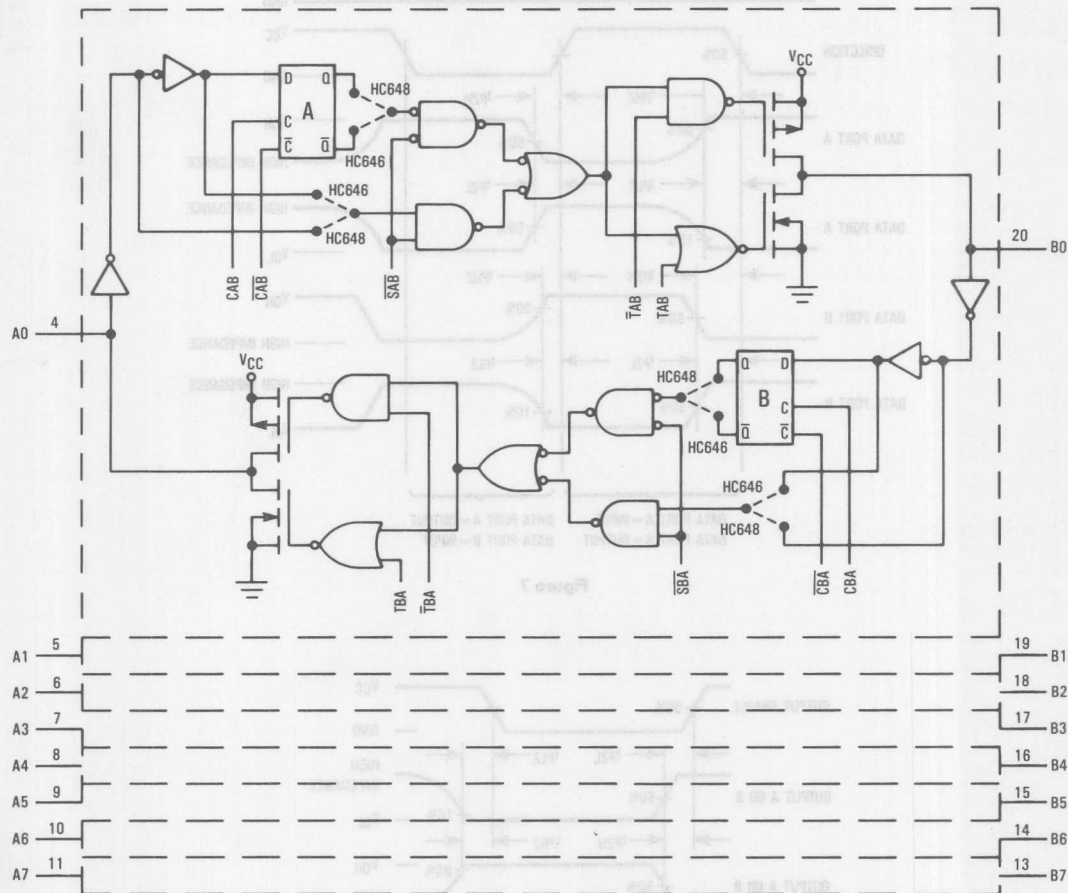


*Includes all probe and jig capacitance.

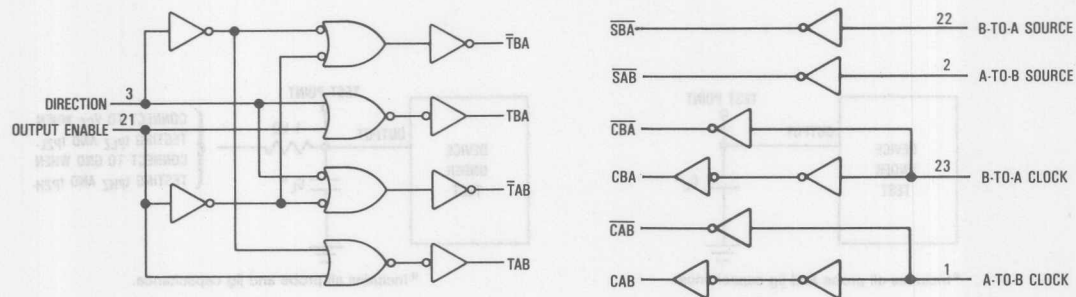
Figure 10. Test Circuit

MC54/74HC646•MC54/74HC648

LOGIC DETAIL HC646 and HC648



5



Octal 3-State Bus Transceivers and D Flip-Flops

High-Performance Silicon-Gate CMOS

The MC54/74HC651 and the MC54/74HC652 are identical in pinout to the LS651 and the LS652. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

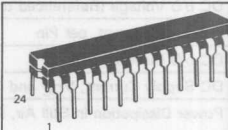
These devices are bus transceivers with D flip-flops. Depending on the status of the Data-Source Selection pins, data may be routed to the outputs either from the flip-flops or transmitted real-time from the inputs (see Function Table and Application Information).

The Output Enables, A-to-B (OEB) and B-to-A (OEA), control the transceiver's function. Bus A and Bus B cannot be routed as outputs to each other simultaneously, but can be routed as inputs to the A and B flip-flops simultaneously. Also, the A and B flip-flops can be routed as outputs to Bus A and Bus B simultaneously. Additionally, when either or both of the ports are in the high impedance state, these I/O pins may be used as inputs to the D flip-flops for data storage.

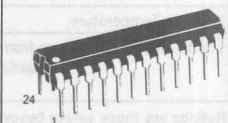
The user should note that because the clocks are not gated with the Output Enable pins, data at the A and B ports may be clocked into the storage flip-flops at any time.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 764 FETs or 191 Equivalent Gates

MC54/74HC651 MC54/74HC652



J SUFFIX
CERAMIC
CASE 758



N SUFFIX
PLASTIC
CASE 724



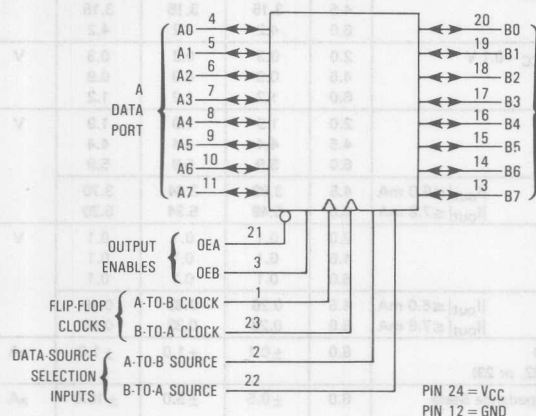
DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

A-to-B CLOCK	1	24	VCC
A-to-B SOURCE	2	23	B-to-A CLOCK
OEB	3	22	B-to-A SOURCE
A0	4	21	OEA
A1	5	20	B0
A2	6	19	B1
A3	7	18	B2
A4	8	17	B3
A5	9	16	B4
A6	10	15	B5
A7	11	14	B6
GND	12	13	B7

HC651 - Inverting Outputs
HC652 - Noninverting Outputs

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{I/O}	DC I/O Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{I/O}	DC I/O Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND (Pins 1, 2, 3, 21, 22, or 23)	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND, I/O Pins	6.0	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC651•MC54/74HC652

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3, 4 and 8)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output B (or Input B to Output A) (Figures 1, 2 and 8)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A-to-B Clock to Output B (or B-to-A Clock to Output A) (Figures 3, 4 and 8)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A-to-B Source to Output B (or B-to-A Source to Output A) (Figures 5, 6 and 8)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, OEA or OEB to Output A or B (Figures 7 and 9)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, OEA or OEB to Output A or B (Figures 7 and 9)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Channel) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V		pF
		60		

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input A to A-to-B Clock (or Input B to B-to-A Clock) (Figures 3 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, A-to-B Clock to Input A (or B-to-A Clock to Input B) (Figures 3 and 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t _w	Minimum Pulse Width, A-to-B Clock (or B-to-A Clock) (Figures 3 and 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC651•MC54/74HC652

FUNCTION TABLE - HC652

(The Function Table for the HC651 is the same as this, but with the outputs inverted)

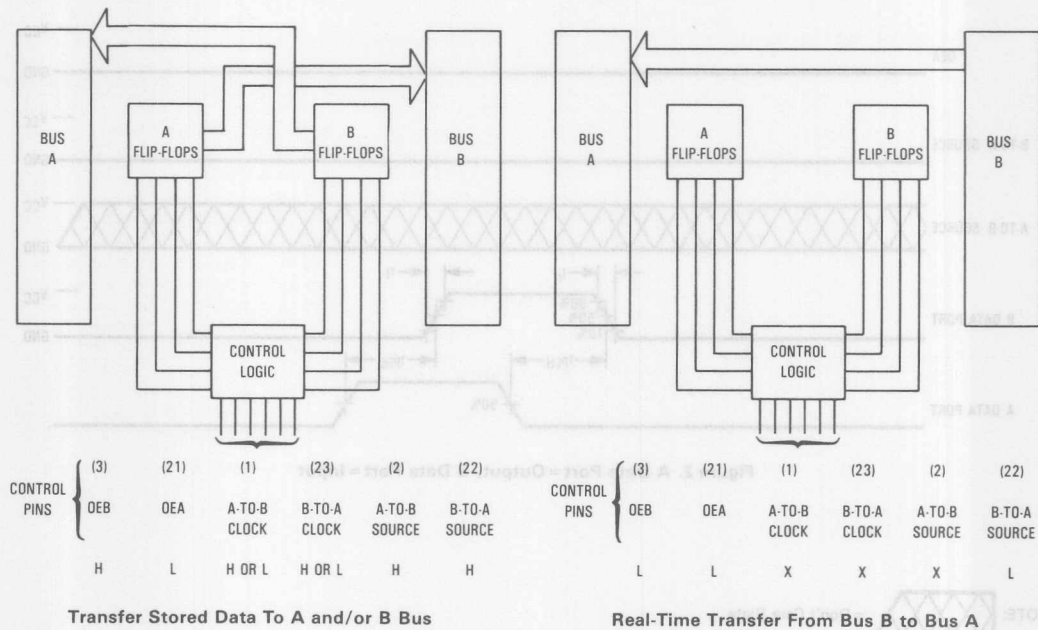
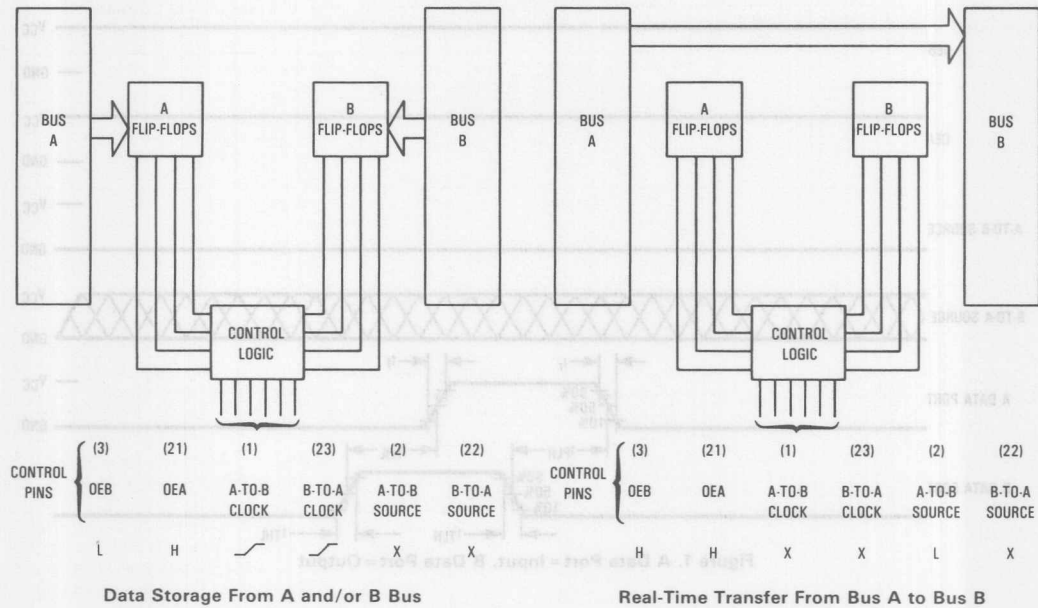
		Control Inputs				Data Port Status		Storage Flip-Flop States		Description of Operation
OEB	OEa	A-to-B Clock	B-to-A Clock	A-to-B Source	B-to-A Source	A	B	Q _A	Q _B	
L	H	H, L, 	H, L, 	X	X	Input: X	Input: X	no change	no change	The output functions of the A and B ports are disabled.
				X	X	L H X X	X X L H	L H X X	X X L H	The ports may be used as inputs to the storage flip-flops. Data at the inputs are clocked into the flip-flops with the rising edge of the Clocks.
H	H					Input:	Output:			The outputs of the B data port are enabled and behave according to the following logic equation: $B = [A \cdot (\overline{A\text{-to-B Source}})] + [Q_A \cdot (A\text{-to-B Source})]$
		X*	X*	L	X	L H	L H	no change no change	no change no change	1.) When A-to-B Source is low, the data at the A data port are displayed at the B data port. The states of the storage flip-flops are not affected.
				H	X	X	Q _A	no change	no change	2.) When A-to-B Source is high, the states of the A storage flip-flops are displayed at the B data port.
			X*	L	X	L H	L H	L H	no change no change	3.) When A-to-B Source is low, the data at the A data port are clocked into the A storage flip-flops by a rising-edge signal on the A-to-B Clock.
				H	X	L H	Q _A Q _A	L H	no change no change	4.) When A-to-B Source is high, the data at the A data port are clocked into the A storage flip-flops by a rising-edge signal on the A-to-B Clock. The states, Q _A , of the storage flip-flops propagate directly to the B data port.
L	L					Output:	Input:			The outputs of the A data port are enabled and behave according to the following logic equation: $A = [B \cdot (\overline{B\text{-to-A Source}})] + [Q_B \cdot (B\text{-to-A Source})]$
		X*	X*	X	L	L H	L H	no change no change	no change no change	1.) When B-to-A Source is low, the data at the B data port are displayed at the A data port. The states of the storage flip-flops are not affected.
				X	H	Q _B	X	no change	no change	2.) When B-to-A Source is high, the states of the B storage flip-flops are displayed at the A data port.
		X*		X	L	L H	L H	no change no change	L H	3.) When B-to-A Source is low, the data at the B data port are clocked into the B storage flip-flops by a rising-edge signal on the B-to-A Clock.
				X	H	Q _B Q _B	L H	no change no change	L H	4.) When B-to-A Source is high, the data at the B data port are clocked into the B storage flip-flops by a rising-edge signal on the B-to-A Clock. The states, Q _B , of the storage flip-flops propagate directly to the A data port.
H	L	X*	X*	H	H	Output: Q _B	Output: Q _A	no change	no change	When A-to-B Source and/or B-to-A Source are high, then states of the A storage flip-flops are displayed on the B port and/or the state of the B storage flip-flops are displayed on the A port.

*The clocks are not internally gated with either the Output Enables or the Source inputs. Therefore, data at the A and B ports may be clocked into the storage flip-flops at any time.

5

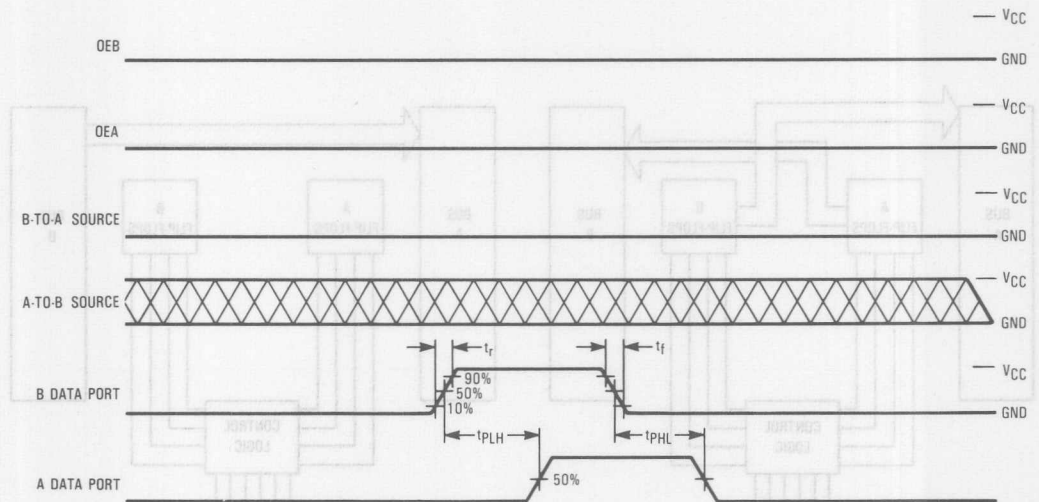
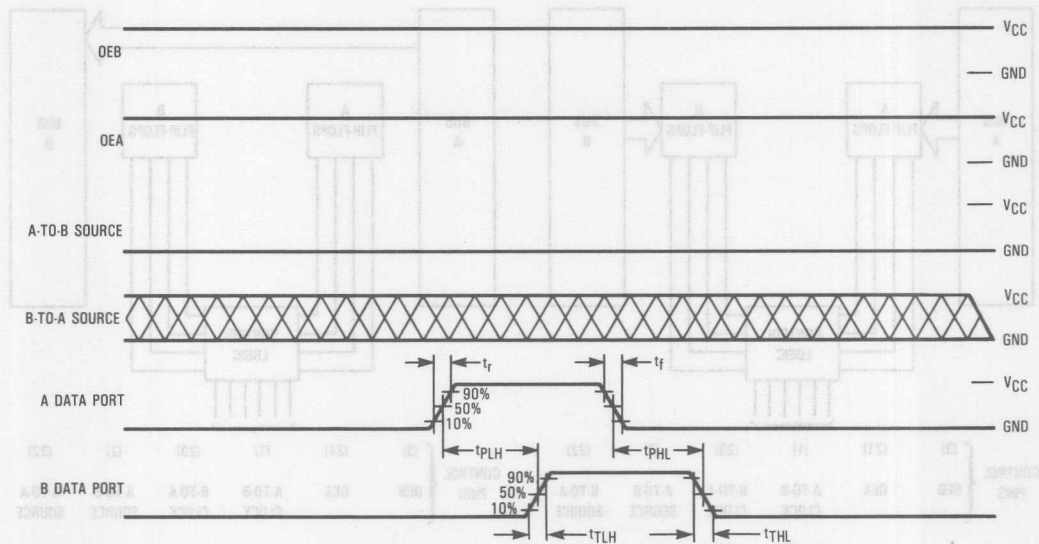
MC54/74HC651•MC54/74HC652

TYPICAL APPLICATIONS



5

(The Diagrams For The HC651 Are The Same As Below, But With The Outputs Inverted)



NOTE:  = Don't Care State

MC54/74HC651•MC54/74HC652

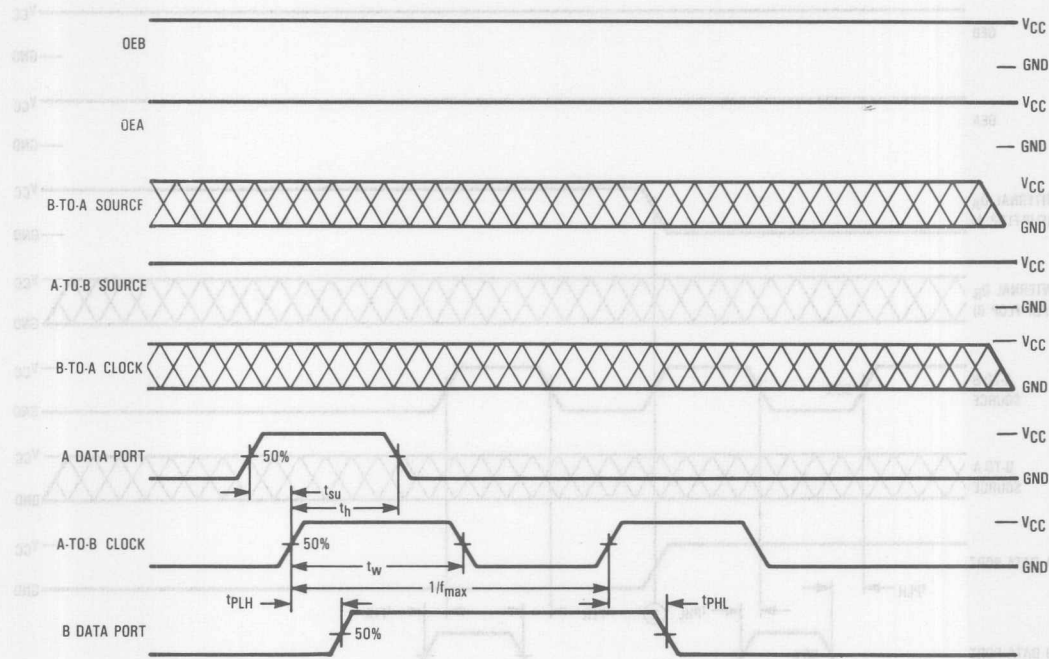


Figure 3. A Data Port = Input, B Data Port = Output

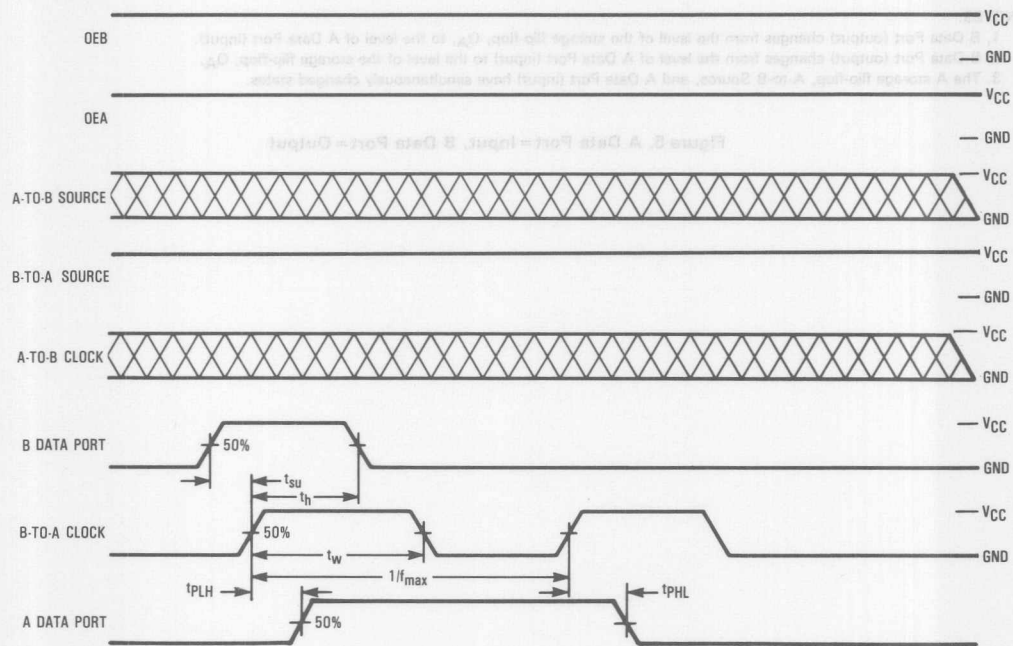
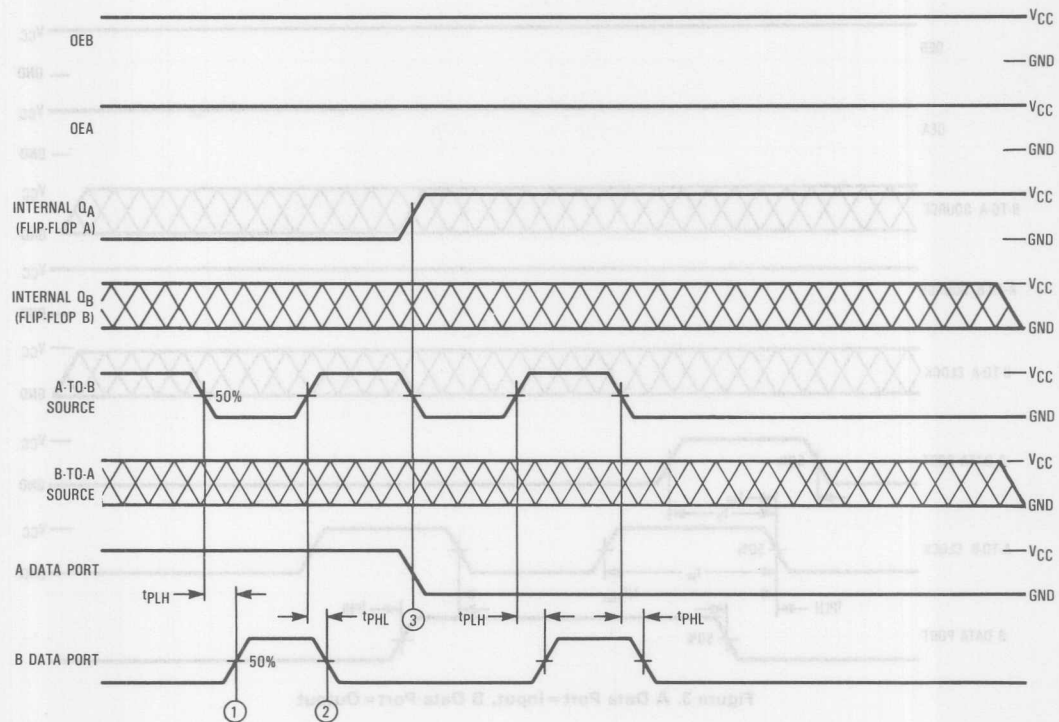


Figure 4. B Data Port = Input, A Data Port = Output

MC54/74HC651•MC54/74HC652



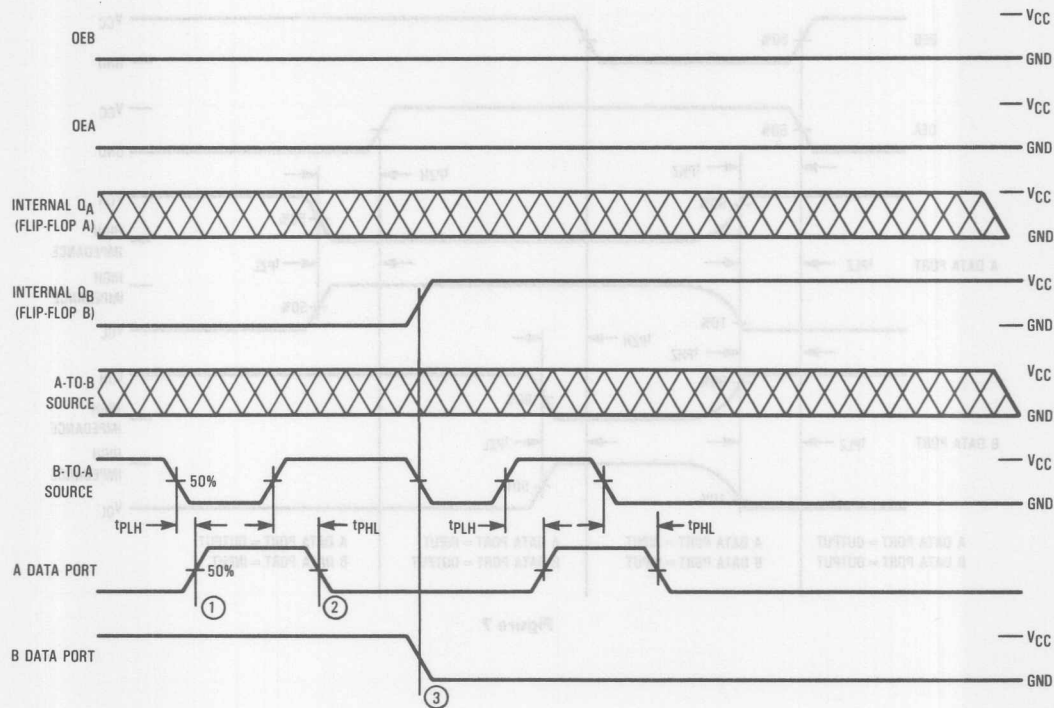
NOTES:

1. B Data Port (output) changes from the level of the storage flip-flop, Q_A , to the level of A Data Port (input).
2. B Data Port (output) changes from the level of A Data Port (input) to the level of the storage flip-flop, Q_A .
3. The A storage flip-flop, A-to-B Source, and A Data Port (input) have simultaneously changed states.

Figure 5. A Data Port = Input, B Data Port = Output

5

MC54/74HC651•MC54/74HC652



NOTES:

1. A Data Port (output) changes from the level of the storage flip-flop, Q_B , to the level of B Data Port (input).
2. A Data Port (output) changes from the level of B Data Port (input) to the level of storage flip-flop, Q_B .
3. The B storage flip-flop, B-to-A Source, and B Data Port (input) have simultaneously changed states for the purpose of this example. A Data Port (output) is now displaying the voltage level of B Data Port (input).

Figure 6. A Data Port = Output, B Data Port = Input

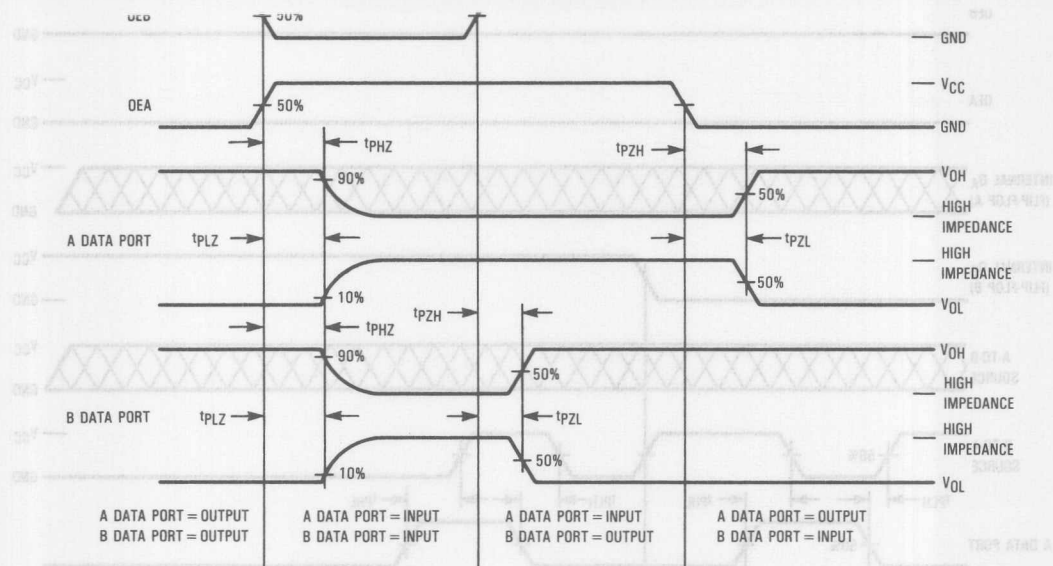
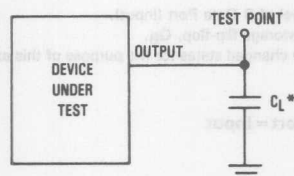
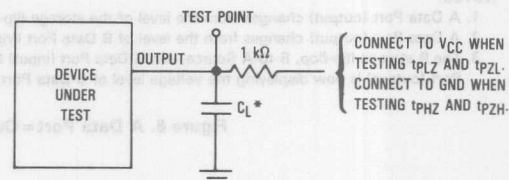


Figure 7



*Includes all probe and jig capacitance.

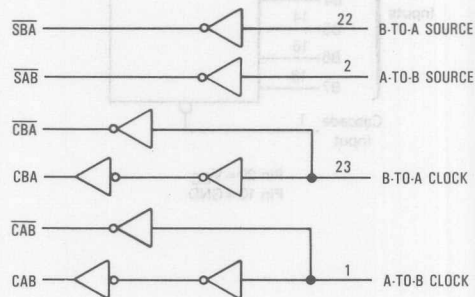
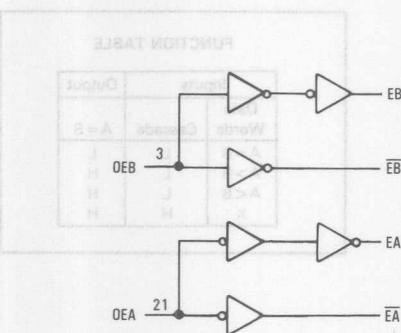
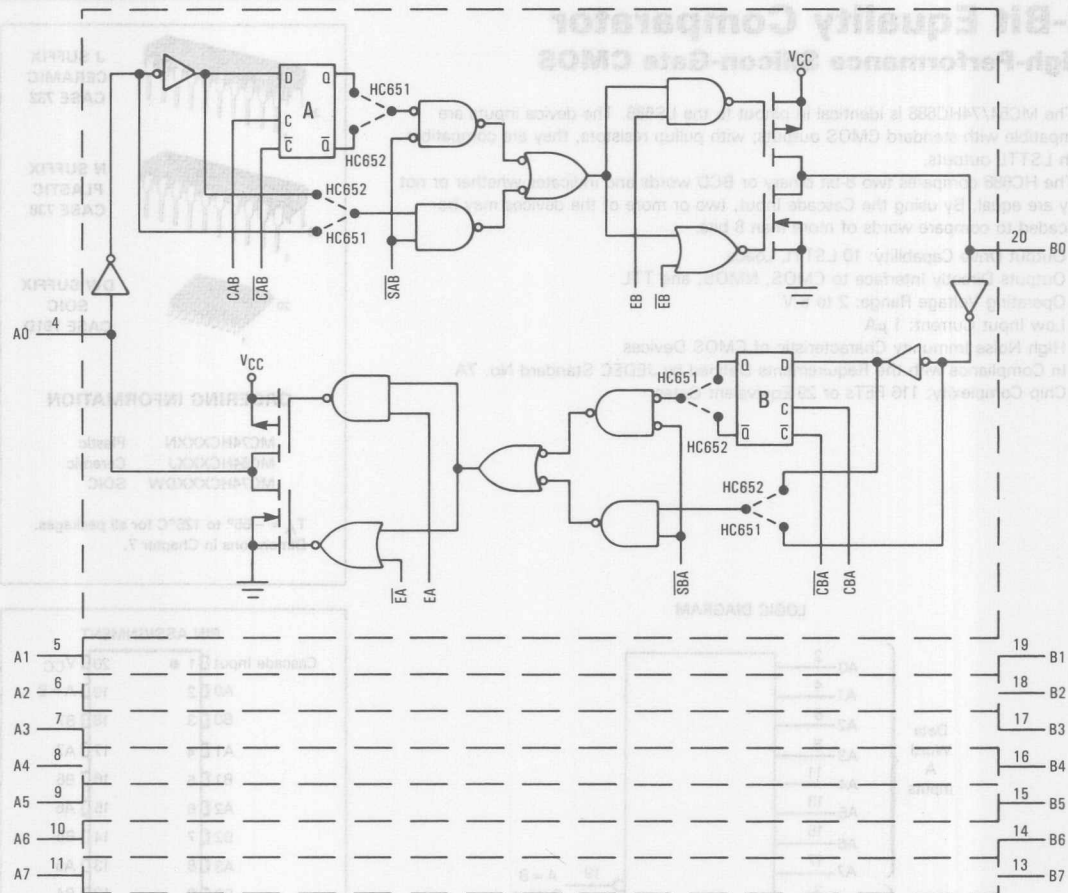
Figure 8. Test Circuit



*Includes all probe and jig capacitance.

Figure 9. Test Circuit

LOGIC DETAIL
HC651 and HC652



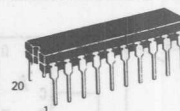
MC54/74HC688

8-Bit Equality Comparator High-Performance Silicon-Gate CMOS

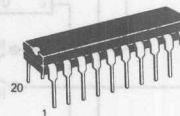
The MC54/74HC688 is identical in pinout to the LS688. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC688 compares two 8-bit binary or BCD words and indicates whether or not they are equal. By using the Cascade Input, two or more of the devices may be cascaded to compare words of more than 8 bits.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 116 FETs or 29 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



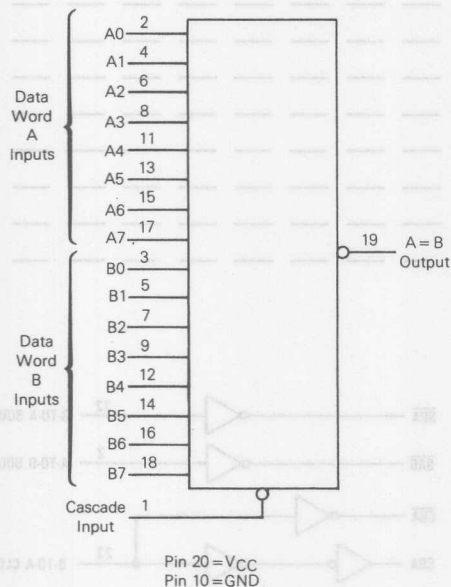
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

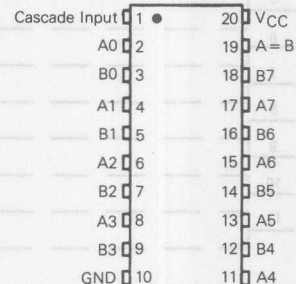
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
Data Words	Cascade	A = B
A = B	L	L
A > B	L	H
A < B	L	H
X	H	H

MC54/74HC688

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2)	$V_{CC} = 2.0 \text{ V}$ 0 $V_{CC} = 4.5 \text{ V}$ 0 $V_{CC} = 6.0 \text{ V}$ 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC688

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A or B to Output A = B (Figures 1 and 3)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Cascade Input to Output A = B (Figures 2 and 3)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		30	

SWITCHING WAVEFORMS

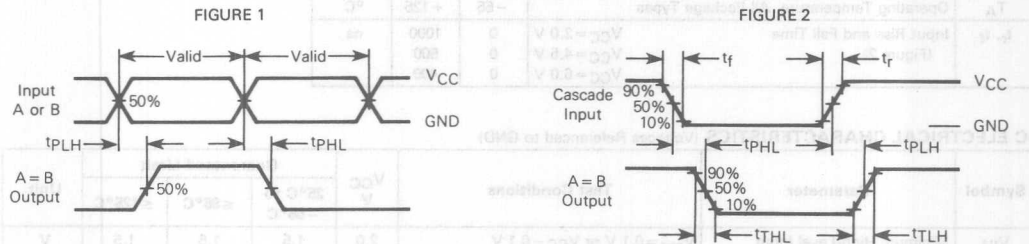
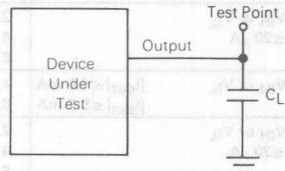


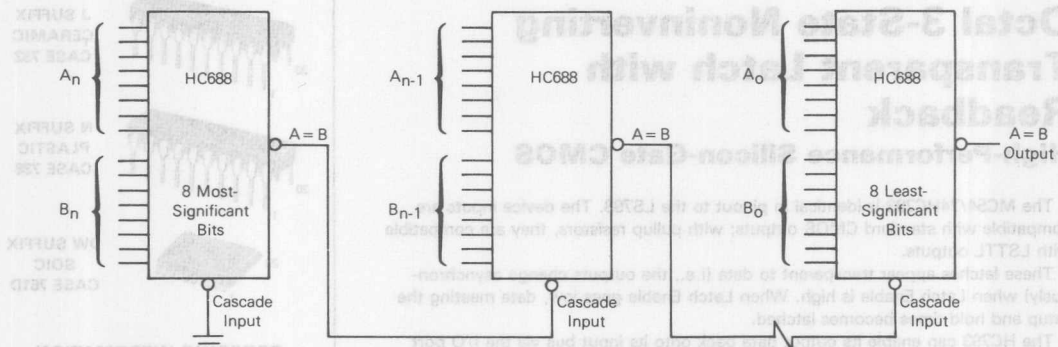
FIGURE 3 — TEST CIRCUIT



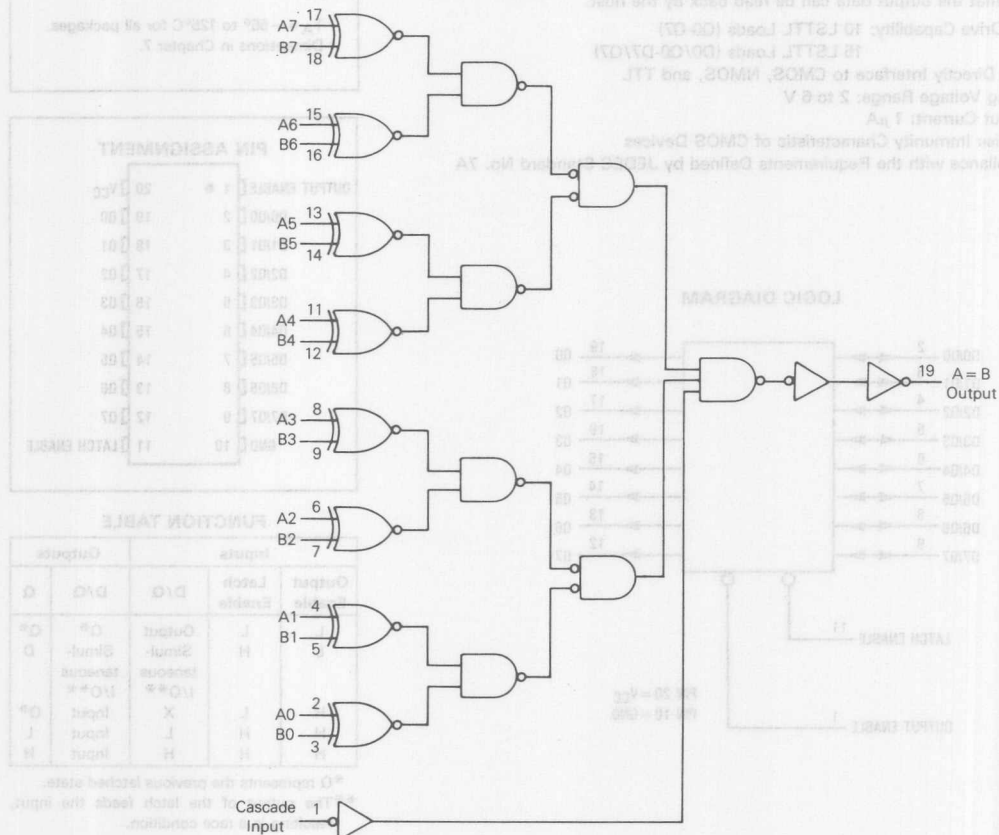
* Includes all probe and jig capacitance.

TYPICAL APPLICATION

Two or more HC688 8-bit Equality Comparators may be cascaded to compare binary or BCD numbers having more than 8 bits. One method of accomplishing this is shown here.



EXPANDED LOGIC DIAGRAM



Product Preview

Octal 3-State Noninverting Transparent Latch with Readback

High-Performance Silicon-Gate CMOS

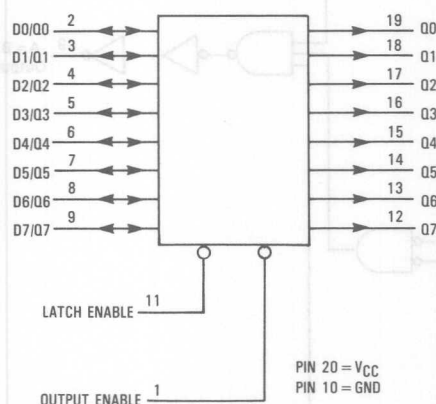
The MC54/74HC793 is identical in pinout to the LS793. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

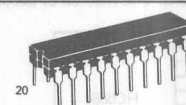
The HC793 can enable its output data back onto its input bus via the I/O port configuration. The Output Enable input determines how the pins D0/Q0-D7/Q7 are configured. When Output Enable is high, D0/Q0-D7/Q7 are inputs to the latches, configuring D0/Q0-D7/Q7 as an input bus. When Output Enable is low, the outputs of the latches are enabled on D0/Q0-D7/Q7, configuring D0/Q0-D7/Q7 as an output bus so that the output data can be read back by the host.

- Output Drive Capability: 10 LSTTL Loads (Q0-Q7)
15 LSTTL Loads (D0/Q0-D7/Q7)
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A

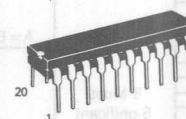
LOGIC DIAGRAM



MC54/74HC793



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

OUTPUT ENABLE	1	20	V_{CC}
D0/Q0	2	19	Q0
D1/Q1	3	18	Q1
D2/Q2	4	17	Q2
D3/Q3	5	16	Q3
D4/Q4	6	15	Q4
D5/Q5	7	14	Q5
D6/Q6	8	13	Q6
D7/Q7	9	12	Q7
GND	10	11	LATCH ENABLE

FUNCTION TABLE

Output Enable	Inputs		Outputs	
	Latch Enable	D/Q	D/Q	Q
L	L	Output	Q*	Q*
L	H	Simultaneous I/O**	Simultaneous I/O**	D
H	L	X	Input	Q*
H	H	L	Input	L
H	H	H	Input	H

*Q represents the previous latched state.
**The output of the latch feeds the input, resulting in a race condition.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74HC793

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin (Pins 1, 11)	± 20	mA
I_{out}	DC Output Current, per Pin (Pins 12-19)	± 25	mA
$I_{I/O}$	DC Output Current, per Pin (Pins 2-9)	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0$ V 0 $V_{CC} = 4.5$ V 0 $V_{CC} = 6.0$ V 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} Pins 2-9 $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
		$V_{in} = V_{IH}$ or V_{IL} Pins 12-19 $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} Pins 2-9 $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
		$V_{in} = V_{IH}$ or V_{IL} Pins 12-19 $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μ A
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	6.0	8	80	160	μ A

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

MC54/74HC793

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input Data to Q (Figures 1 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to D0/Q0-D7/Q7 (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to D0/Q0-D7/Q7 (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, D0/Q0-D7/Q7	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q0-Q7 (Figures 1 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance (Pins 1, 11)	—	10	10	10	pF
C _{out}	Maximum I/O Capacitance (I/O in High-Impedance State) (Output Enable = V _{IH})	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		TBD	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Input Data to Latch Enable (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Enable to Input Data (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

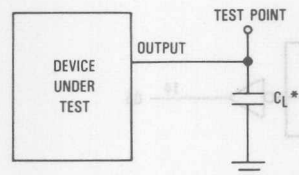
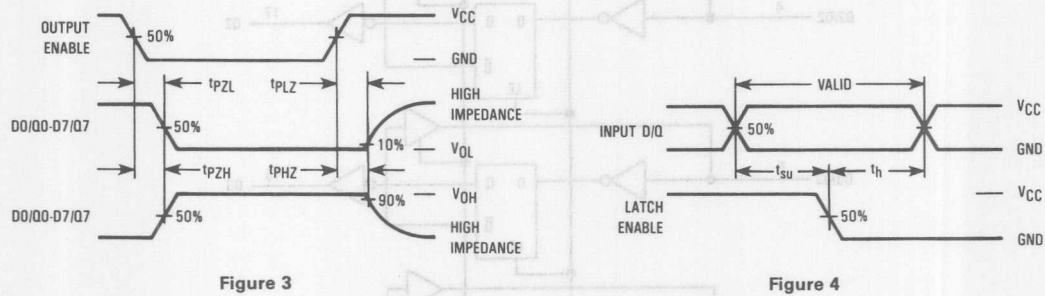
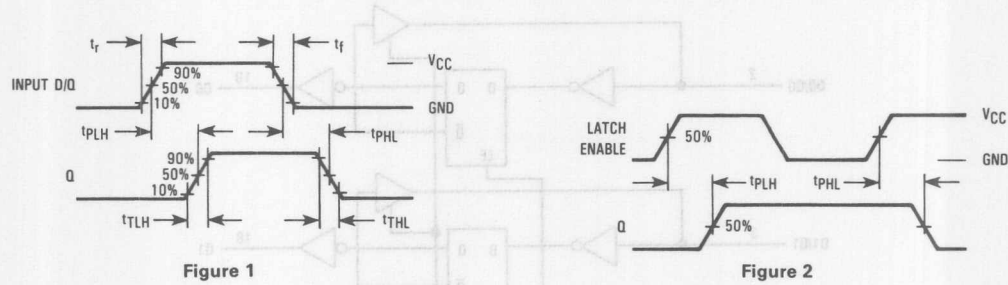
NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

I _{CC}	Maximum Current (see Package)	V _{IH} = V _{CC} or GND	100	50	50	mA
		V _{IH} = V _{CC} or GND	100	50	50	
I _{OL}	Maximum Output Sink Current	V _O = V _{CC} or GND	100	50	50	mA
		V _O = V _{CC} or GND	100	50	50	
I _{OH}	Maximum Output Sourcing Current	V _O = V _{CC} or GND	100	50	50	mA
		V _O = V _{CC} or GND	100	50	50	
I _{IL}	Maximum Input Leakage Current	V _I = V _{CC} or GND	100	50	50	nA
		V _I = V _{CC} or GND	100	50	50	
I _{OS}	Maximum Three-Phase Leakage Current	V _I = V _{CC} or GND	100	50	50	nA
		V _I = V _{CC} or GND	100	50	50	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

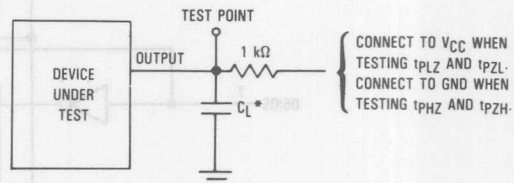
MC54/74HC793

SWITCHING WAVEFORMS



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

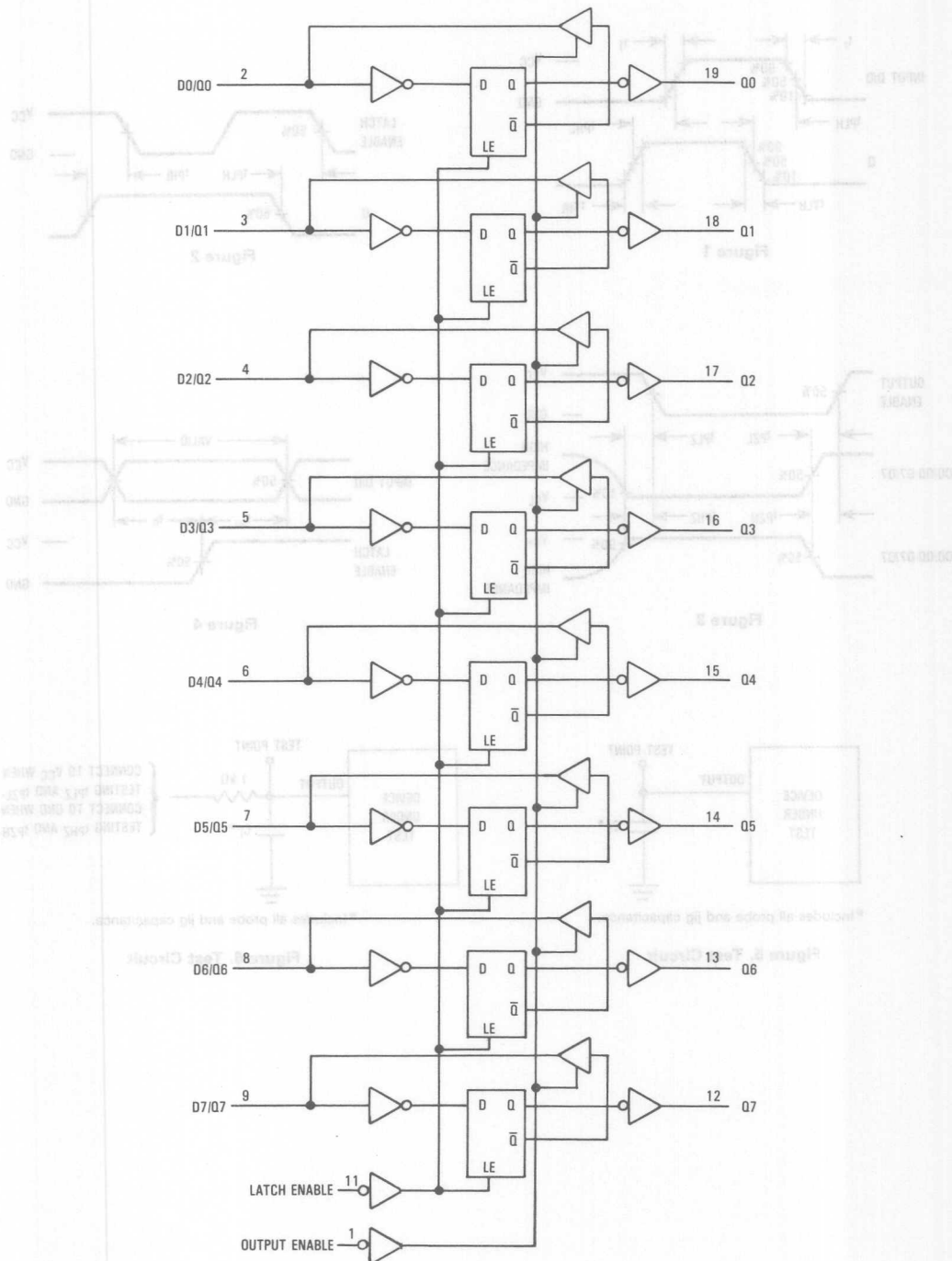


*Includes all probe and jig capacitance.

Figure 6. Test Circuit

MC54/74HC793

EXPANDED LOGIC DIAGRAM



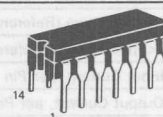
5

MC54/74HC4002

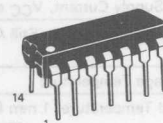
Dual 4-Input NOR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC4002 is identical in pinout to the MC14002B and MC14002UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 28 FETs or 7 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



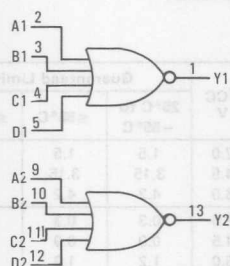
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND
PINS 6, 8 = NO CONNECTION

PIN ASSIGNMENT

Y1	1	14	V_{CC}
A1	2	13	Y2
B1	3	12	D2
C1	4	11	C2
D1	5	10	B2
NC	6	9	A2
GND	7	8	NC

NC = NO CONNECTION

FUNCTION TABLE

Inputs				Output
A	B	C	D	Y
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 2)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V 26	pF
----------	--	--	----

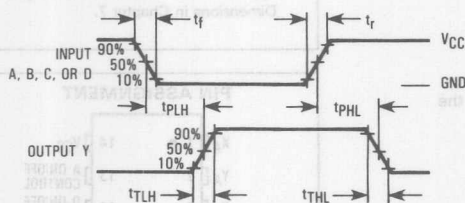
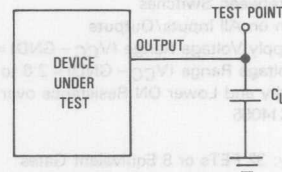
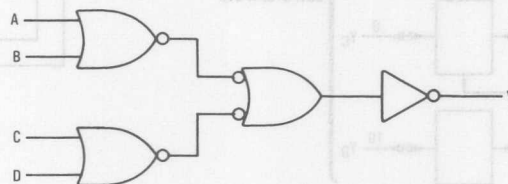


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(1/2 of the Device)

MC54/74HC4016

Advance Information Quad Analog Switch/ Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

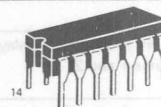
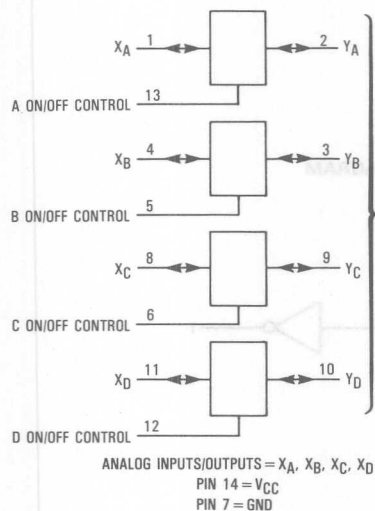
The MC54/74HC4016 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The HC4016 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

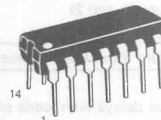
This device is identical in both function and pinout to the HC4066. The ON/OFF Control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316. For analog switches with lower R_{ON} characteristics, use the HC4066.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 12.0 Volts
- Analog Input Voltage Range ($V_{CC} - GND$) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 32 FETs or 8 Equivalent Gates

LOGIC DIAGRAM



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC4016

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	-0.5 to +14.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{in}	Digital Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}^*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)			ns
	$V_{CC} = 2.0$ V	0	1000	
	$V_{CC} = 4.5$ V	0	500	
	$V_{CC} = 9.0$ V	0	400	
	$V_{CC} = 12.0$ V	0	250	

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn, i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Voltage ON/OFF Control Inputs	$R_{on} = \text{per spec}$	2.0 4.5 9.0 12.0	1.5 3.15 6.3 8.4	1.5 3.15 6.3 8.4	1.5 3.15 6.3 8.4	V
V_{IL}	Maximum Low-Level Voltage ON/OFF Control Inputs	$R_{on} = \text{per spec}$	2.0 4.5 9.0 12.0	0.3 0.9 1.8 2.4	0.3 0.9 1.8 2.4	0.3 0.9 1.8 2.4	V
I_{in}	Maximum Input Leakage Current, ON/OFF Control Inputs	$V_{in} = V_{CC} \text{ or GND}$	12.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $V_{IO} = 0$ V	6.0 12.0	2 8	20 80	40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4016

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
R _{on}	Maximum "ON" Resistance	V _{in} = V _{IH} V _{IS} = V _{CC} to GND I _S ≤ 2.0 mA (Figures 1, 2)	2.0†	—	—	—	Ω
			4.5	320	400	480	
			9.0	170	215	255	
			12.0	170	215	255	
		V _{in} = V _{IH} V _{IS} = V _{CC} or GND (Endpoints) I _S ≤ 2.0 mA (Figures 1, 2)	2.0	—	—	—	
			4.5	180	225	270	
			9.0	135	170	205	
			12.0	135	170	205	
ΔR _{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V _{in} = V _{IH} V _{IS} = 1/2 (V _{CC} - GND) I _S ≤ 2.0 mA	2.0	—	—	—	Ω
			4.5	30	35	40	
			9.0	20	25	30	
			12.0	20	25	30	
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel	V _{in} = V _{IL} V _{IO} = V _{CC} or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I _{on}	Maximum On-Channel Leakage Current, Any One Channel	V _{in} = V _{IH} V _{IS} = V _{CC} or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V_{CC} - GND) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, ON/OFF Control Inputs: t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0	50	65	75	ns
		4.5	10	13	15	
		9.0	10	13	15	
		12.0	10	13	15	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	150	190	225	ns
		4.5	30	38	45	
		9.0	30	38	45	
		12.0	30	38	45	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	125	160	185	ns
		4.5	25	32	37	
		9.0	25	32	37	
		12.0	25	32	37	
C	Maximum Capacitance	ON/OFF Control Input	—	10	10	pF
		Control Input = GND	—	—	—	
		Analog I/O Feedthrough	—	35 1.0	35 1.0	35 1.0

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		15	

MC54/74HC4016

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND unless noted)

Symbol	Parameter	Test Conditions	V _{CC} V	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f _{in} = 1 MHz Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{OS} Increase f _{in} Frequency Until dB Meter Reads -3 dB R _L = 50 Ω, C _L = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off-Channel Feedthrough Isolation (Figure 6)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	-50 -50 -50 -40 -40 -40	dB
—	Feedthrough Noise, Control to Switch (Figure 7)	V _{in} ≤ 1 MHz Square Wave (t _r = t _f = 6 ns) Adjust R _L at Setup so that I _S = 0 A R _L = 600 Ω, C _L = 50 pF R _L = 10 kΩ, C _L = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	60 130 200 30 65 100	mV _{pp}
—	Crosstalk Between Any Two Switches (Figure 12)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	-70 -70 -70 -80 -80 -80	dB
THD	Total Harmonic Distortion (Figure 14)	f _{in} = 1 kHz, R _L = 10 kΩ, C _L = 50 pF THD = THD _{Measured} - THD _{Source} V _{IS} = 4.0 V _{pp} sine wave V _{IS} = 8.0 V _{pp} sine wave V _{IS} = 11.0 V _{pp} sine wave	4.5 9.0 12.0	0.10 0.06 0.04	%

*Guaranteed limits not tested. Determined by design and verified by qualification.

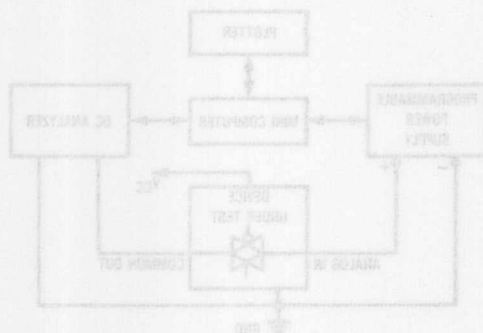


Figure 5. On Resistance Test Set-Up

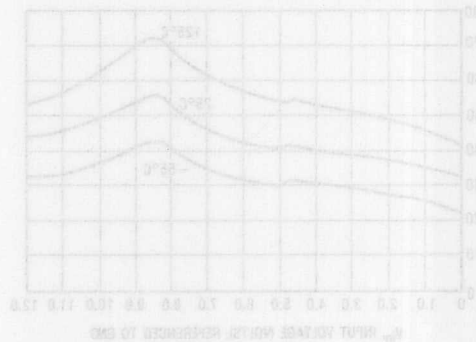


Figure 1a. Typical On Resistance, V_{CC} = 12.0 V

MC54/74HC4016

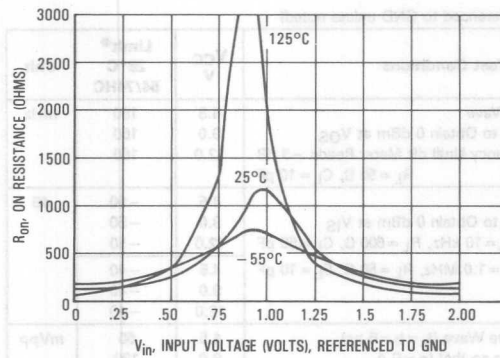


Figure 1a. Typical On Resistance, $V_{CC} = 2.0$ V

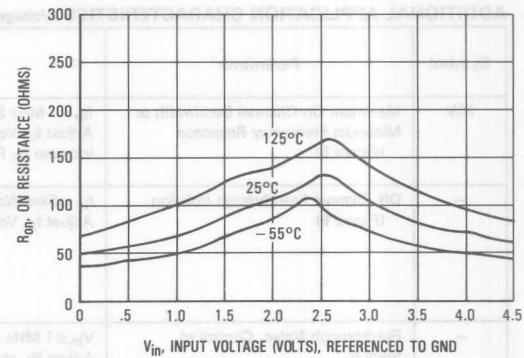


Figure 1b. Typical On Resistance, $V_{CC} = 4.5$ V

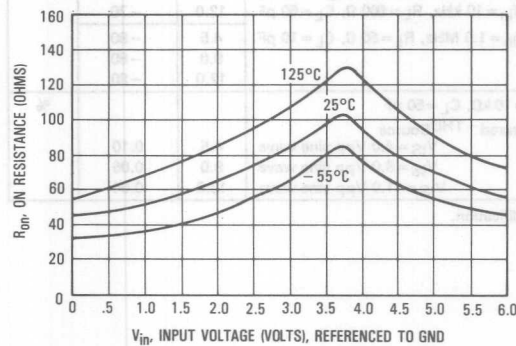


Figure 1c. Typical On Resistance, $V_{CC} = 6.0$ V

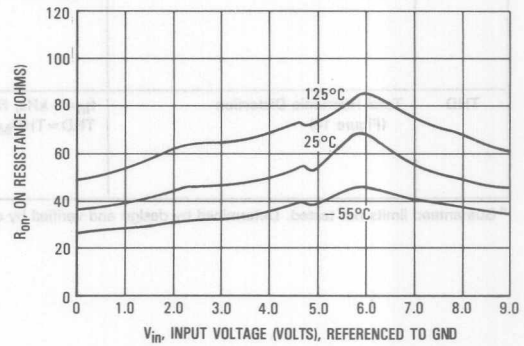


Figure 1d. Typical On Resistance, $V_{CC} = 9.0$ V

5

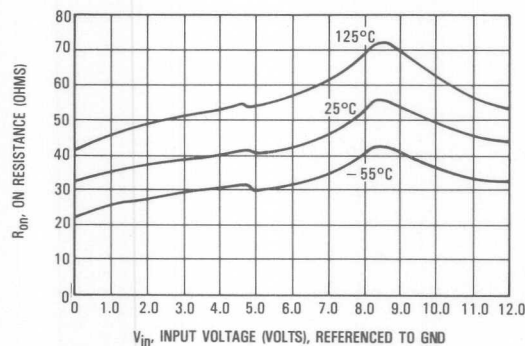


Figure 1e. Typical On Resistance, $V_{CC} = 12.0$ V

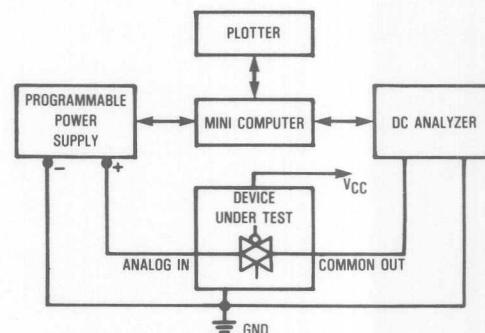


Figure 2. On Resistance Test Set-Up

MC54/74HC4016

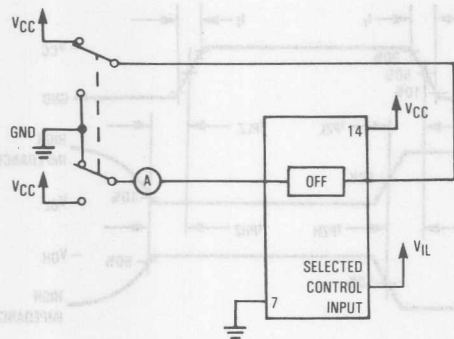


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

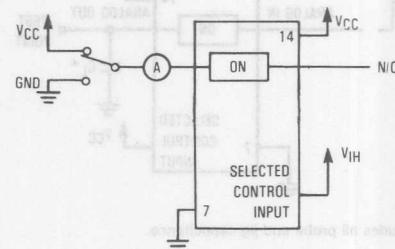
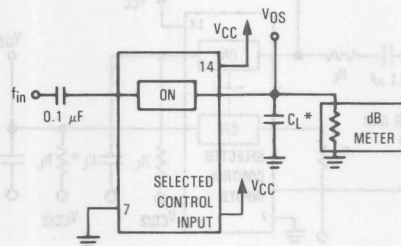
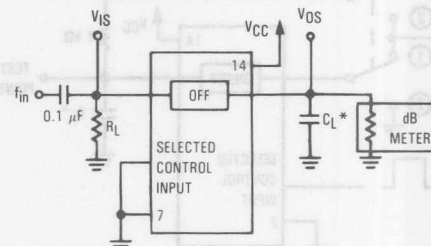


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



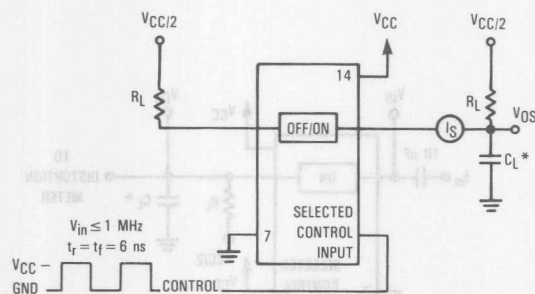
*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth Test Set-Up



*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

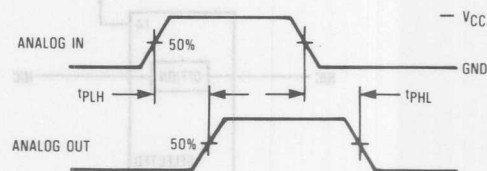
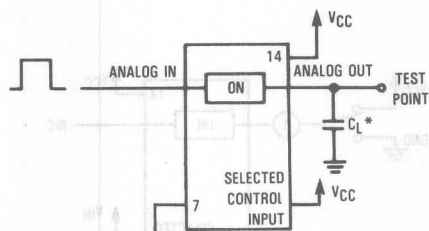


Figure 8. Propagation Delays, Analog In to Analog Out

MC54/74HC4016



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

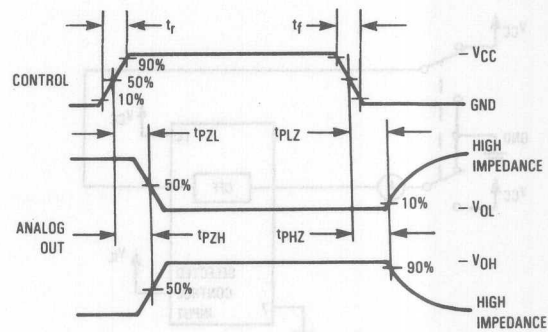
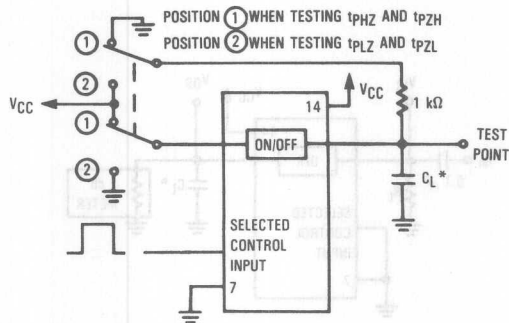
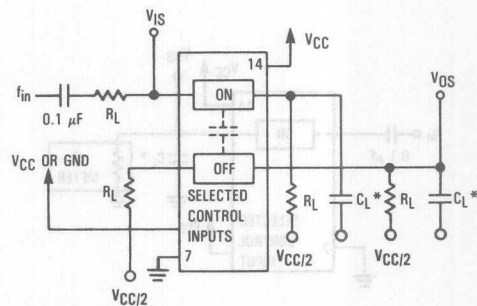


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

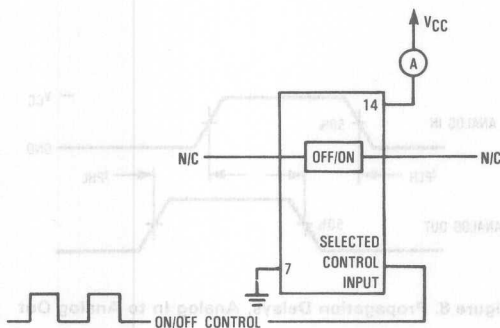
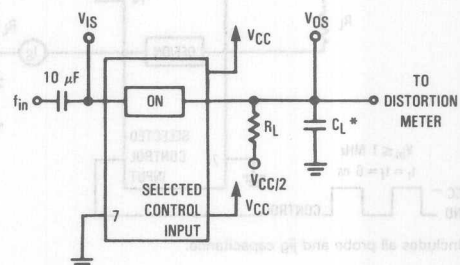


Figure 13. Power Dissipation Capacitance Test Set-Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

MC54/74HC4016

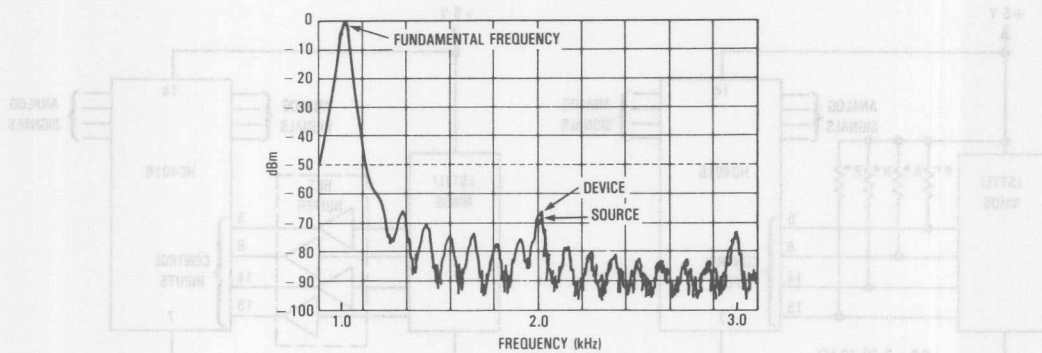


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below GND. In the example below,

the difference between V_{CC} and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the D_x diodes with MO-sorbs (Motorola high current surge protectors). MO-sorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear-out mechanism.

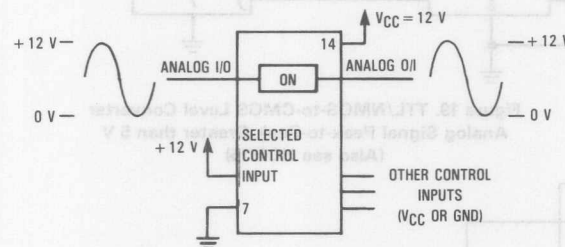


Figure 16. 12 V Application

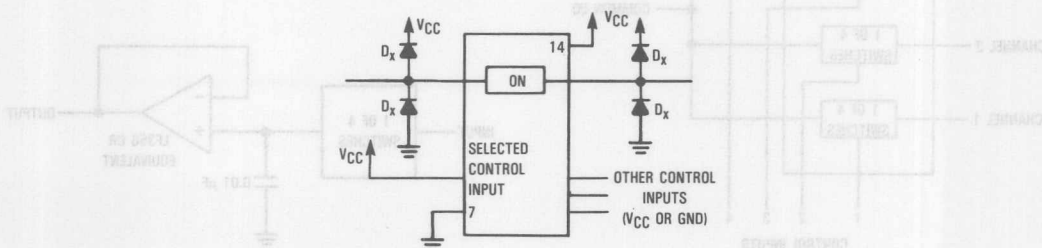


Figure 17. Transient Suppressor Application

MC54/74HC4016

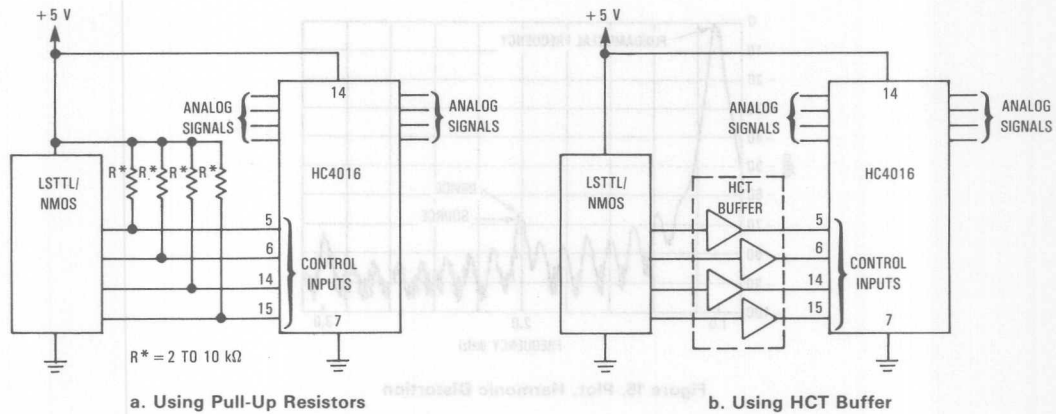


Figure 18. LSTTL/NMOS to HCMOS Interface

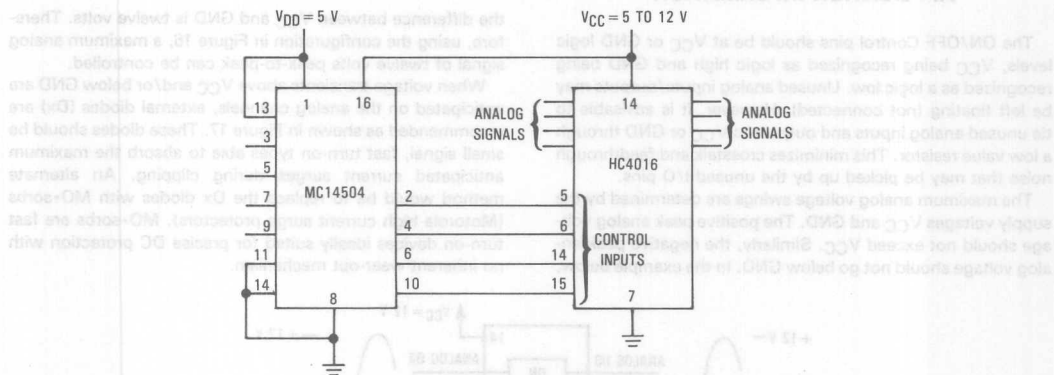


Figure 19. TTL/NMOS-to-CMOS Level Converter
Analog Signal Peak-to-Peak Greater than 5 V
 (Also see HC4316)

5

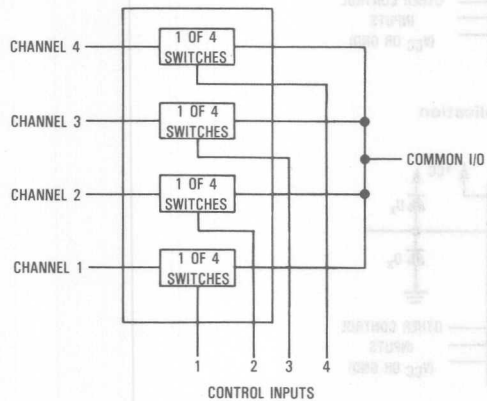


Figure 20. 4-Input Multiplexer

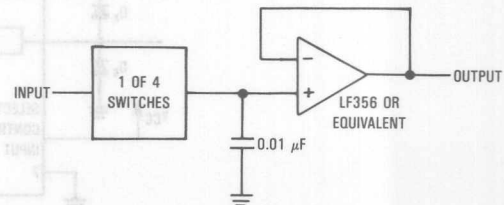


Figure 21. Sample/Hold Amplifier

MC54/74HC4017

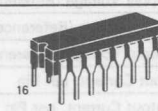
Decade Counter

High-Performance Silicon-Gate CMOS

The MC54/74HC4017 is identical in pinout to the standard CMOS MC14017B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4017 uses a five stage Johnson counter and decoding logic to provide high-speed operation. This device also has an active-high, as well as active-low clock input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 176 FETs or 44 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



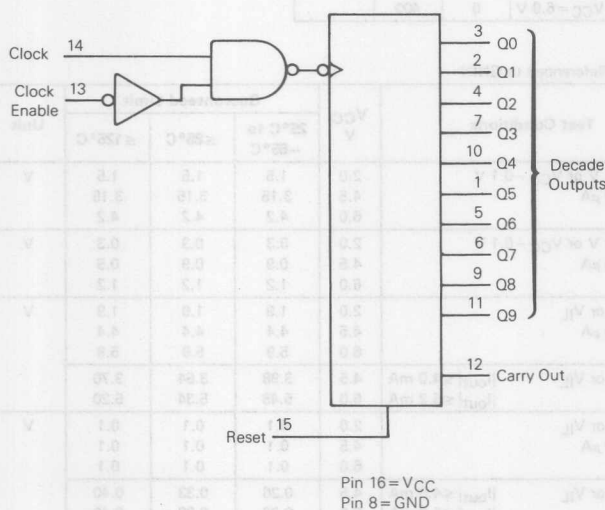
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



Pin 16 = V_{CC}
Pin 8 = GND

PIN ASSIGNMENT

Q5	1	16	V_{CC}
Q1	2	15	Reset
Q0	3	14	Clock
Q2	4	13	Clock Enable
Q6	5	12	Carry Out
Q7	6	11	Q9
Q3	7	10	Q4
GND	8	9	Q8

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4017

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 9)	2.0 4.5 6.0	4.0 20 24	3.2 16 19	2.6 13 15	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 9)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Carry Out (Figures 2 and 9)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 3 and 9)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
t_{PLH}	Maximum Propagation Delay, Reset to Carry Out (Figures 3 and 9)	2.0 4.5 6.0	230 46 39	290 58 49	345 69 59	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock Enable to Q (Figures 4 and 9)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock Enable to Carry Out (Figures 5 and 9)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 8 and 9)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V		pF
		35		





MC54/74HC4017

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Clock Enable to Clock (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_{su}	Minimum Setup Time, Clock Enable to Clock (Inhibit Count) (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_h	Minimum Hold Time, Clock to Clock Enable (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t_{rec}	Minimum Recovery Time, Reset to Clock (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_w	Minimum Pulse Width, Clock Input (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Reset Input (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Clock Enable Input (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

FUNCTION TABLE

Clock	Clock Enable	Reset	Output State*
L	X	L	no change
X	H	L	no change
X	X	H	reset counter, Q0 = H, Q1-Q9 = L, C0 = H
	L	L	advance to next state
	X	L	no change
X		L	no change
H		L	advance to next state

X = Don't care

* Carry Out = H for Q0, Q1, Q2, Q3, or Q4 = H; Carry Out = L otherwise.

PIN DESCRIPTIONS

INPUTS

CLOCK (PIN 14) — Counter clock input. While Clock Enable is low, a low-to-high transition on this input advances the counter to its next state.

RESET (PIN 15) — Asynchronous counter reset input. A high level at this input initializes the counter and forces Q0 and Carry Out to a high, Q1-Q9 are forced to a low level.

CLOCK ENABLE (PIN 13) — Active-low clock enable input. A low level on this input allows the device to count. A high level on this input inhibits the counting operation. This input may also be used as a negative-edge clock input, using Clock (Pin 14) as an active-high enable pin.

OUTPUTS

Q0-Q9 (PINS 3, 2, 4, 7, 10, 1, 5, 6, 9, 11) — Decoded decade counter outputs. Each of these outputs is high for one clock period only.

CARRY OUT (PIN 12) — Cascading output pin. This output is used either as a cascading output or a symmetrical divide-by-ten output. This output goes low when a count of five is reached and high when the counter advances to zero or when reset. When the counters are cascaded this output provides a rising-edge signal for the clock input of the next counter stage.

MC54/74HC4017

SWITCHING WAVEFORMS

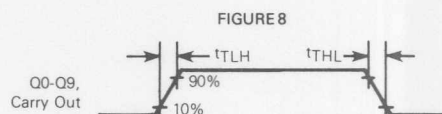
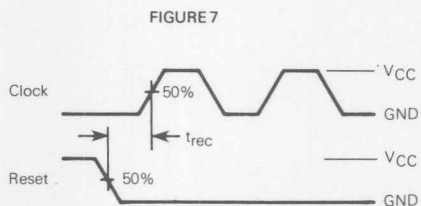
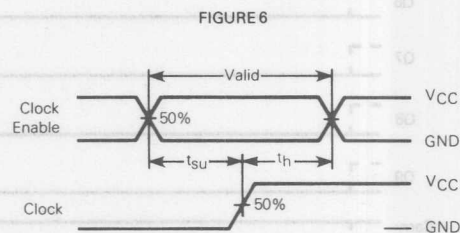
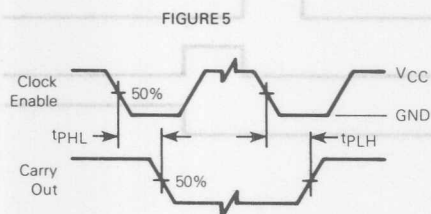
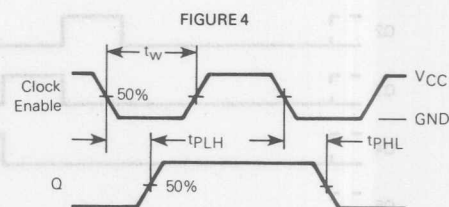
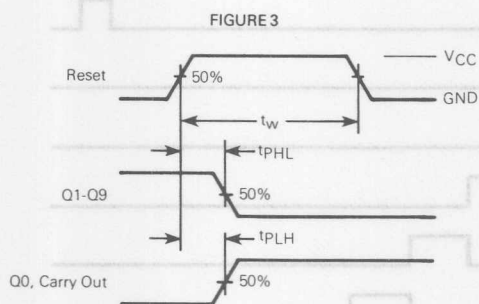
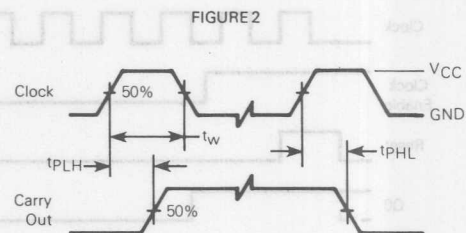
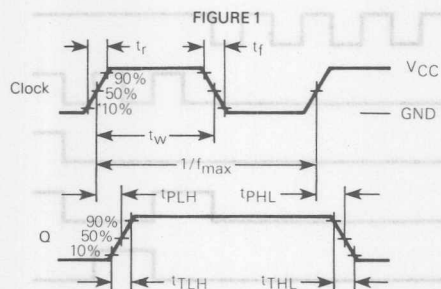
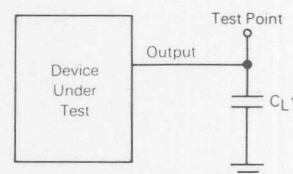


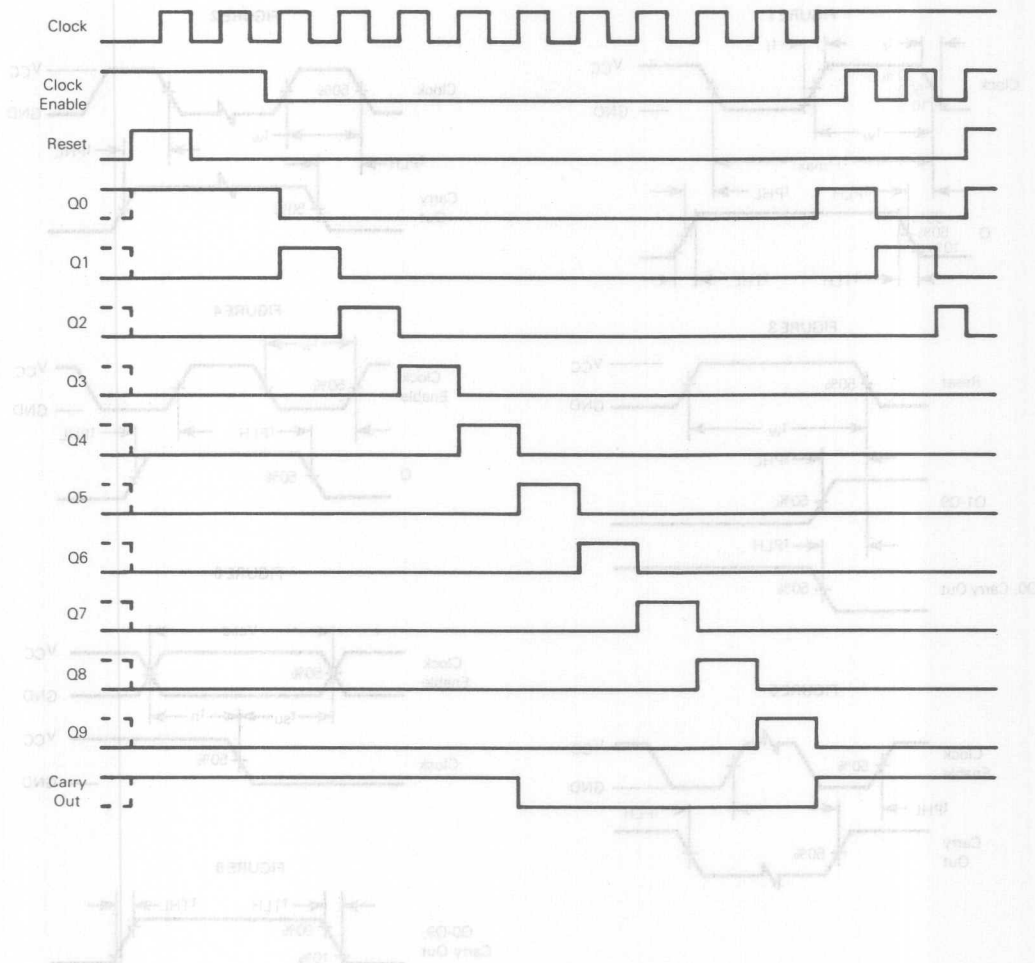
FIGURE 9 — TEST CIRCUIT



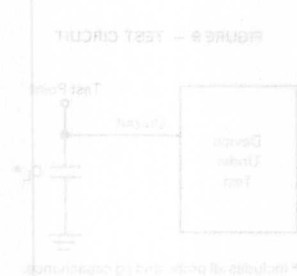
* Includes all probe and jig capacitance.

MC54/74HC4017

5. TIMING DIAGRAM

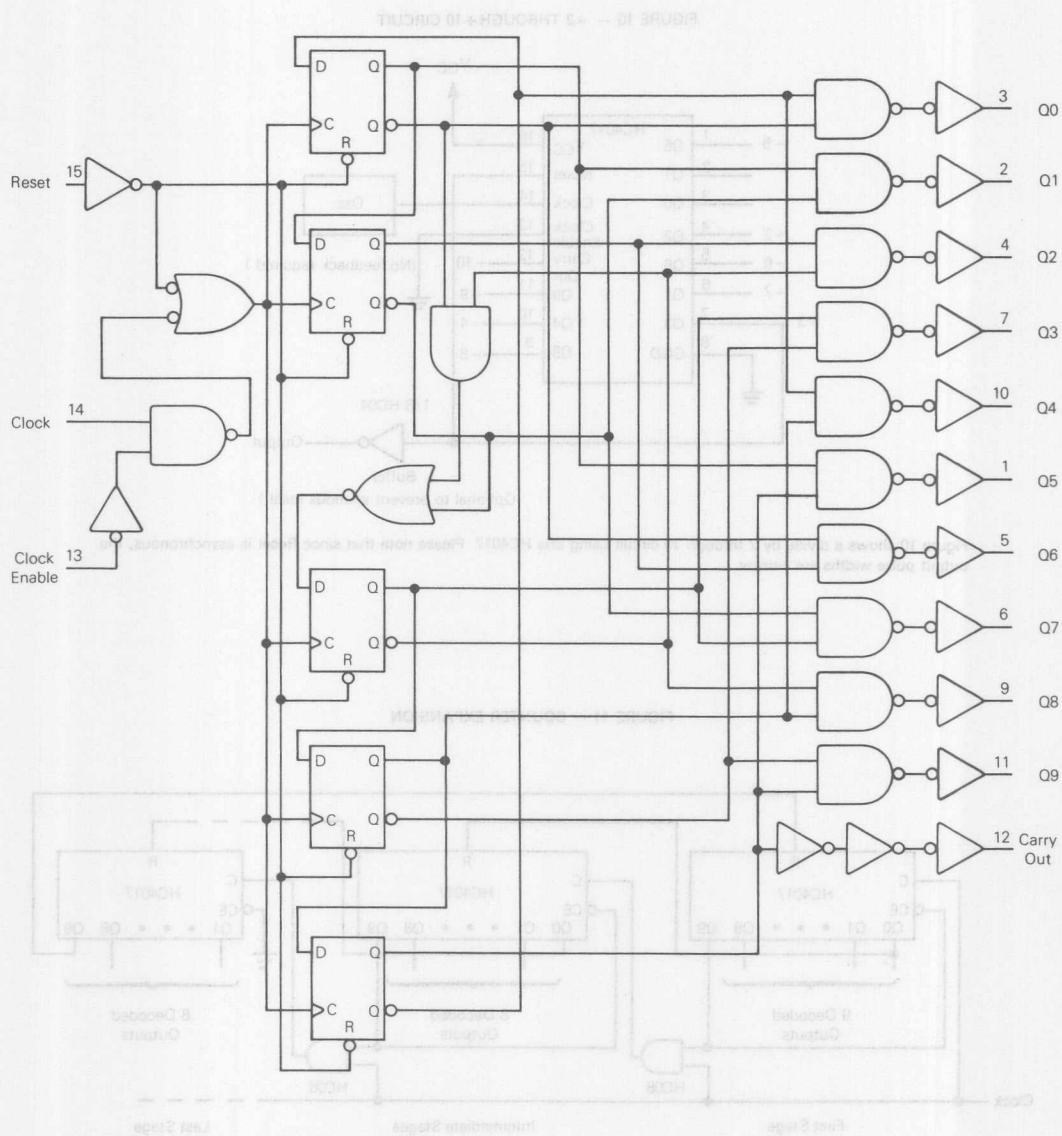


5



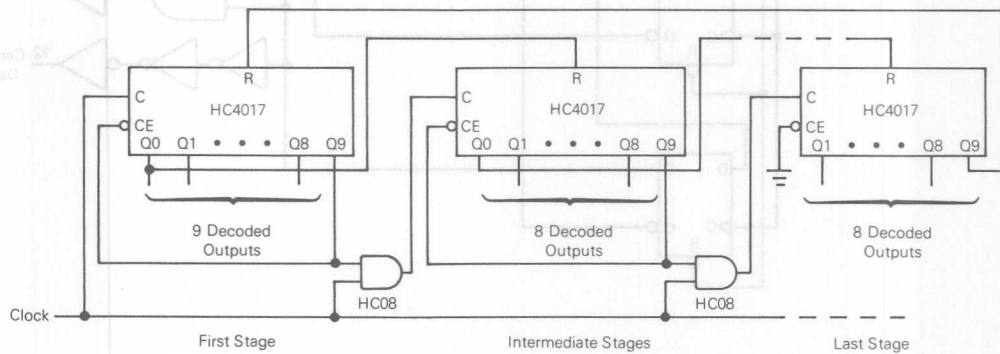
MC54/74HC4017

EXPANDED LOGIC DIAGRAM



TYPICAL APPLICATIONS

FIGURE 11 — COUNTER EXPANSION



5

MC54/74HC4020

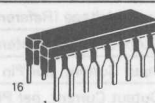
14-Stage Binary Ripple Counter High-Performance Silicon-Gate CMOS

The MC54/74HC4020 is identical in pinout to the standard CMOS MC14020B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

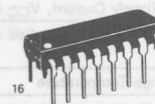
This device consists of 14 master-slave flip-flops with 12 stages brought out to pins. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4020 for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 620**



**N SUFFIX
PLASTIC
CASE 648**



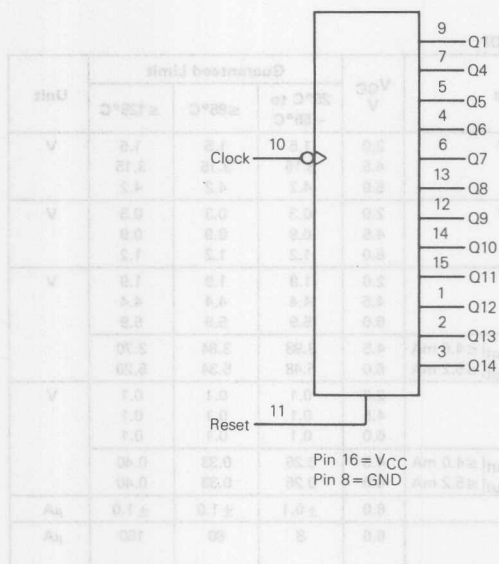
**D SUFFIX
SOIC
CASE 751**

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Q12	1	16	V_{CC}
Q13	2	15	Q11
Q14	3	14	Q10
Q6	4	13	Q8
Q5	5	12	Q9
Q7	6	11	Reset
Q4	7	10	Clock
GND	8	9	Q1

FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4020

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t _{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Q _N to Q _{N+1} (Figures 3 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
 - Information on typical parametric values can be found in Chapter 4.
- *For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:
V_{CC} = 2.0 V: t_p = [205 + 107.5(N - 1)] ns
V_{CC} = 4.5 V: t_p = [41 + 21.5(N - 1)] ns
V_{CC} = 6.0 V: t_p = [35 + 18.3(N - 1)] ns

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		30	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4020

PIN DESCRIPTIONS

INPUTS

CLOCK (PIN 10) — Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

RESET (PIN 11) — Active-high reset. A high level applied

to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1, Q4—Q14 (PINS 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3) — Active-high outputs. Each QN output divides the Clock input frequency by 2^N .

SWITCHING WAVEFORMS

FIGURE 1

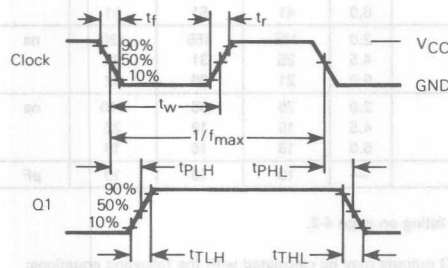


FIGURE 3

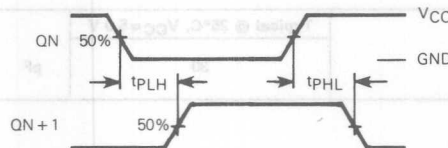


FIGURE 2

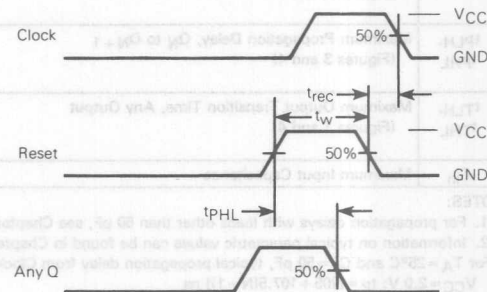
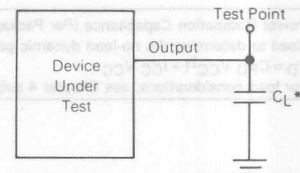
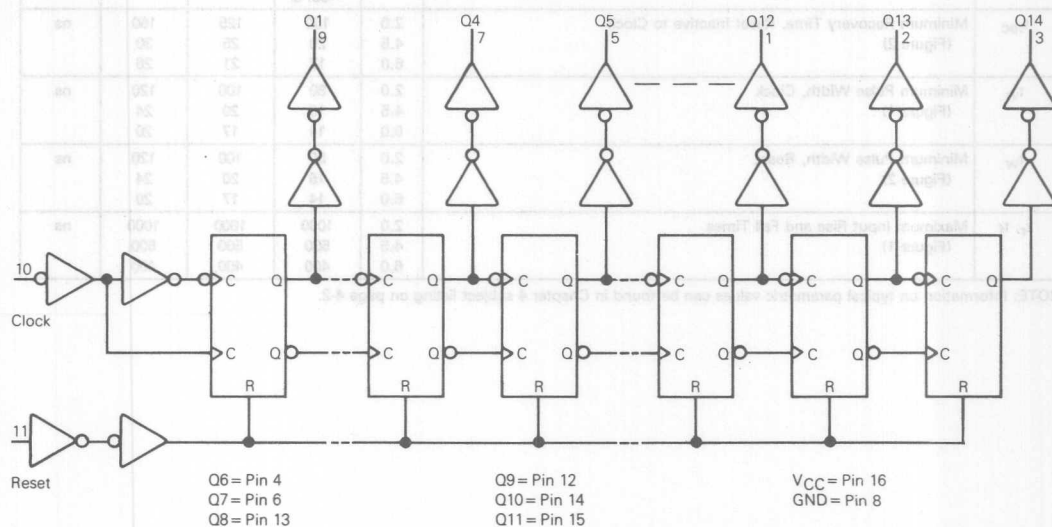


FIGURE 4 — TEST CIRCUIT

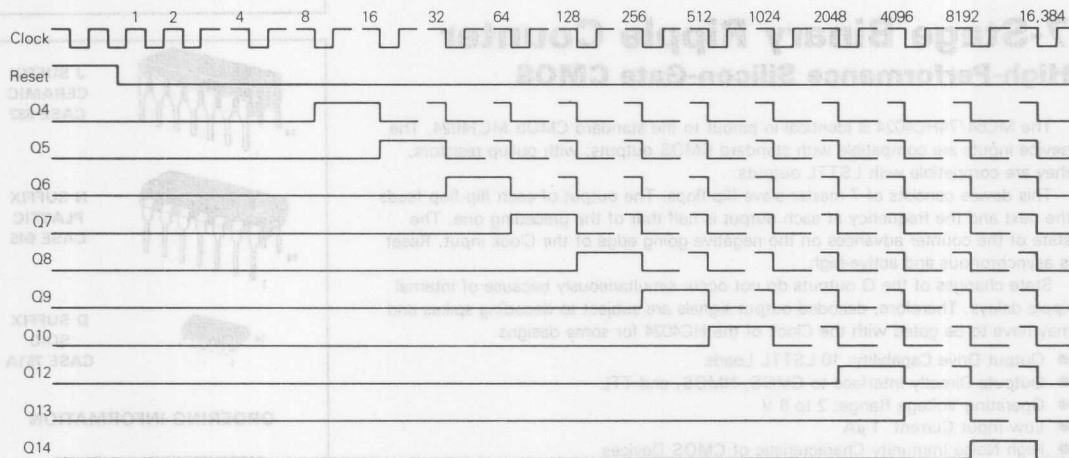


* Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM

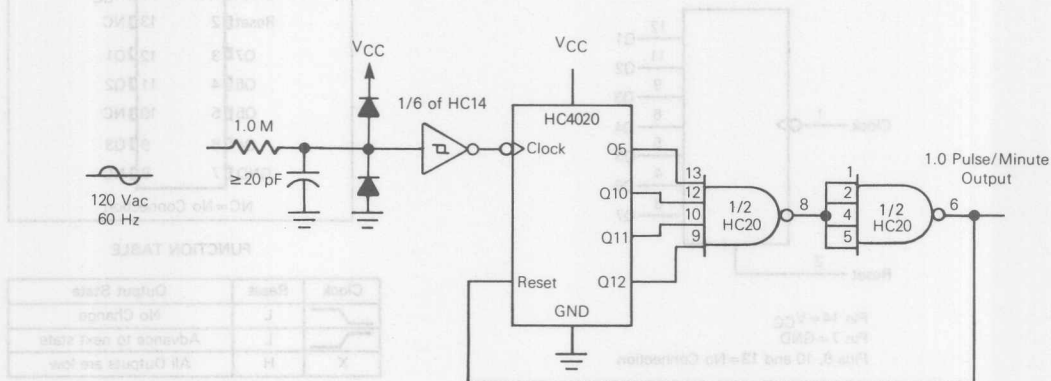


APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the MC54/74HC14, Schmitt-trigger inverter. The HC14 squares-up the input waveform and feeds the

HC4020. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



MC54/74HC4024

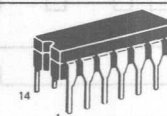
7-Stage Binary Ripple Counter High-Performance Silicon-Gate CMOS

The MC54/74HC4024 is identical in pinout to the standard CMOS MC14024. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

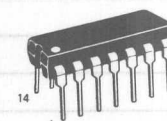
This device consists of 7 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4024 for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 206 FETs or 51.5 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 632**



**N SUFFIX
PLASTIC
CASE 646**



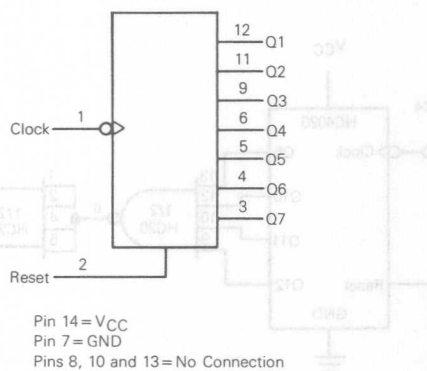
**D SUFFIX
SOIC
CASE 751A**

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Clock	1	14	V_{CC}
Reset	2	13	NC
Q7	3	12	Q1
Q6	4	11	Q2
Q5	5	10	NC
Q4	6	9	Q3
GND	7	8	NC

NC = No Connection

FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

MC54/74HC4024

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	6.0	8	80	160	μ A

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4024

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, Input t_r=t_f=6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	5.4 27 32	4.4 22 26	3.6 18 21	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t _{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, QN to QN + 1 (Figures 3 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

*For T_A=25°C and C_L=50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC}=2.0\text{ V: } t_p = [205 + 100(N-1)] \text{ ns}$$

$$V_{CC}=4.5\text{ V: } t_p = [41 + 20(N-1)] \text{ ns}$$

$$V_{CC}=6.0\text{ V: } t_p = [35 + 17(N-1)] \text{ ns}$$

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} =5.0 V	pF
		30	

TIMING REQUIREMENTS (Input t_r=t_f=6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

PIN DESCRIPTIONS

INPUTS

CLOCK (PIN 1) — Negative-edge triggering clock input. A high-to-low transition of this input advances the state of the counter.

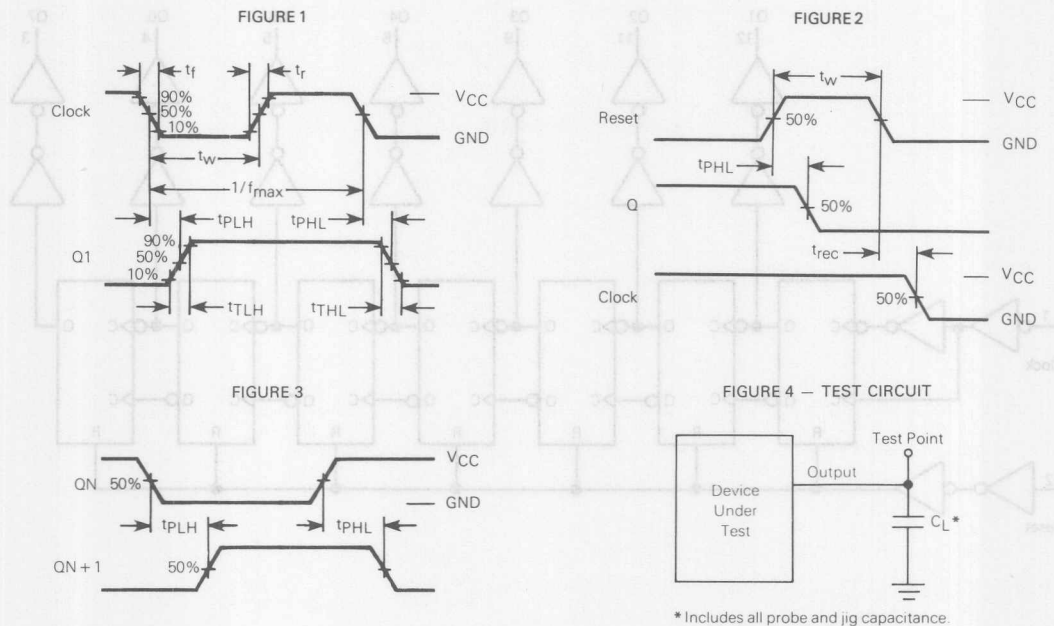
RESET (PIN 2) — Active-high asynchronous reset. A high level applied to this input resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

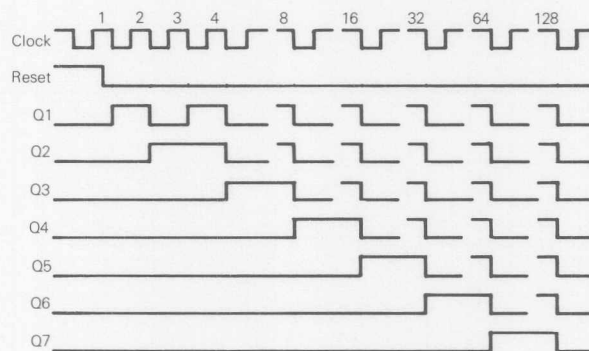
Q1-Q7 (PINS 12, 11, 9, 6, 5, 4, 3) — Active-high outputs. Each QN output divides the Clock input frequency by 2^N.

MC54/74HC4024

SWITCHING WAVEFORMS

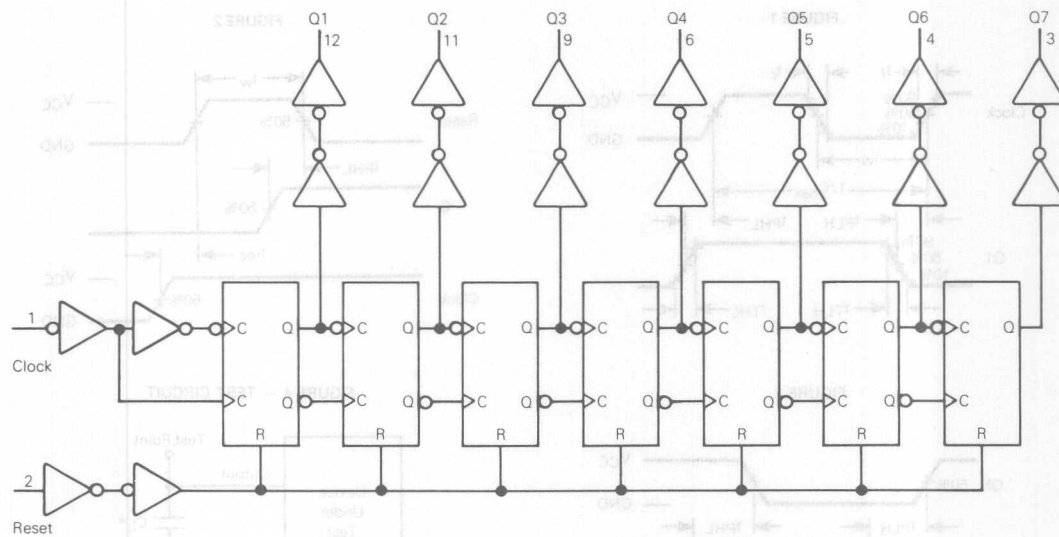


TIMING DIAGRAM

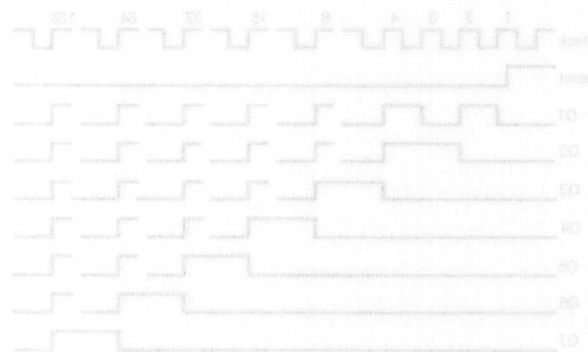


MC54/74HC4024

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



MC54/74HC4040

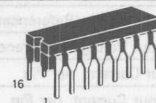
12-Stage Binary Ripple Counter High-Performance Silicon-Gate CMOS

The MC54/74HC4040 is identical in pinout to the standard CMOS MC14040. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

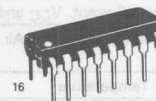
This device consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4040 for some designs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates



**J SUFFIX
CERAMIC
CASE 620**



**N SUFFIX
PLASTIC
CASE 648**



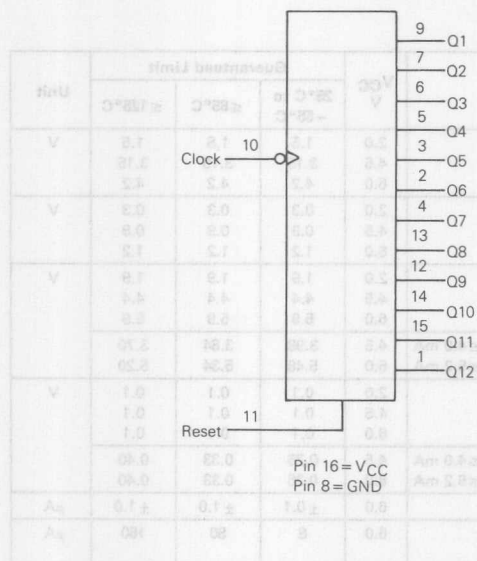
**D SUFFIX
SOIC
CASE 751**

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ\text{C}$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN ASSIGNMENT

Q12	1	16	V_{CC}
Q6	2	15	Q11
Q5	3	14	Q10
Q7	4	13	Q8
Q4	5	12	Q9
Q3	6	11	Reset
Q2	7	10	Clock
GND	8	9	Q1

FUNCTION TABLE

Clock	Reset	Output State
L	L	No Change
L	H	Advance to next state
X	H	All Outputs are low

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ 0 1000 $V_{CC} = 4.5 \text{ V}$ 0 500 $V_{CC} = 6.0 \text{ V}$ 0 400		ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4040

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	5.0 25 29	4.0 20 24	3.4 17 20	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q1* (Figures 1 and 4)	2.0 4.5 6.0	210 42 36	265 53 45	315 63 54	ns
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, QN to QN+1 (Figures 3 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

*For $T_A = 25^\circ\text{C}$ and $C_L = 50$ pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC} = 2.0 \text{ V: } t_p = [205 + 107.5(N - 1)] \text{ ns}$$

$$V_{CC} = 4.5 \text{ V: } t_p = [41 + 21.5(N - 1)] \text{ ns}$$

$$V_{CC} = 6.0 \text{ V: } t_p = [35 + 18.3(N - 1)] \text{ ns}$$

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		35	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

PIN DESCRIPTIONS

INPUTS

CLOCK (PIN 10) — Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

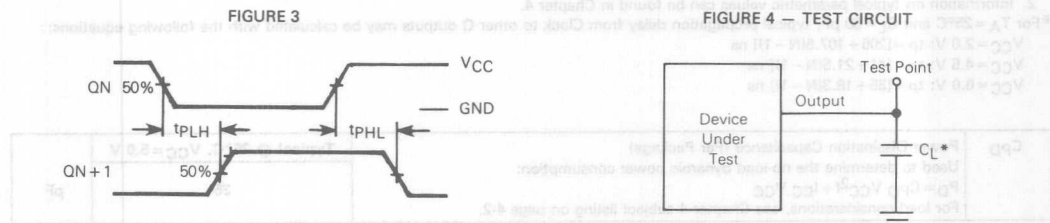
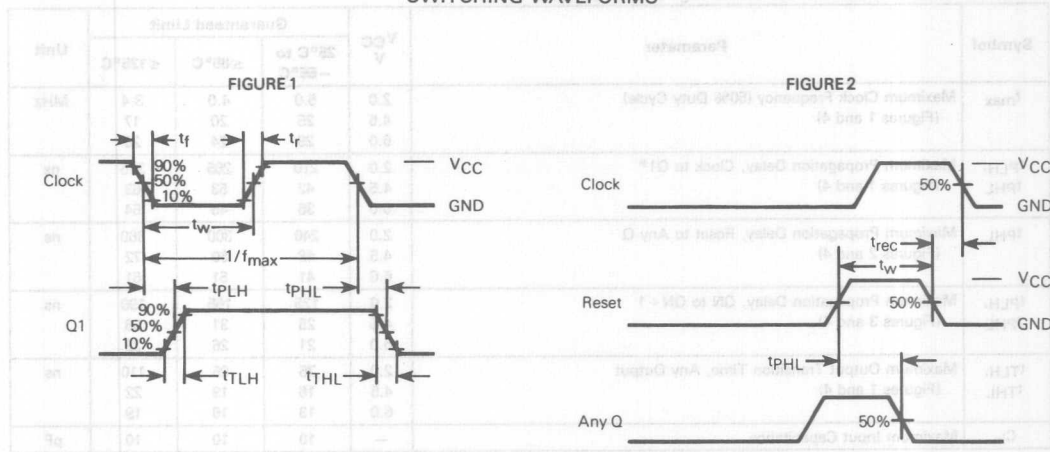
RESET (PIN 11) — Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

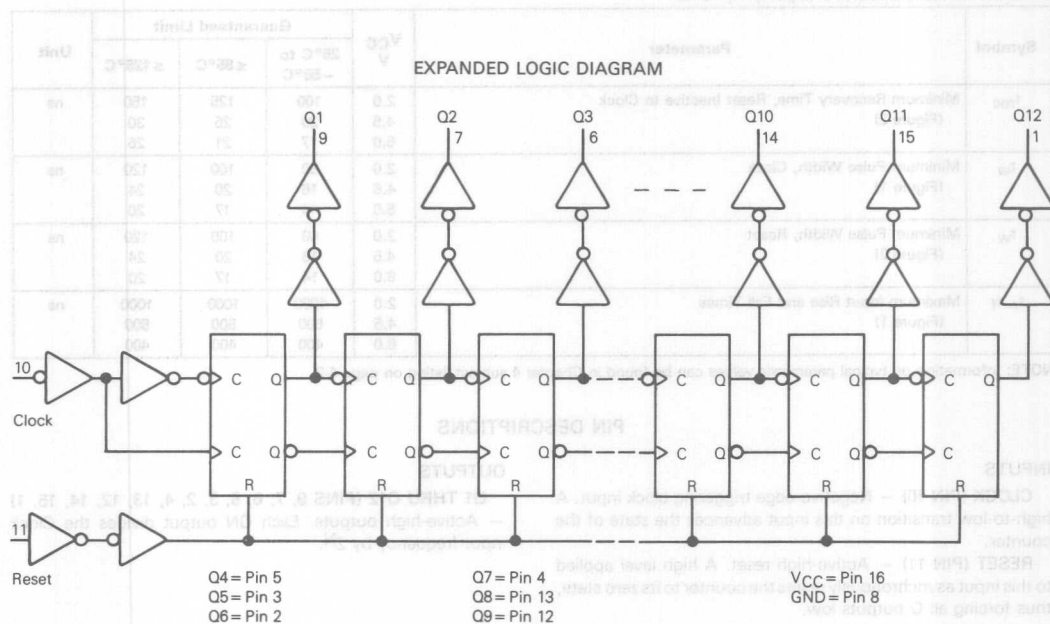
Q1 THRU Q12 (PINS 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1) — Active-high outputs. Each QN output divides the Clock input frequency by 2^N .

MC54/74HC4040

SWITCHING WAVEFORMS

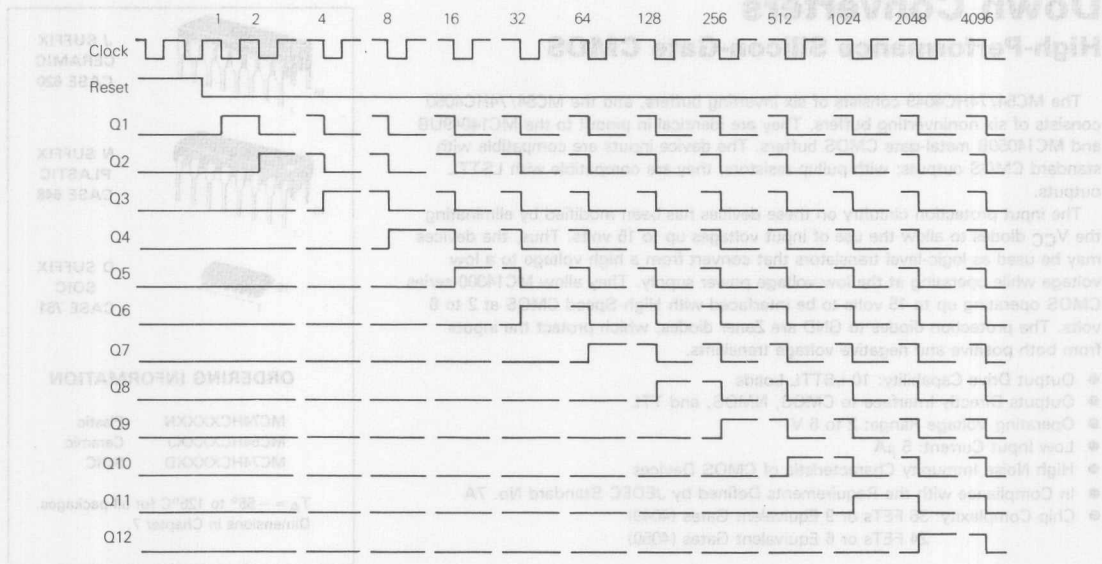


* Includes all probe and jig capacitance.



MC54/74HC4040

TIMING DIAGRAM

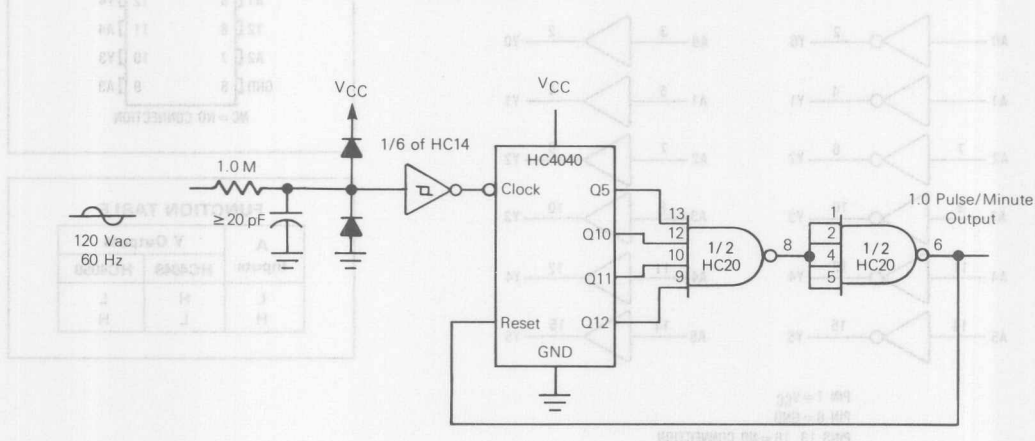


APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sine wave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the input of the HC14, Schmitt-trigger inverter. The HC14 squares-up the input waveform and feeds the HC4040.

Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



Hex Buffers/Logic-Level Down Converters

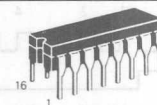
High-Performance Silicon-Gate CMOS

The MC54/74HC4049 consists of six inverting buffers, and the MC54/74HC4050 consists of six noninverting buffers. They are identical in pinout to the MC14049UB and MC14050B metal-gate CMOS buffers. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

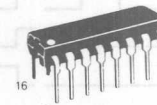
The input protection circuitry on these devices has been modified by eliminating the V_{CC} diodes to allow the use of input voltages up to 15 volts. Thus, the devices may be used as logic-level translators that convert from a high voltage to a low voltage while operating at the low-voltage power supply. They allow MC14000-series CMOS operating up to 15 volts to be interfaced with High-Speed CMOS at 2 to 6 volts. The protection diodes to GND are Zener diodes, which protect the inputs from both positive and negative voltage transients.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 5 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 36 FETs or 9 Equivalent Gates (4049)
24 FETs or 6 Equivalent Gates (4050)

MC54/74HC4049 MC54/74HC4050



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



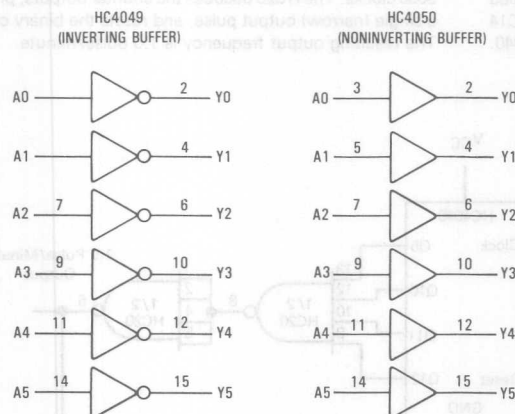
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAMS



PIN 1 = V_{CC}
PIN 8 = GND
PINS 13, 16 = NO CONNECTION

PIN ASSIGNMENT

V_{CC}	1	16	NC
Y0	2	15	Y5
A0	3	14	A5
Y1	4	13	NC
A1	5	12	Y4
Y2	6	11	A4
A2	7	10	Y3
GND	8	9	A3

NC = NO CONNECTION

FUNCTION TABLE

A Inputs	Y Outputs	
	HC4049	HC4050
L	H	L
H	L	H

MC54/74HC4049•MC54/74HC4050

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to +18	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC}+0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields **referenced to the GND pin, only**. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $GND \leq V_{in} \leq 15$ V and $GND \leq V_{out} \leq V_{CC}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in}	DC Input Voltage (Referenced to GND)	0	V _{CC} to 15	V	
V _{out}	DC Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out}=0.1$ V or $V_{CC}-0.1$ V $ I_{out} \leq 20$ μ A	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out}=0.1$ V or $V_{CC}-0.1$ V $ I_{out} \leq 20$ μ A	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in}=V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in}=V_{CC}$ or GND $V_{in}=15$ V	6.0	± 0.1	± 1.0	± 1.0	μ A
			6.0	0.5	5.0	5.0	
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in}=15$ V or GND $I_{out}=0$ μ A	6.0	2	20	40	μ A

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4049•MC54/74HC4050

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	85 17 14	105 21 18	130 26 22	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		27	

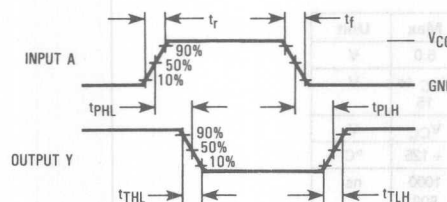


Figure 1a. Switching Waveforms (HC4049)

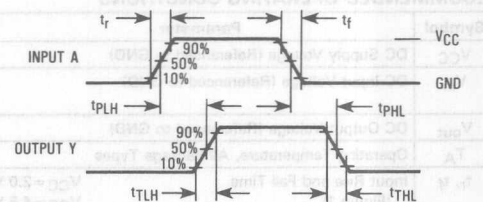


Figure 1b. Switching Waveforms (HC4050)

5

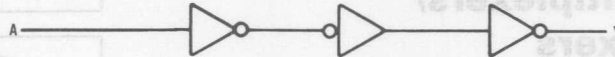
Symbol	Parameter	Test Conditions	V _{CC} V	25°C to -55°C	0°C to +75°C	Guaranteed Limit
V _{IH}	Minimum High-Level Input Voltage	V _{OH} = 0.1 V or V _{CC} - 0.1 V I _{OH} = -20 μA	2.0 4.5 6.0	1.8 3.2 4.2	1.8 3.2 4.2	1.8 3.2 4.2
V _{IL}	Maximum Low-Level Input Voltage	V _{OH} = 0.1 V or V _{CC} - 0.1 V I _{OL} = 20 μA	2.0 4.5 6.0	0.9 0.9 0.9	0.9 0.9 0.9	0.9 0.9 0.9
V _{OH}	Minimum High-Level Output Voltage	V _{IH} = V _{IH} or V _{CC} I _{OH} = -20 μA	2.0 4.5 6.0	1.8 3.2 4.2	1.8 3.2 4.2	1.8 3.2 4.2
V _{OL}	Maximum Low-Level Output Voltage	V _{IH} = V _{IH} or V _{CC} I _{OL} = 20 μA	2.0 4.5 6.0	0.9 0.9 0.9	0.9 0.9 0.9	0.9 0.9 0.9
I _{OH}	Maximum High-Level Output Current	V _{IH} = V _{IH} or V _{CC} V _{OL} = 0.1 V or V _{CC} - 0.1 V	2.0 4.5 6.0	±0.1 ±0.1 ±0.1	±0.1 ±0.1 ±0.1	±0.1 ±0.1 ±0.1
I _{OL}	Maximum Low-Level Output Current	V _{IH} = V _{IH} or V _{CC} V _{OL} = 0.1 V or V _{CC} - 0.1 V	2.0 4.5 6.0	±0.1 ±0.1 ±0.1	±0.1 ±0.1 ±0.1	±0.1 ±0.1 ±0.1
I _{CC}	Maximum Quiescent Supply Current (per package)	V _{IH} = 0 V or GND V _{OL} = 0 V or GND	2.0 4.5 6.0	±0.1 ±0.1 ±0.1	±0.1 ±0.1 ±0.1	±0.1 ±0.1 ±0.1

*Includes all probe and jig capacitance.

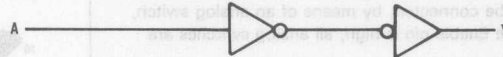
Figure 2. Test Circuit

LOGIC DETAIL

HC4049
(1/6 of the Device)

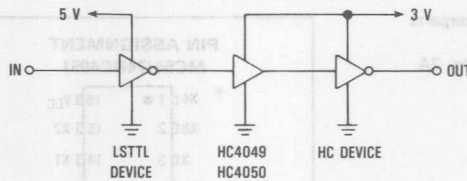


HC4050
(1/6 of the Device)

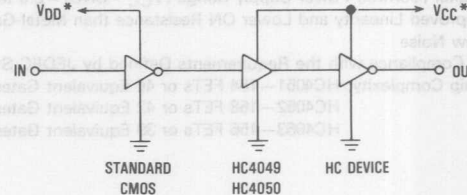


TYPICAL APPLICATIONS

LSTTL to Low-Voltage HSCMOS



High-Voltage CMOS to HSCMOS



NOTE: To determine the noise immunity for the LSTTL to low-voltage configuration, use Eq. 1 and Eq. 2:
(TTL) $V_{OH} - (CMOS) V_{IH}$ Eq. 1
(TTL) $V_{OL} - (CMOS) V_{IL}$ Eq. 2

For the supply levels shown:
 $2.4 - 3 (75\%) = 2.4 - 2.25 = 0.15 V$
 $0.4 - 3 (15\%) = 0.4 - 0.45 = 0.05 V$

Therefore, worst case noise immunity is 50 mV.
For supply levels greater than 4.5 volts use the 74HCT04 for direct interface to TTL outputs.

*Table 1. Supply Examples

V _{DD}	V _{CC}
15 V	2 V
12 V	5 V
12 V	3 V

Advance Information

Analog Multiplexers/ Demultiplexers High-Performance Silicon-Gate CMOS

The MC54/74HC4051, MC54/74HC4052, and MC54/74HC4053 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4051, HC4052, and HC4053 are identical in pinout to the metal-gate MC14051B, MC14052B, and MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is high, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (R_{ON}) is more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

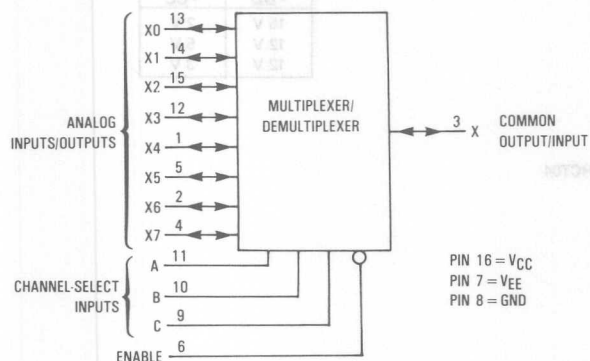
For multiplexers/demultiplexers with channel select latches, see HC4351, HC4352, and HC4353.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC} - GND$) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal-Gate Counterparts
- Low Noise
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: HC4051—184 FETs or 46 Equivalent Gates
HC4052—168 FETs or 42 Equivalent Gates
HC4053—156 FETs or 39 Equivalent Gates

5

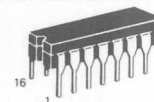
LOGIC DIAGRAM MC54/74HC4051

Single-Pole, 8-Position Plus Common Off

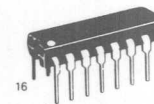


PIN 16 = V_{CC}
PIN 7 = V_{EE}
PIN 8 = GND

MC54/74HC4051 MC54/74HC4052 MC54/74HC4053



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC74HCXXXXN Plastic
MC54HCXXXXJ Ceramic
MC74HCXXXXDW SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT MC54/74HC4051



FUNCTION TABLE MC54/74HC4051

Control Inputs				ON Channels
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	None

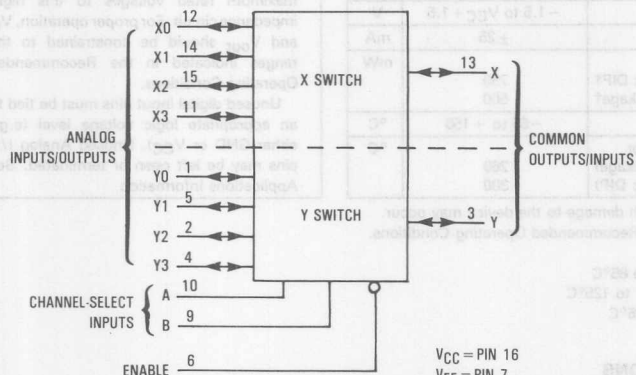
X = don't care

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

MC54/74HC4052 Double-Pole, 4-Position Plus Common Off

LOGIC DIAGRAM



PIN ASSIGNMENT

Y0	1	16	VCC
Y2	2	15	X2
Y3	3	14	X1
Y1	4	13	X
ENABLE	5	12	X0
VEE	6	11	X3
GND	7	10	A
	8	9	B

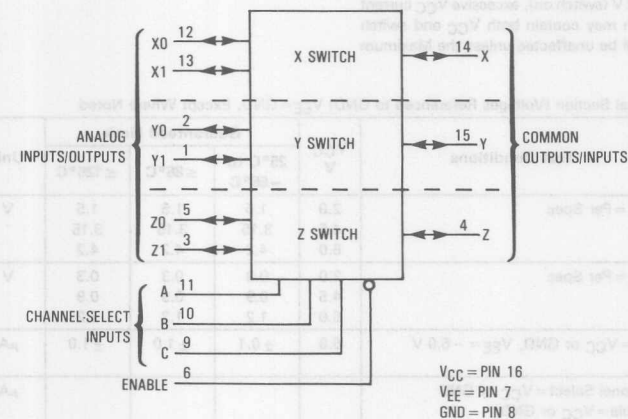
FUNCTION TABLE

Control Inputs		Select		ON Channels	
Enable		B	A		
L	L	L	L	Y0	X0
L	L	L	H	Y1	X1
L	L	H	L	Y2	X2
L	L	H	H	Y3	X3
H	X	X	X	None	

X = Don't Care

MC54/74HC4053 Triple Single-Pole, Double-Position Plus Common Off

LOGIC DIAGRAM



PIN ASSIGNMENT

Y1	1	16	VCC
Y0	2	15	Y
Z1	3	14	X
Z0	4	13	X1
ENABLE	5	12	X0
VEE	6	11	A
GND	7	10	B
	8	9	C

FUNCTION TABLE

Control Inputs		Select		ON Channels	
Enable		C	B	A	
L	L	L	L	L	Z0 Y0 X0
L	L	L	L	H	Z0 Y0 X1
L	L	L	H	L	Z0 Y1 X0
L	L	L	H	H	Z0 Y1 X1
L	L	H	L	L	Z1 Y0 X0
L	L	H	L	H	Z1 Y0 X1
L	L	H	H	L	Z1 Y1 X0
L	L	H	H	H	Z1 Y1 X1
H	X	X	X	X	None

X = Don't Care

NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X Switch, Input B controls the Y Switch, and Input C controls the Z Switch.

MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V _{EE})	−0.5 to +7.0 −0.5 to 14.0	V
V _{EE}	Negative DC Supply Voltage (Ref. to GND)	−7.0 to +0.5	V
V _{IS}	Analog Input Voltage	V _{EE} −0.5 to V _{CC} +0.5	V
V _{in}	Digital Input Voltage (Ref. to GND)	−1.5 to V _{CC} +1.5	V
I	DC Current Into or Out of Any Pin	±25	mA
P _D	Power Dissipation in Still Air Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the ranges indicated in the Recommended Operating Conditions.

Unused digital input pins must be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated. See Applications Information.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Power Dissipation Temperature Derating:

Plastic "N" Package: −10 mW/°C from 65° to 85°C
Ceramic "J" Package: −10 mW/°C from 100° to 125°C
SOIC "D" Package: −7 mW/°C from 65° to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V _{EE})	2.0 2.0	6.0 12.0	V
V _{EE}	Negative DC Supply Voltage (Ref. to GND)	−6.0	GND	V
V _{IS}	Analog Input Voltage	V _{EE}	V _{CC}	V
V _{in}	Digital Input Voltage (Ref. to GND)	GND	V _{CC}	V
V _{IO} *	Static or Dynamic Voltage Across Switch	—	1.2	V
T _A	Operating Temperature, All Package Types	−55	+125	°C
t _r , t _f	Input Rise and Fall Time, (Channel Select or Enable Inputs)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R _{ON} = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	R _{ON} = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
I _{in}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V _{in} = V _{CC} or GND, V _{EE} = −6.0 V	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V _{CC} or GND Enable = V _{CC} or GND V _{IS} = V _{CC} or GND V _{IO} = 0 V V _{EE} = GND V _{EE} = −6.0	6.0 6.0	2 8	20 80	40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V _{CC}	V _{EE}	Guaranteed Limit			Unit
					25°C to -55°C	≤85°C	≤125°C	
R _{on}	Maximum "ON" Resistance	V _{in} = V _{IL} or V _{IH}	4.5	0.0	190	240	280	Ω
		V _{IS} = V _{CC} to V _{EE}	4.5	-4.5	120	150	170	
		I _S ≤ 2.0 mA (Figures 1, 2)	6.0	-6.0	100	125	140	
		V _{in} = V _{IL} or V _{IH}	4.5	0.0	150	190	230	
ΔR _{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V _{in} = V _{IL} or V _{IH}	4.5	0.0	30	35	40	Ω
		V _{IS} = 1/2 (V _{CC} - V _{EE})	4.5	-4.5	12	15	18	
		I _S ≤ 2.0 mA	6.0	-6.0	10	12	14	
		V _{in} = V _{IL} or V _{IH}	4.5	0.0	100	125	140	
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel	V _{in} = V _{IL} or V _{IH}	6.0	-6.0	0.1	0.5	1.0	μA
		V _{IO} = V _{CC} - V _{EE}						
		Switch Off (Figure 3)						
		V _{in} = V _{IL} or V _{IH}	6.0	-6.0	0.2	2.0	4.0	
I _{on}	Maximum On-Channel Leakage Current, Channel to Channel	V _{in} = V _{IL} or V _{IH}	6.0	-6.0	0.1	1.0	2.0	μA
		V _{IO} = V _{CC} - V _{EE}						
		Switch to Switch = V _{CC} - V _{EE}						
		Switch Off (Figure 4)						
I _{on}	Maximum On-Channel Leakage Current, Channel to Channel	V _{in} = V _{IL} or V _{IH}	6.0	-6.0	0.2	2.0	4.0	μA
		V _{IO} = V _{CC} - V _{EE}						
		Switch to Switch = V _{CC} - V _{EE}						
		Switch Off (Figure 5)						

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC}	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Channel-Select to Analog Output (Figure 9)	2.0	370	465	550	ns
		4.5	74	93	110	
		6.0	63	79	94	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	290	364	430	ns
		4.5	58	73	86	
		6.0	49	62	73	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	345	435	515	ns
		4.5	69	87	103	
		6.0	59	74	87	
C _{in}	Maximum Input Capacitance, Channel-Select or Enable Inputs	—	10	10	10	pF
C _{I/O}	Maximum Capacitance Analog I/O All Switches Off	—	35	35	35	pF
		—	130	130	130	
		—	80	80	80	
		—	50	50	50	
	Feedthrough	—	1.0	1.0	1.0	

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) (Figure 13) Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V			pF
		45 (HC4051)	80 (HC4052)	45 (HC4053)	

MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

Symbol	Parameter	Test Condition	V _{CC} V	V _{EE} V	Limit*	Unit
					25°C 54/74HC	
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6)	f _{in} = 1 MHz Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{OS} Increase f _{in} Frequency Until dB Meter Reads -3 dB R _L = 50 Ω, C _L = 10 pF	2.25	-2.25	51 52 53	MHz
			4.50	-4.50	80 95 120	
			6.00	-6.00	80 95 120	
—	Off-Channel Feedthrough Isolation (Figure 7)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF	2.25	-2.25	—50	dB
			4.50	-4.50	—50	
			6.00	-6.00	—50	
		f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	2.25	-2.25	—40	
—	Feedthrough Noise, Channel Select Input to Common O/I (Figure 8)	V _{in} ≤ 1 MHz Square Wave (t _r = t _f = 6 ns) Adjust R _L at Setup so that I _S = 0 A Enable = GND R _L = 600 Ω, C _L = 50 pF	2.25	-2.25	25	mV _{pp}
			4.50	-4.50	105	
			6.00	-6.00	135	
		R _L = 10 kΩ, C _L = 10 pF	2.25	-2.25	35	
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF	2.25	-2.25	—50	dB
			4.50	-4.50	—50	
			6.00	-6.00	—50	
		f _{in} = 1 MHz, R _L = 50 Ω, C _L = 10 pF	2.25	-2.25	—60	
THD	Total Harmonic Distortion (Figure 14)	f _{in} = 1 kHz, R _L = 10 kΩ, C _L = 50 pF THD = THD _{Measured} - THD _{Source} V _{IS} = 4.0 V _{pp} sine wave V _{IS} = 8.0 V _{pp} sine wave V _{IS} = 11.0 V _{pp} sine wave	2.25	-2.25	0.10	%
			4.50	-4.50	0.08	
			6.00	-6.00	0.05	

*Limits not tested. Determined by design and verified by qualification.

5

MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

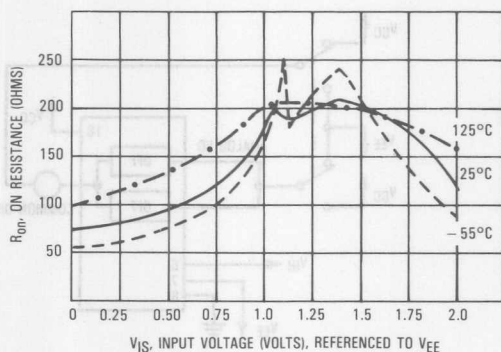


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE} = 2.0$ V

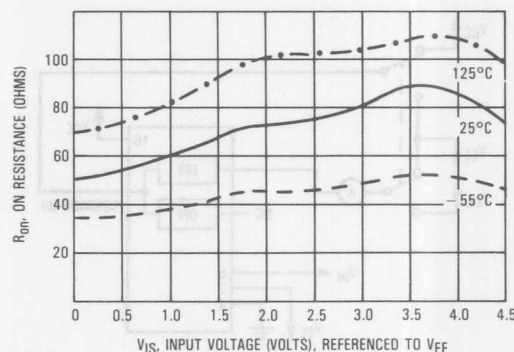


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE} = 4.5$ V

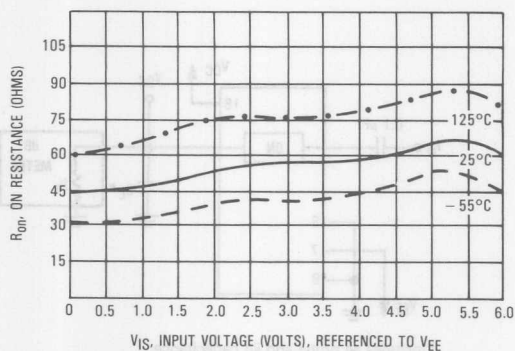


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 6.0$ V

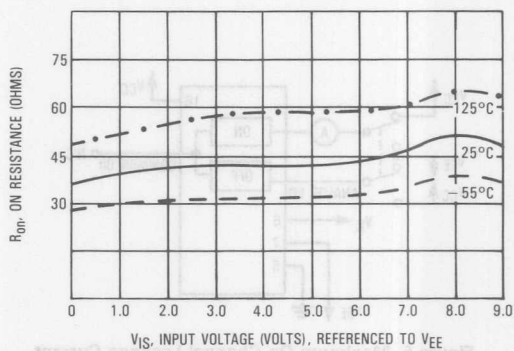


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 9.0$ V

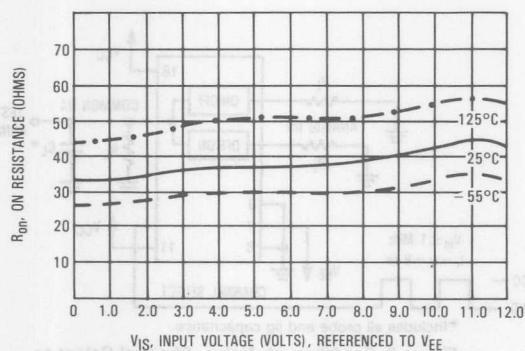


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE} = 12.0$ V

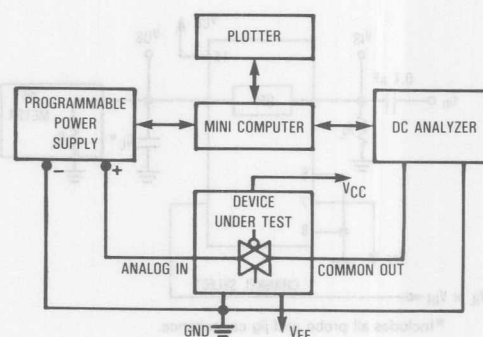


Figure 2. On Resistance Test Set-Up

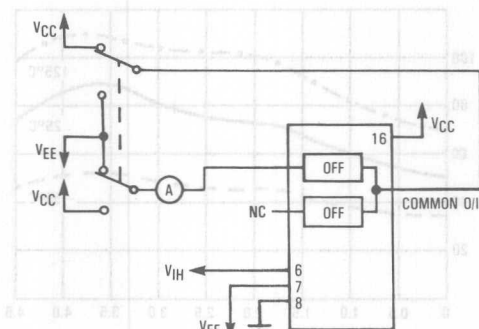


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

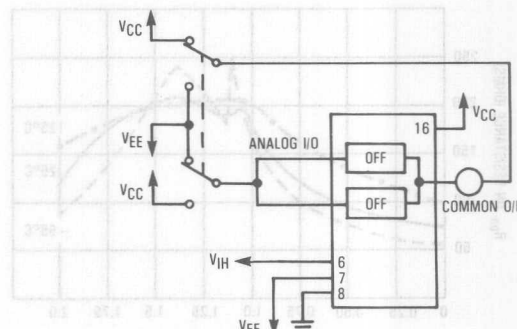


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

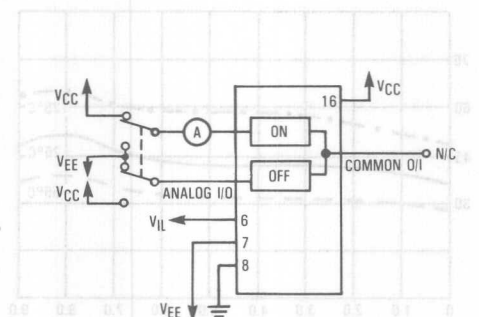
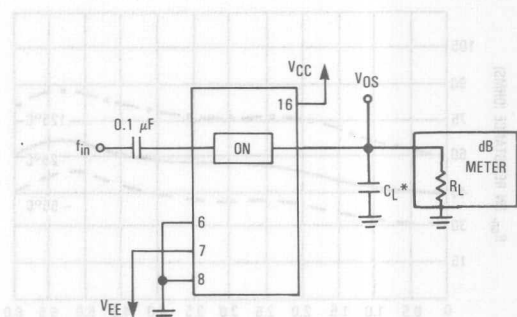


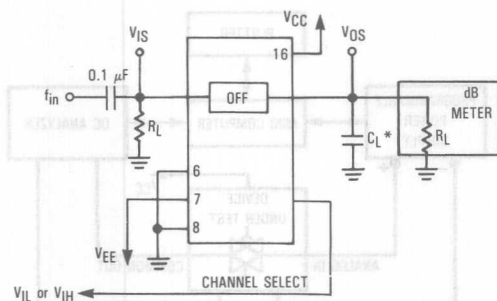
Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



*Includes all probe and jig capacitance.

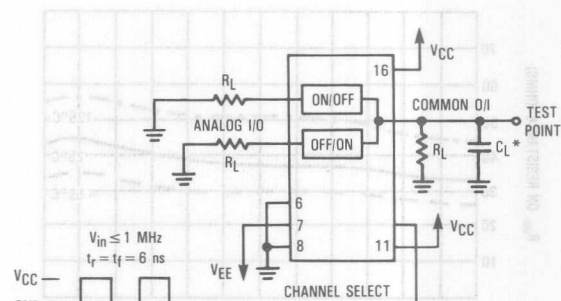
Figure 6. Maximum On-Channel Bandwidth, Test Set-Up

5



*Includes all probe and jig capacitance.

Figure 7. Off-Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

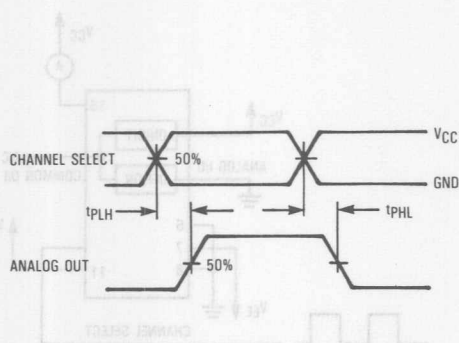
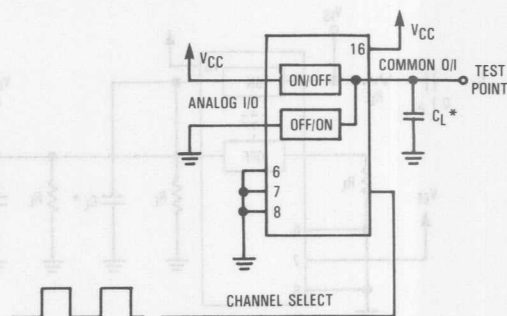


Figure 9a. Propagation Delays,
Channel Select to Analog Out



*Includes all probe and jig capacitance.

Figure 9b. Propagation Delay, Test Set-Up Channel
Select to Analog Out

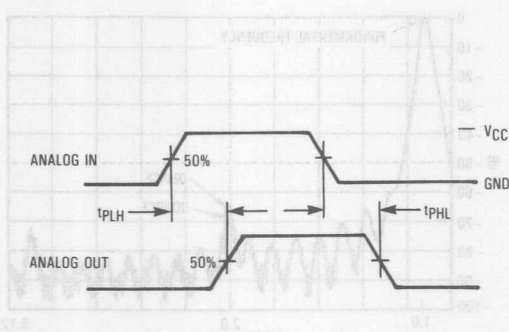
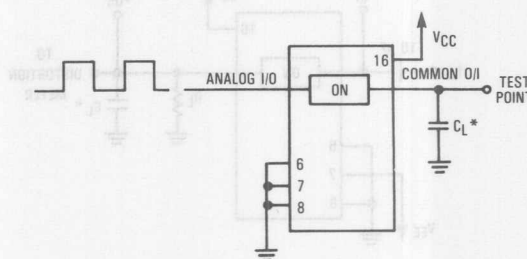


Figure 10a. Propagation Delays,
Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 10b. Propagation Delay, Test Set-Up
Analog In to Analog Out

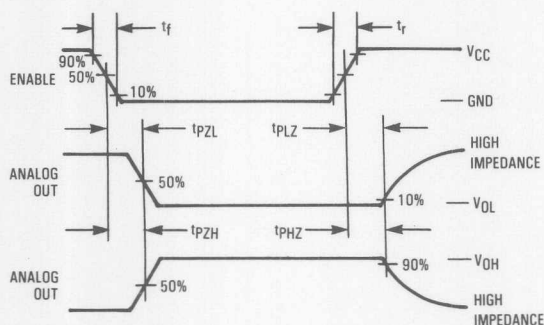


Figure 11a. Propagation Delays,
Enable to Analog Out

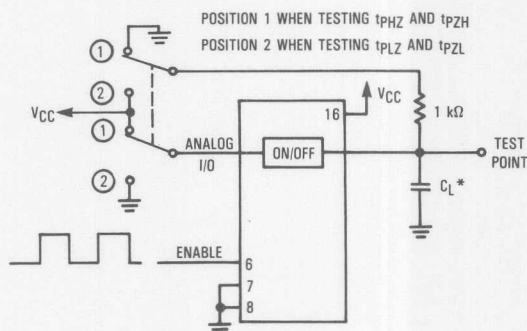
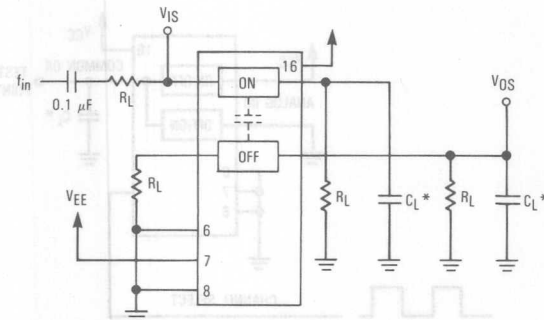


Figure 11b. Propagation Delay, Test Set-Up
Enable to Analog Out

MC54/74HC4051 • MC54/74HC4052 • MC54/74HC4053



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

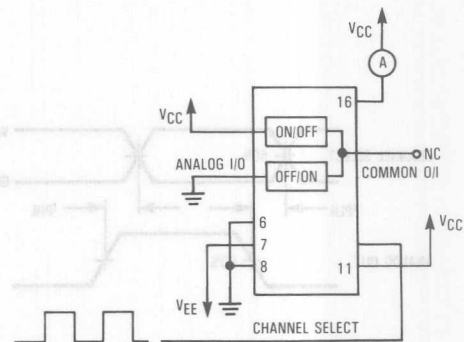
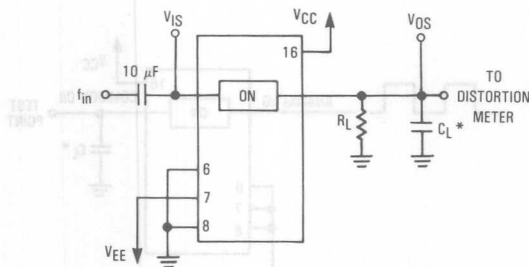


Figure 13. Power Dissipation Capacitance, Test Set-Up



*Includes all probe and jig capacitance.

Figure 14a. Total Harmonic Distortion, Test Set-Up

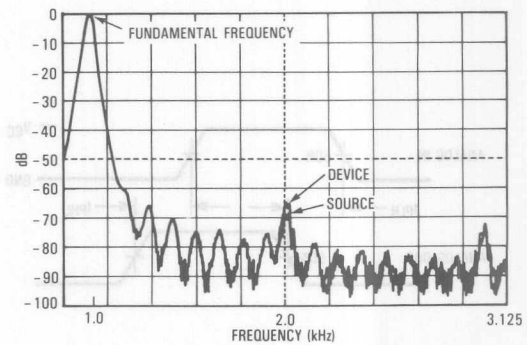


Figure 14b. Plot, Harmonic Distortion

5

MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$V_{CC} = +5\text{ V} = \text{logic high}$
 $GND = 0\text{ V} = \text{logic low}$

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below V_{EE} . In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration in Figure 15, a maximum analog signal of

ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked-up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$V_{CC} - GND = 2\text{ to }6\text{ volts}$
 $V_{EE} - GND = 0\text{ to }-6\text{ volts}$
 $V_{CC} - V_{EE} = 2\text{ to }12\text{ volts}$
 and $V_{EE} \leq GND$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

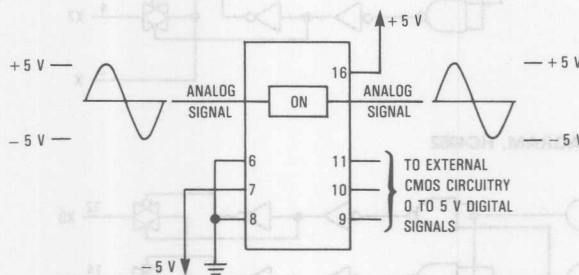


Figure 15. Application Example

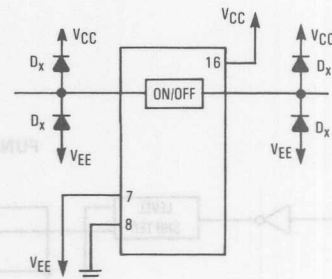
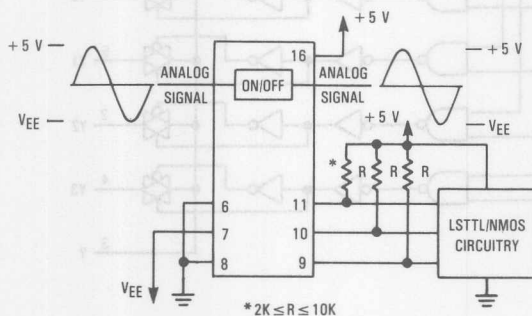
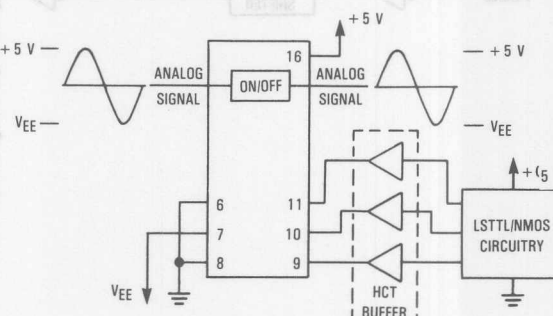


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull-Up Resistors

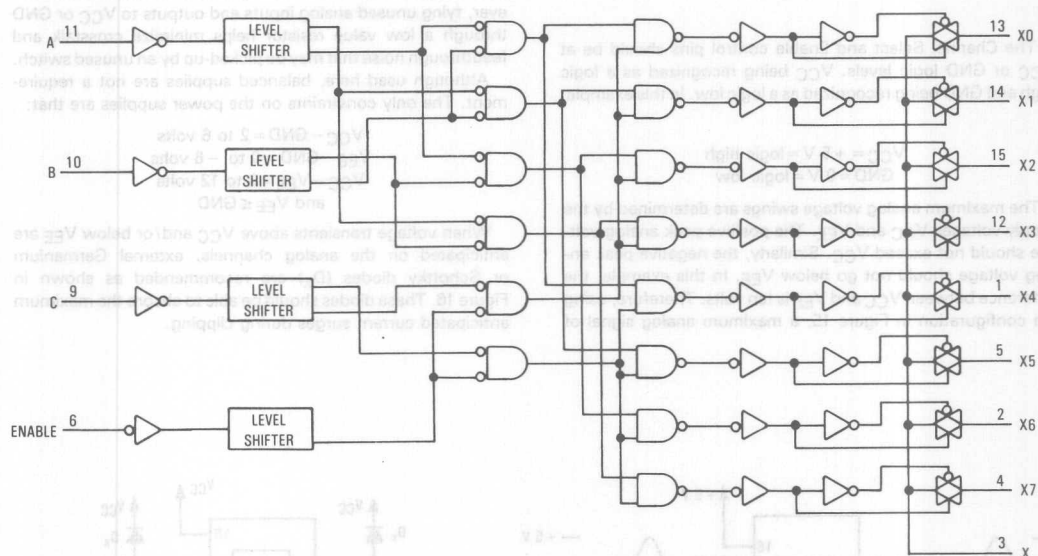


b. Using HCT Interface

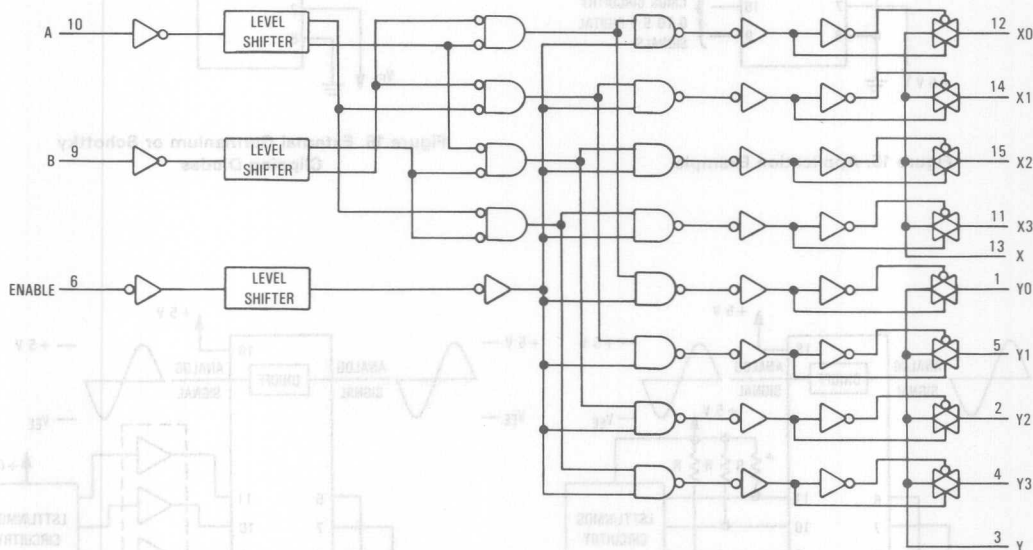
Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

MC54/74HC4051•MC54/74HC4052•MC54/74HC4053

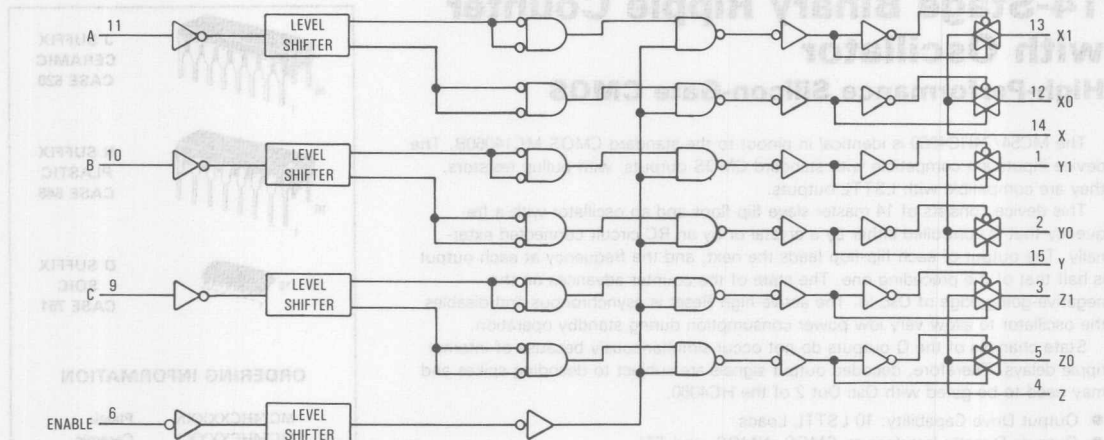
FUNCTION DIAGRAM, HC4051



FUNCTION DIAGRAM, HC4052



FUNCTION DIAGRAM, HC4053

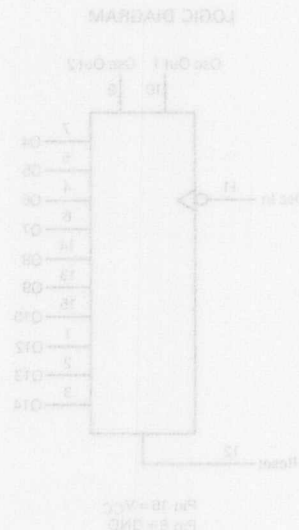


PIN ASSIGNMENT

Pin	Function
1	Y1
2	Y0
3	Z1
4	Z
5	Z0
6	ENABLE
9	C
10	B
11	A
12	X0
13	X1
14	X
15	Y

FUNCTION TABLE

Output State	Reset	Q
Q0 to Q7	L	Q0 to Q7
Q0 to Q7	H	Q0 to Q7



MC54/74HC4060

14-Stage Binary Ripple Counter with Oscillator

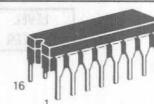
High-Performance Silicon-Gate CMOS

The MC54/74HC4060 is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

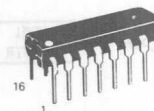
This device consists of 14 master-slave flip-flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip-flop feeds the next, and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of Osc In. The active-high Reset is asynchronous and disables the oscillator to allow very low power consumption during standby operation.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may need to be gated with Osc Out 2 of the HC4060.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 390 FETs or 97.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



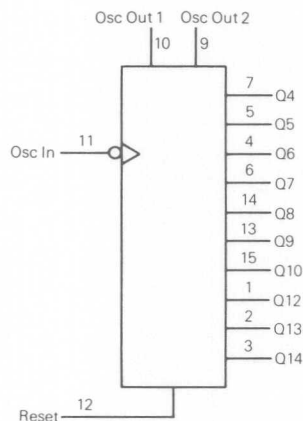
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



Pin 16 = VCC
 Pin 8 = GND

PIN ASSIGNMENT

Q12	1	16	VCC
Q13	2	15	Q10
Q14	3	14	Q8
Q6	4	13	Q9
Q5	5	12	Reset
Q7	6	11	Osc In
Q4	7	10	Osc Out 1
GND	8	9	Osc Out 2

FUNCTION TABLE

Osc In	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

MC54/74HC4060

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	- 65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
Ceramic DIP: - 10 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.5**	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	- 55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

**The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 11 with an external clock source.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to - 55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage (Q4-Q10, Q12-Q14)	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
V_{OL}	Maximum Low-Level Output Voltage (Q4-Q10, Q12-Q14)	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	

MC54/74HC4060

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND) (Continued)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{OH}	Minimum High-Level Output Voltage (Osc Out 1, Osc Out 2)	V _{in} = V _{CC} or GND I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{CC} or GND I _{out} ≤ 1.0 mA I _{out} ≤ 1.3 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage (Osc Out 1, Osc Out 2)	V _{in} = V _{CC} or GND I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{CC} or GND I _{out} ≤ 1.0 mA I _{out} ≤ 1.3 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	5.0	4.0	3.4	MHz
		4.5	25	20	17	
		6.0	29	24	20	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Osc In to Q4* (Figures 1 and 4)	2.0	530	665	795	ns
		4.5	106	133	159	
		6.0	91	114	135	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Osc In to Q14* (Figures 1 and 4)	2.0	1600	2000	2400	ns
		4.5	320	400	480	
		6.0	272	344	408	
t _{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0	240	300	360	ns
		4.5	48	60	72	
		6.0	41	51	61	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, QN to QN + 1 (Figures 3 and 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
 - Information on typical parametric values can be found in Chapter 4.
- *For T_A = 25°C and C_L = 50 pF, typical propagation delay from Osc In to other Q outputs may be calculated with the following equations:
V_{CC} = 2.0 V: t_p = [205 + 107.5(N - 1)] ns
V_{CC} = 4.5 V: t_p = [41 + 21.5(N - 1)] ns
V_{CC} = 6.0 V: t_p = [35 + 18.3(N - 1)] ns

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

MC54/74HC4060

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Osc In* (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_w	Minimum Pulse Width, Osc In (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

*Osc In driven with external clock.

PIN DESCRIPTIONS

INPUTS

OSC IN (PIN 11) — Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

RESET (PIN 12) — Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

OUTPUTS

Q4-Q10, Q12-Q14 (PINS 7, 5, 4, 6, 14, 13, 15, 1, 2, 3) — Active-high outputs. Each QN output divides the oscillator

frequency by 2^N . The user should note that Q1, Q2, Q3, and Q11 are not available as outputs.

OSC OUT 1, OSC OUT 2 (PINS 10, 9) — Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator. (See Figures 4 and 5). When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 must be left open circuited. With the crystal oscillator configuration in Figure 6, Osc Out 2 must be left open circuited.

SWITCHING WAVEFORMS

FIGURE 1

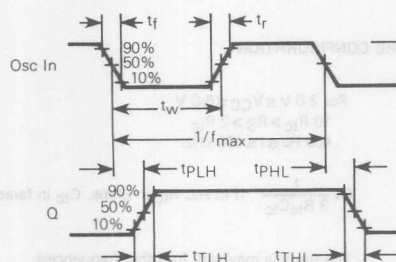


FIGURE 3

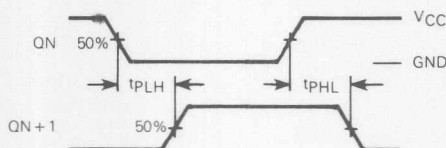


FIGURE 2

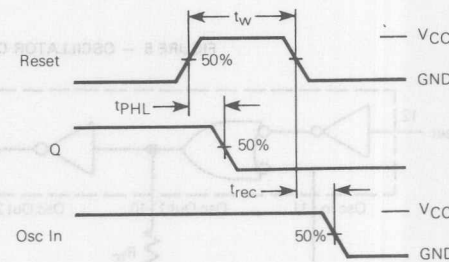
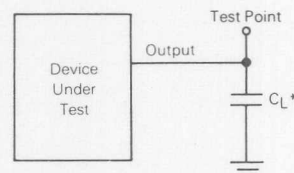


FIGURE 4 — TEST CIRCUIT



* Includes all probe and jig capacitance.

EXPANDED LOGIC DIAGRAM

5

The formula may vary for other frequencies.

MC54/74HC4060

FIGURE 6 — PIERCE CRYSTAL OSCILLATOR CIRCUIT

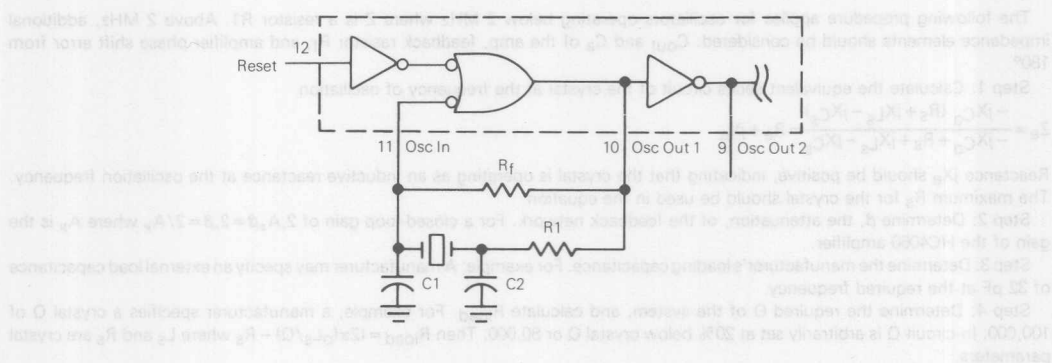
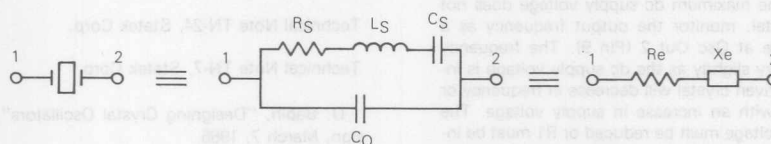


TABLE 1 — CRYSTAL OSCILLATOR
AMPLIFIER SPECIFICATIONS
 $T_A = 25^\circ\text{C}$ (Input = Pin 11, Output = Pin 10)

Type	Positive Reactance (Pierce)
Input Resistance, R_{in}	60 M Ω minimum
Output Impedance, Z_{out} (4.5 V supply)	200 Ω (see text)
Input Capacitance, C_{in}	5 pF typical
Output Capacitance, C_{out}	7 pF typical
Series Capacitance, C_a	5 pF typical
Open loop voltage gain with output at full swing, α	<div> <div>3 Vdc supply</div> <div>4 Vdc supply</div> <div>5 Vdc supply</div> <div>6 Vdc supply</div> </div> <div> <div>5.0 expected minimum</div> <div>4.0 expected minimum</div> <div>3.3 expected minimum</div> <div>3.1 expected minimum</div> </div>

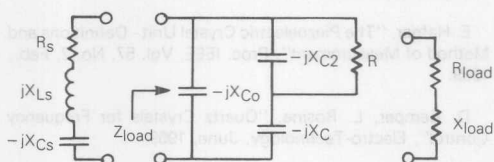
PIERCE CRYSTAL OSCILLATOR DESIGN

FIGURE 7 — EQUIVALENT CRYSTAL NETWORKS



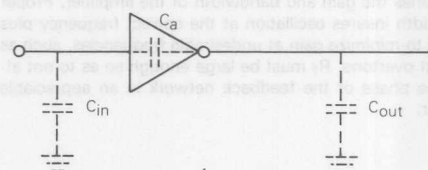
Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE 8 — SERIES EQUIVALENT CRYSTAL LOAD



NOTE: $C = C_1 + C_{in}$ and $R = R_1 + R_{out}$. C_0 is considered as part of the load. C_a and R_f typically have minimal effect below 2 MHz.

FIGURE 9 — PARASITIC CAPACITANCES OF THE AMPLIFIER



Values are listed in Table 1.

DESIGN PROCEDURES

The following procedure applies for oscillators operating below 2 MHz where Z is a resistor R1. Above 2 MHz, additional impedance elements should be considered: C_{OUT} and C_a of the amp, feedback resistor R_f, and amplifier phase shift error from 180°.

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{C_0}(R_s + jX_{L_s} - jX_{C_s})}{-jX_{C_0} + R_s + jX_{L_s} - jX_{C_s}} = R_e + jX_e$$

Reactance jX_e should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R_s for the crystal should be used in the equation.

Step 2: Determine β, the attenuation, of the feedback network. For a closed-loop gain of 2, A_vβ = 2, β = 2/A_v where A_v is the gain of the HC4060 amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: A manufacturer may specify an external load capacitance of 32 pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R_{load}. For example, a manufacturer specifies a crystal Q of 100,000. In-circuit Q is arbitrarily set at 20% below crystal Q or 80,000. Then R_{load} = (2πf₀L_s/Q) - R_s where L_s and R_s are crystal parameters.

Step 5: Simultaneously solve, using a computer,

$$\beta = \frac{X_C \cdot X_{C2}}{R \cdot R_e + X_{C2}(X_e - X_C)} \quad (\text{with feedback phase shift} = 180^\circ) \quad (1)$$

$$X_e = X_{C2} + X_C + \frac{R_e X_{C2}}{R} = X_{C_{load}} \quad (\text{where the loading capacitor is an external load, not including } C_0) \quad (2)$$

$$R_{load} = \frac{RX_{C_0}X_{C2}[(X_C + X_{C2})(X_C + X_{C_0}) - X_C(X_C + X_{C_0} + X_{C2})]}{X_{C2}^2(X_C + X_{C_0})^2 + R^2(X_C + X_{C_0} + X_{C2})^2} \quad (3)$$

Here R = R_{OUT} + R1. R_{OUT} is amp output resistance, R1 is Z. The C corresponding to X_C is given by C = C1 + C_{in}.

Alternately, pick a value for R1 (i.e. let R1 = R_s). Solve Equations 1 and 2 for C1 and C2. Use Equation 3 and the fact that Q = 2πf₀L_s/(R_s + R_{load}) to find in-circuit Q. If Q is not satisfactory pick another value for R1 and repeat the procedure.

CHOOSING R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

SELECTING R_f

The feedback resistor, R_f, typically ranges up to 20 MΩ. R_f determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone. R_f must be large enough so as to not affect the phase of the feedback network in an appreciable manner.

ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

ALSO RECOMMENDED FOR READING:

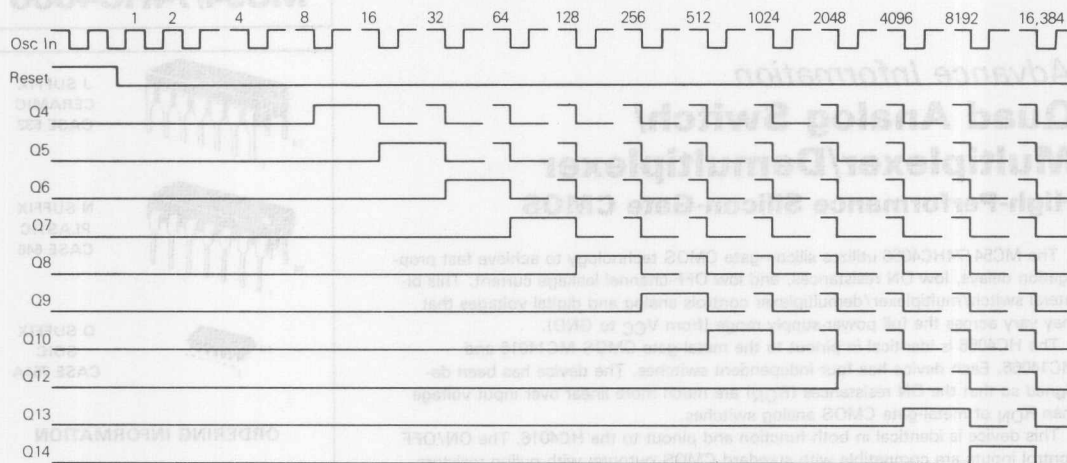
E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

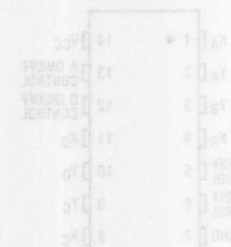
MC54/74HC4060

TIMING DIAGRAM



MC54/74HC4060
MC54/74HC4060
MC54/74HC4060

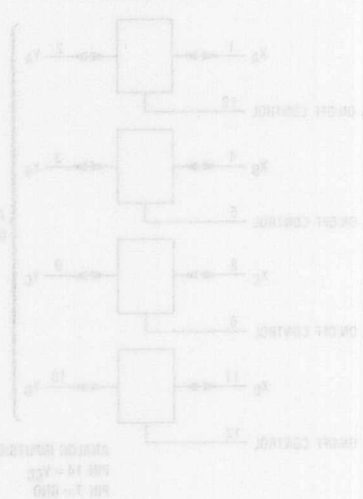
PIN ASSIGNMENT



FUNCTION TABLE

On/Off Control	State of Analog Switch
1	On
0	Off

LOGIC DIAGRAM



Advance Information

Quad Analog Switch/ Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

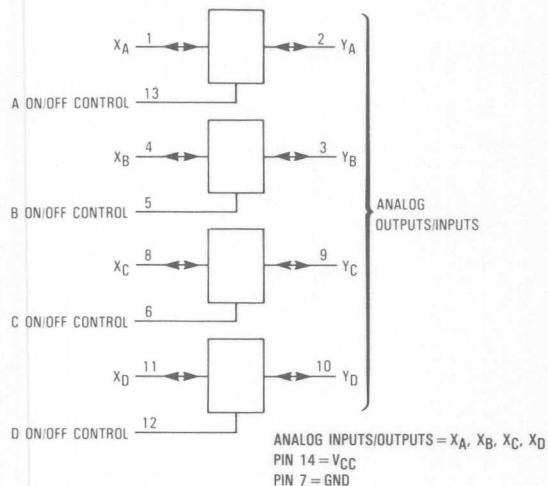
The MC54/74HC4066 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The HC4066 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

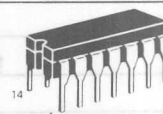
This device is identical in both function and pinout to the HC4016. The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 12.0 Volts
- Analog Input Voltage Range ($V_{CC} - GND$) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066 or HC4016
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates

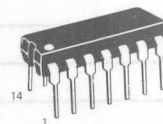
LOGIC DIAGRAM



MC54/74HC4066



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



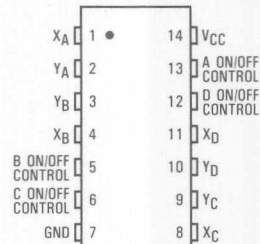
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC4066

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage (Referenced to GND)	-0.5 to +14.0	V
V _{IS}	Analog Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{in}	Digital Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
I	DC Current Into or Out of Any Pin	±25	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V
V _{IS}	Analog Input Voltage (Referenced to GND)	GND	V _{CC}	V
V _{in}	Digital Input Voltage (Referenced to GND)	GND	V _{CC}	V
V _{IO} *	Static or Dynamic Voltage Across Switch	—	1.2	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)			ns
	V _{CC} = 2.0 V	0	1000	
	V _{CC} = 4.5 V	0	500	
	V _{CC} = 9.0 V	0	400	
	V _{CC} = 12.0 V	0	250	

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Voltage ON/OFF Control Inputs	R _{on} = Per Spec	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			9.0	6.3	6.3	6.3	
			12.0	8.4	8.4	8.4	
V _{IL}	Maximum Low-Level Voltage ON/OFF Control Inputs	R _{on} = Per Spec	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			9.0	1.8	1.8	1.8	
			12.0	2.4	2.4	2.4	
I _{in}	Maximum Input Leakage Current, ON/OFF Control Inputs	V _{in} = V _{CC} or GND	12.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND V _{IO} = 0 V	6.0	2	20	40	μA
			12.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4066

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
R _{on}	Maximum "ON" Resistance	V _{in} = V _{IH} V _{IS} = V _{CC} to GND I _S ≤ 2.0 mA (Figures 1, 2)	2.0†	—	—	—	Ω
			4.5	170	215	255	
			9.0	85	106	130	
			12.0	85	106	130	
		V _{in} = V _{IH} V _{IS} = V _{CC} or GND (Endpoints) I _S ≤ 2.0 mA (Figures 1, 2)	2.0	—	—	—	
			4.5	85	106	130	
			9.0	63	78	95	
			12.0	63	78	95	
ΔR _{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V _{in} = V _{IH} V _{IS} = 1/2 (V _{CC} - GND) I _S ≤ 2.0 mA	2.0	—	—	—	Ω
			4.5	30	35	40	
			9.0	20	25	30	
			12.0	20	25	30	
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel	V _{in} = V _{IL} V _{IO} = V _{CC} or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I _{on}	Maximum On-Channel Leakage Current, Any One Channel	V _{in} = V _{IH} V _{IS} = V _{CC} or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V_{CC} - V_{EE}) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, ON/OFF Control Inputs: t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0	50	65	75	ns
		4.5	10	13	15	
		9.0	10	13	15	
		12.0	10	13	15	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	150	190	225	ns
		4.5	30	38	45	
		9.0	30	30	30	
		12.0	30	30	30	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	125	160	185	ns
		4.5	25	32	37	
		9.0	25	32	37	
		12.0	25	32	37	
C	Maximum Capacitance	ON/OFF Control Input	—	10	10	pF
		Control Input = GND	—	—	—	
		Analog I/O Feedthrough	—	35 1.0	35 1.0	

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13) Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		15	

MC54/74HC4066

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V _{CC} V	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f _{in} = 1 MHz Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{OS} Increase f _{in} Frequency Until dB Meter Reads -3 dB R _L = 50 Ω, C _L = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off-Channel Feedthrough Isolation (Figure 6)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	-50 -50 -50 -40 -40 -40	dB
—	Feedthrough Noise, Control to Switch (Figure 7)	V _{in} ≤ 1 MHz Square Wave (t _r = t _f = 6 ns) Adjust R _L at Setup so that I _S = 0 A R _L = 600 Ω, C _L = 50 pF R _L = 10 kΩ, C _L = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	60 130 200 30 65 100	mVpp
—	Crosstalk Between Any Two Switches (Figure 12)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	4.5 9.0 12.0 4.5 9.0 12.0	-70 -70 -70 -80 -80 -80	dB
THD	Total Harmonic Distortion (Figure 14)	f _{in} = 1 kHz, R _L = 10 kΩ, C _L = 50 pF THD = THD _{Measured} - THD _{Source} V _{IS} = 4.0 Vpp sine wave V _{IS} = 8.0 Vpp sine wave V _{IS} = 11.0 Vpp sine wave	4.5 9.0 12.0	0.10 0.06 0.04	%

*Guaranteed limits not tested. Determined by design and verified by qualification.

MC54/74HC4066

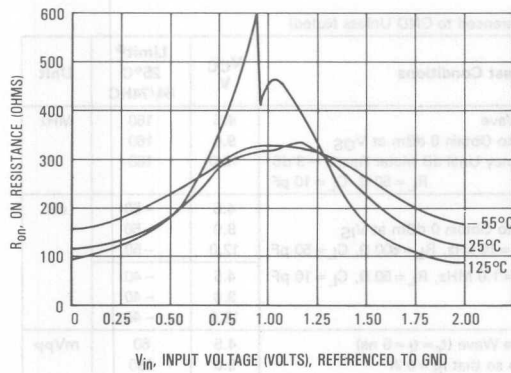


Figure 1a. Typical On Resistance, $V_{CC} = 2.0$ V

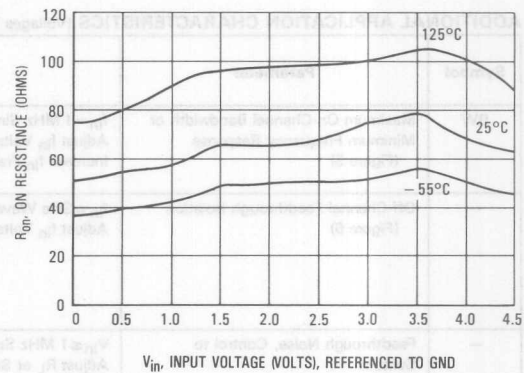


Figure 1b. Typical On Resistance, $V_{CC} = 4.5$ V

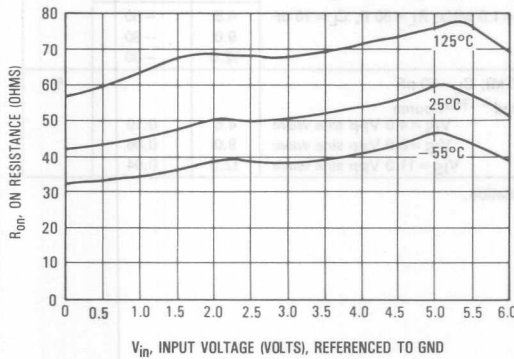


Figure 1c. Typical On Resistance, $V_{CC} = 6.0$ V

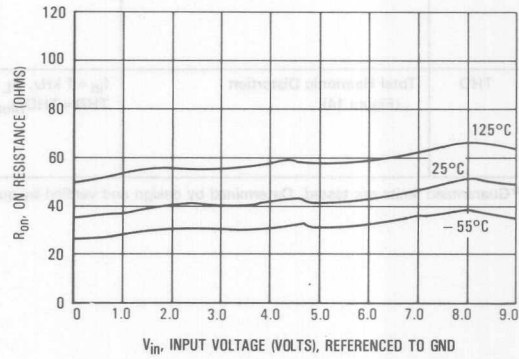


Figure 1d. Typical On Resistance, $V_{CC} = 9.0$ V

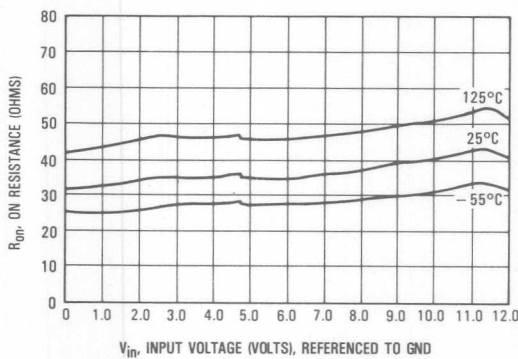


Figure 1e. Typical On Resistance, $V_{CC} = 12.0$ V

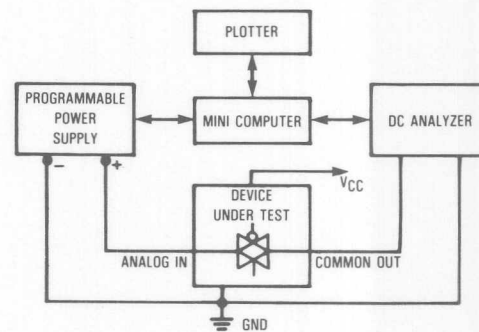


Figure 2. On Resistance Test Set-Up

5

MC54/74HC4066

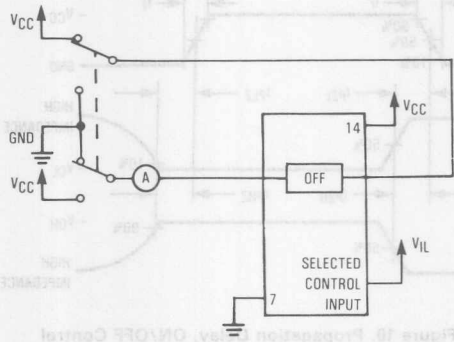


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

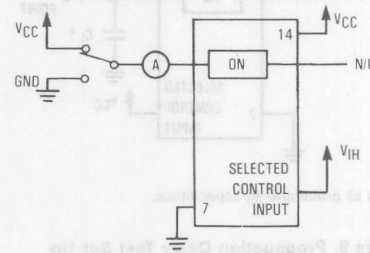
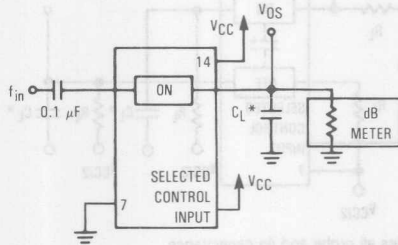
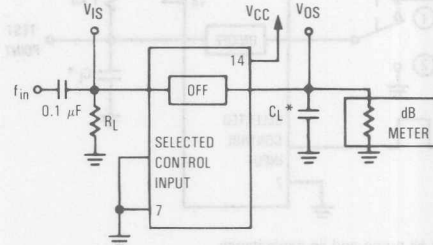


Figure 4. Maximum On Channel Leakage Current, Test Set-Up



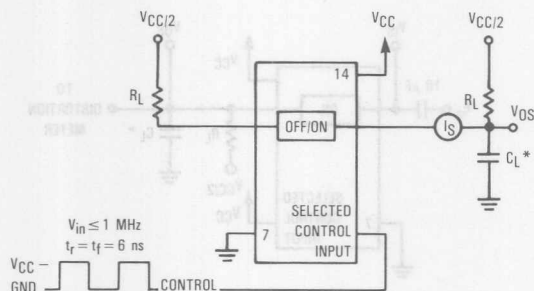
*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth Test Set-Up



*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

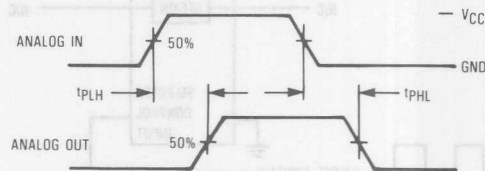
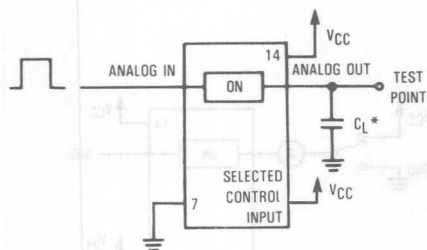


Figure 8. Propagation Delays, Analog In to Analog Out

MC54/74HC4066



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

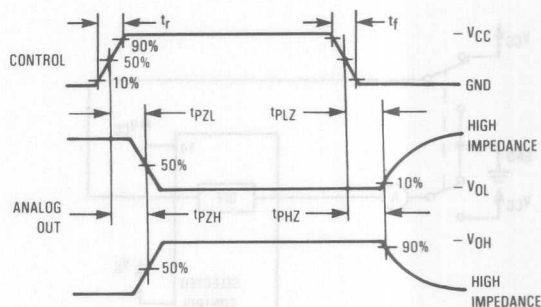
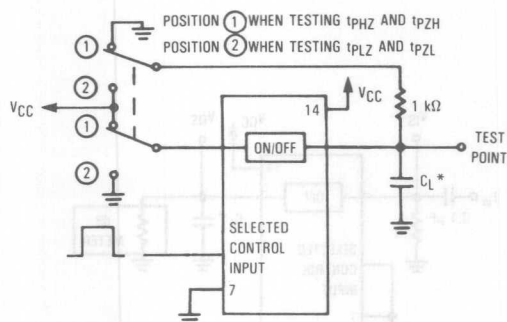
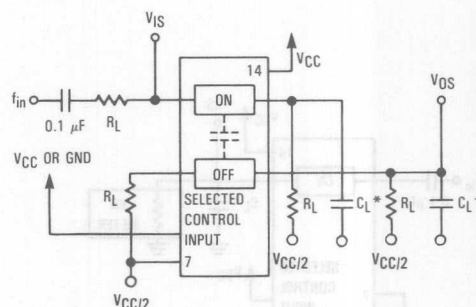


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

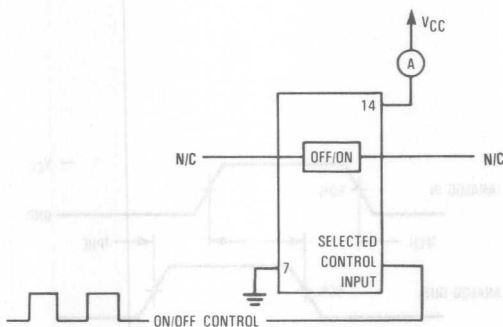
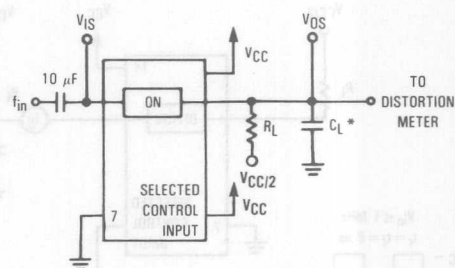


Figure 13. Power Dissipation Capacitance Test Set-Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

MC54/74HC4066

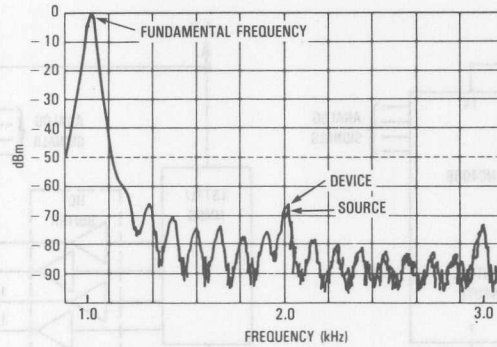


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked-up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below GND. In the example below,

the difference between V_{CC} and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the D_x diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear out mechanism.

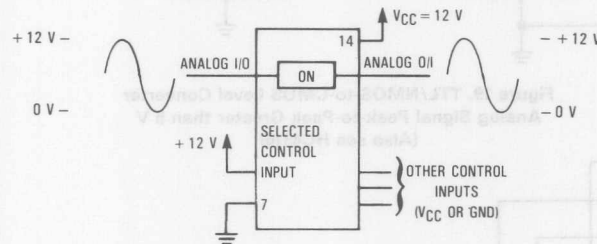


Figure 16. 12 V Application

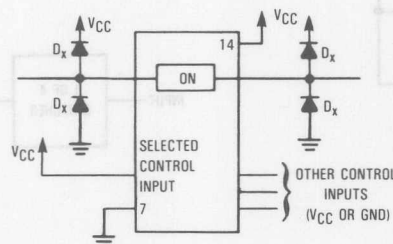


Figure 17. Transient Suppressor Application

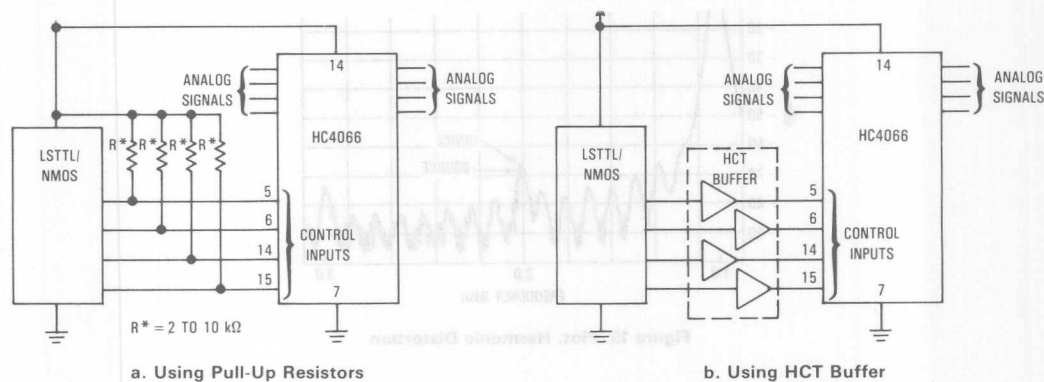


Figure 18. LSTTL/NMOS to HCMOS Interface

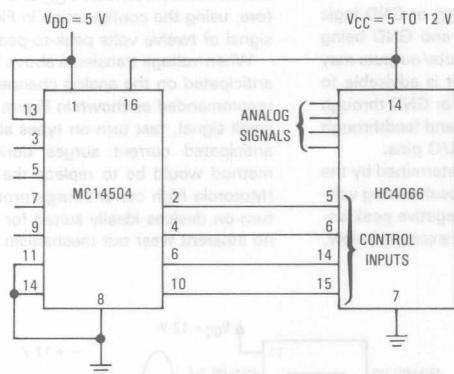


Figure 19. TTL/NMOS-to-CMOS Level Converter
Analog Signal Peak-to-Peak Greater than 5 V
(Also see HC4316)

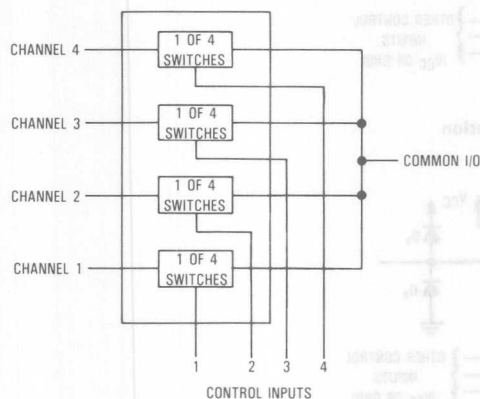


Figure 20. 4-Input Multiplexer

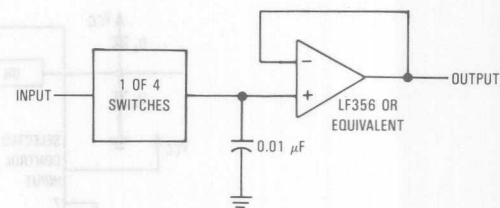


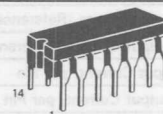
Figure 21. Sample/Hold Amplifier

MC54/74HC4075

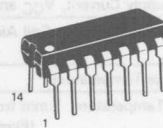
Triple 3-Input OR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC4075 is identical in pinout to the MC14075B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



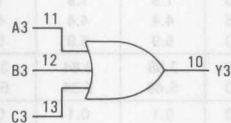
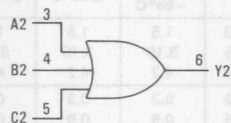
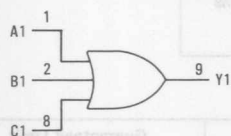
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

$$Y = A + B + C$$

PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	C3
A2	3	12	B3
B2	4	11	A3
C2	5	10	Y3
Y2	6	9	Y1
GND	7	8	C1

FUNCTION TABLE

Inputs			Output
A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} ,V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 1 and 2)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		26	

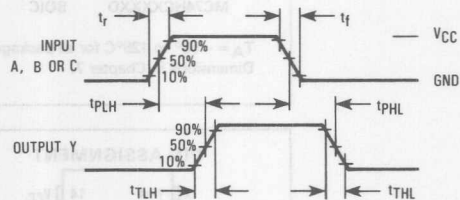
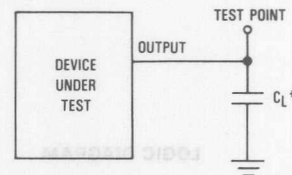
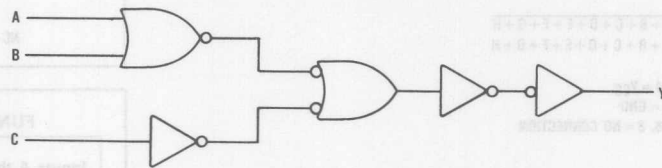


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

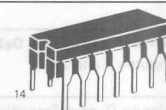
EXPANDED LOGIC DIAGRAM
(1/4 of the Device)

MC54/74HC4078

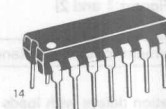
8-Input NOR/OR Gate High-Performance Silicon-Gate CMOS

The MC54/74HC4078 is similar to the CD4078B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 30 FETs or 7.5 Equivalent Gates



J SUFFIX
 CERAMIC
 CASE 632



N SUFFIX
 PLASTIC
 CASE 646



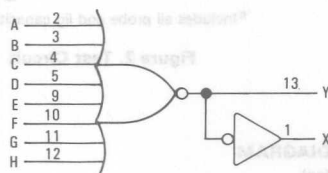
D SUFFIX
 SOIC
 CASE 751A

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 7.

LOGIC DIAGRAM



$$Y = A + B + C + D + E + F + G + H$$

$$X = A + B + C + D + E + F + G + H$$

PIN 14 = V_{CC}
 PIN 7 = GND
 PINS 6, 8 = NO CONNECTION

PIN ASSIGNMENT

X	1	14	V_{CC}
A	2	13	Y
B	3	12	H
C	4	11	G
D	5	10	F
NC	6	9	E
GND	7	8	NC

NC = NO CONNECTION

FUNCTION TABLE

Inputs A through H	Outputs	
	Y	X
All inputs L	H	L
All other combinations	L	H

MC54/74HC4078

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400 ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4078

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Any Input to Output Y (Figures 1 and 3)	2.0 4.5 6.0	130 26 22	165 33 28	195 39 33	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Any Input to Output X (Figures 2 and 3)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1, 2, and 3)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = CPD \cdot V_{CC}^2 f + I_{CC} \cdot V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		29	

SWITCHING WAVEFORMS

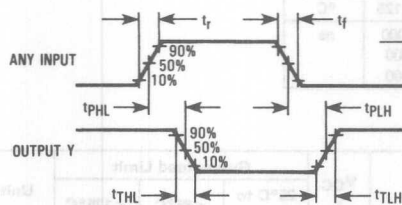


Figure 1

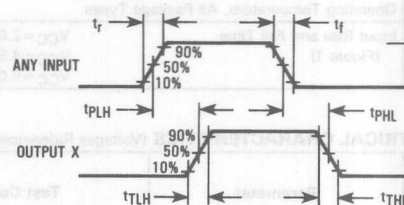
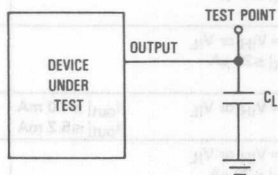


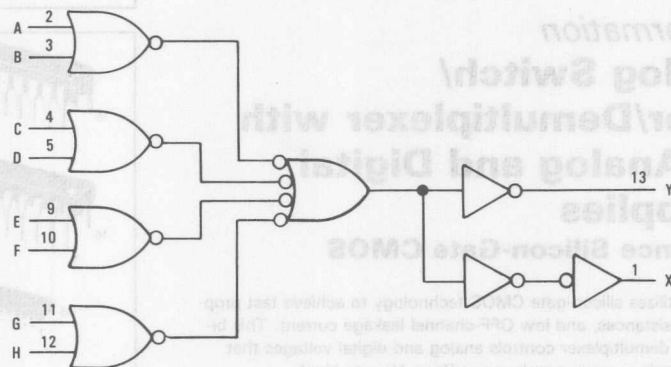
Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit

EXPANDED LOGIC DIAGRAM



The diagram shows a 4-to-1 multiplexer with four data inputs (A, B, C, D) and two select inputs (S0, S1). The output of the multiplexer is connected to a 13-bit bus labeled '13' and 'Y'. The bus is connected to a 13-bit register, which is represented by a triangle with a circle at its output. The register has a feedback loop from its output back to its input. The output of the register is also connected to a 13-bit bus labeled '13' and 'Y'.

MC54/74HC4316

Advance Information

Quad Analog Switch/ Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies

High-Performance Silicon-Gate CMOS

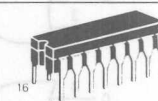
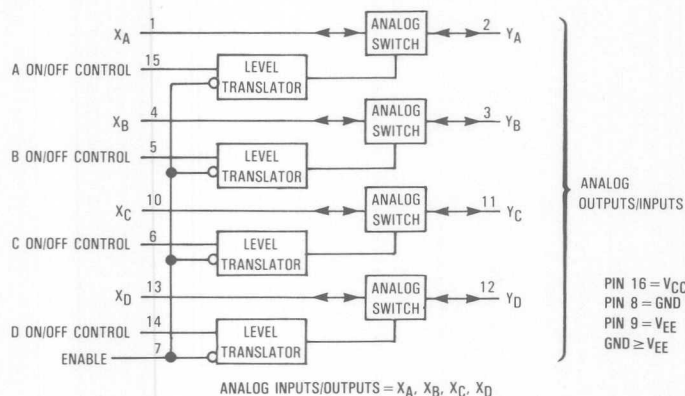
The MC54/74HC4316 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full analog power-supply range (from V_{CC} to V_{EE}).

The HC4316 is similar in function to the metal-gate CMOS MC14016 and MC14066, and to the High-Speed CMOS HC4016 and HC4066. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal-gate CMOS analog switches. Logic-level translators are provided so that the On/Off Control and Enable logic-level voltages need only be V_{CC} and GND, while the switch is passing signals ranging between V_{CC} and V_{EE} . When the Enable pin (active-low) is high, all four analog switches are turned off.

- Logic-Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power-Supply Voltage Range ($V_{CC} - V_{EE}$) = 2.0 to 12.0 Volts
- Digital (Control) Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 6.0 Volts, Independent of V_{EE}
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates

5

BLOCK DIAGRAM



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



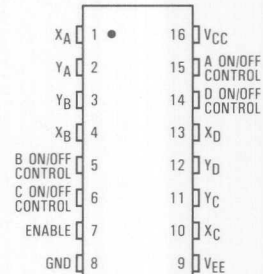
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		State of Analog Switch
Enable	On/Off Control	
L	H	On
L	L	Off
H	X	Off

X = don't care

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC4316

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V _{EE})	-0.5 to +7.0 -0.5 to +14.0	V
V _{EE}	Negative DC Supply Voltage (Ref. to GND)	-7.0 to +0.5	V
V _{IS}	Analog Input Voltage	V _{EE} - 0.5 to V _{CC} + 0.5	V
V _{in}	Digital Input Voltage (Ref. to GND)	-1.5 to V _{CC} + 1.5	V
I	DC Current Into or Out of Any Pin	±25	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage (Ref. to GND)	2.0	6.0	V
V _{EE}	Negative DC Supply Voltage (Ref. to GND)	-6.0	GND	V
V _{IS}	Analog Input Voltage	V _{EE}	V _{CC}	V
V _{in}	Digital Input Voltage (Ref. to GND)	GND	V _{CC}	V
V _{IO} *	Static or Dynamic Voltage Across Switch	—	1.2	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Control or Enable Inputs) (Figure 10)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND Except Where Noted

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Voltage, Control or Enable Inputs	R _{on} = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Voltage, Control or Enable Inputs	R _{on} = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
I _{in}	Maximum Input Leakage Current, Control or Enable Inputs	V _{in} = V _{CC} or GND V _{EE} = -6.0 V	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND V _{IO} = 0 V	V _{EE} = GND V _{EE} = -6.0	6.0 6.0	2 8	20 80	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4316

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to V_{EE})

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					25°C to -55°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to V_{EE} $I_S \leq 2.0$ mA (Figures 1, 2)	2.0*	0.0	—	—	—	Ω
			4.5	0.0	320	400	480	
			4.5	-4.5	170	215	255	
			6.0	-6.0	170	215	255	
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Endpoints) $I_S \leq 2.0$ mA (Figures 1, 2)	2.0	0.0	—	—	—	
			4.5	0.0	180	225	270	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ $V_{IS} = 1/2 (V_{CC} - V_{EE})$ $I_S \leq 2.0$ mA	2.0	0.0	—	—	—	Ω
			4.5	0.0	30	35	40	
			4.5	-4.5	20	25	30	
			6.0	-6.0	20	25	30	
I_{off}	Maximum Off-Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or V_{EE} Switch Off (Figure 3)	6.0	-6.0	0.1	0.5	1.0	μA
I_{on}	Maximum On-Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Figure 4)	6.0	-6.0	0.1	0.5	1.0	μA

*At supply voltage ($V_{CC} - V_{EE}$) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Control or Enable: $t_r = t_f = 6$ ns, $V_{EE} = GND$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t_{pZL} , t_{pZH}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0	265	335	400	ns
		4.5	53	66	80	
		6.0	45	56	68	
C	Maximum Capacitance	ON/OFF Control and Enable Inputs	—	10	10	pF
		Control Input = GND	—	—	—	
		Analog I/O Feedthrough	—	35	35	
			1.0	1.0	1.0	

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

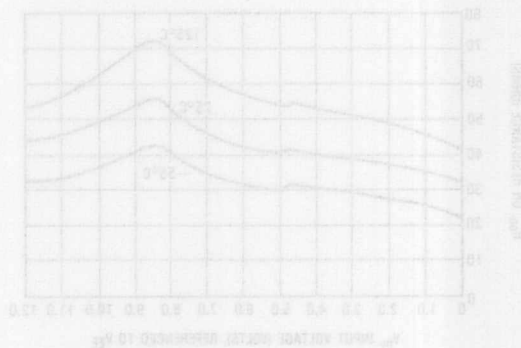
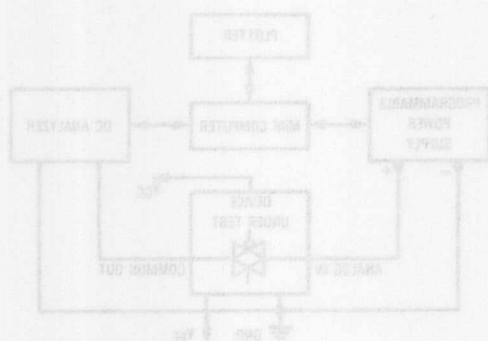
CPD	Power Dissipation Capacitance (Per Switch) (Figure 13) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V		pF
		15		

MC54/74HC4316

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Limit* 25°C	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f _{in} = 1 MHz Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} Increase f _{in} Frequency Until dB Meter Reads -3 dB R _L = 50 Ω, C _L = 10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	150 160 160	MHz
—	Off-Channel Feedthrough Isolation (Figure 6)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	-50 -50 -50 -40 -40 -40	dB
—	Feedthrough Noise, Control to Switch (Figure 7)	V _{in} ≤ 1 MHz Square Wave (t _r = t _f = 6 ns) Adjust R _L at Setup so that I _S = 0 A R _L = 600 Ω, C _L = 50 pF R _L = 10 kΩ, C _L = 10 pF	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	60 130 200 30 65 100	mVpp
—	Crosstalk Between Any Two Switches (Figure 12)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	2.25 4.50 6.00 2.25 4.50 6.00	-2.25 -4.50 -6.00 -2.25 -4.50 -6.00	-70 -70 -70 -80 -80 -80	dB
THD	Total Harmonic Distortion (Figure 14)	f _{in} = 1 kHz, R _L = 10 kΩ, C _L = 50 pF THD = THD _{Measured} - THD _{Source} V _{IS} = 4.0 Vpp sine wave V _{IS} = 8.0 Vpp sine wave V _{IS} = 11.0 Vpp sine wave	2.25 4.50 6.00	-2.25 -4.50 -6.00	0.10 0.06 0.04	%

*Limits not tested. Determined by design and verified by qualification.



MC54/74HC4316

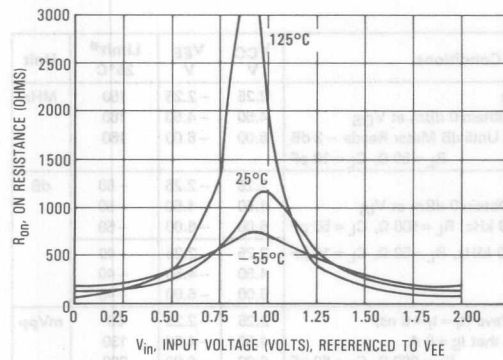


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE} = 2.0$ V

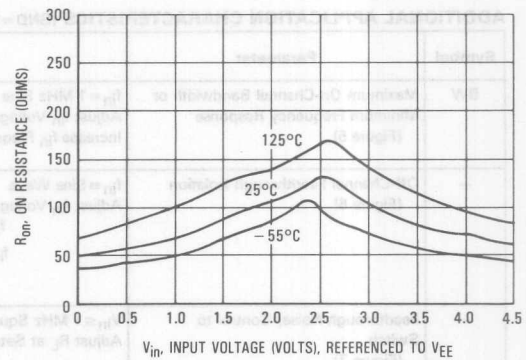


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE} = 4.5$ V

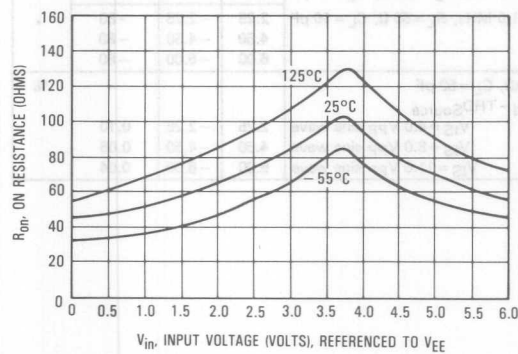


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 6.0$ V

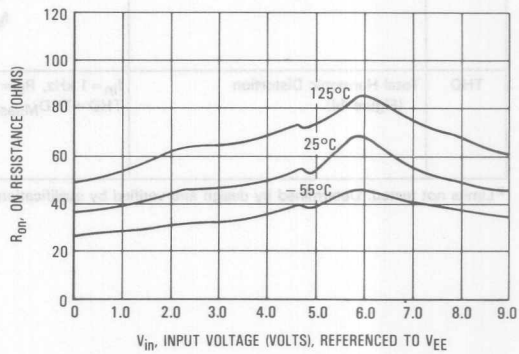


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 9.0$ V

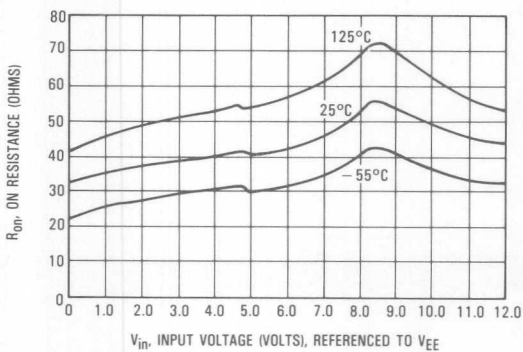


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE} = 12.0$ V

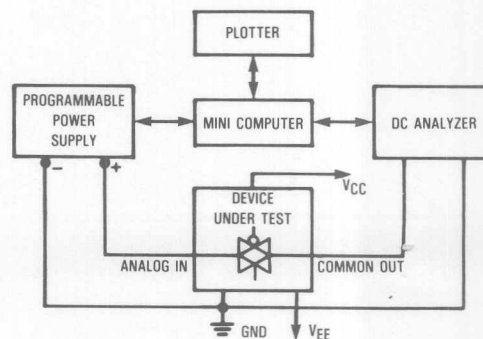


Figure 2. On Resistance Test Set-Up

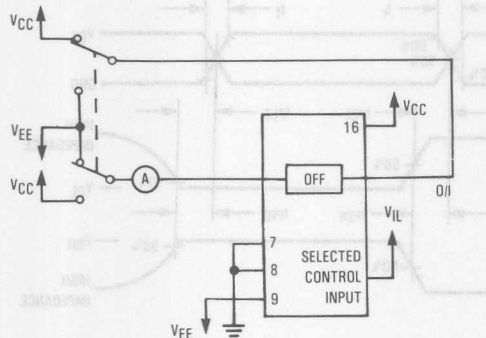


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

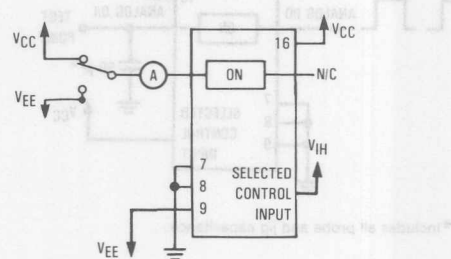
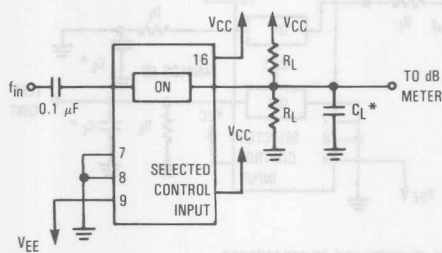
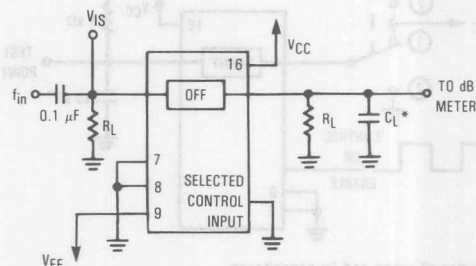


Figure 4. Maximum On Channel Leakage Current, Test Set-Up



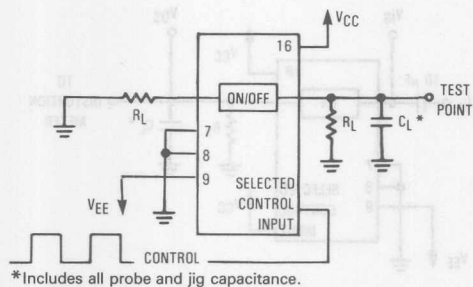
*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth Test Set-Up



*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, Control to Analog Out, Test Set-Up

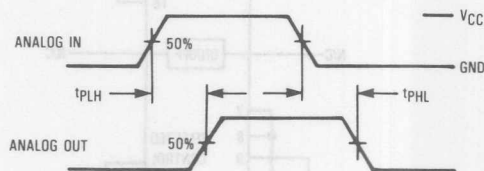
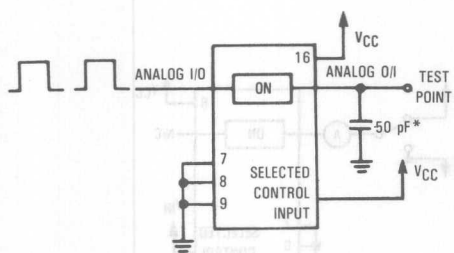


Figure 8. Propagation Delays, Analog in to Analog Out

MC54/74HC4316



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

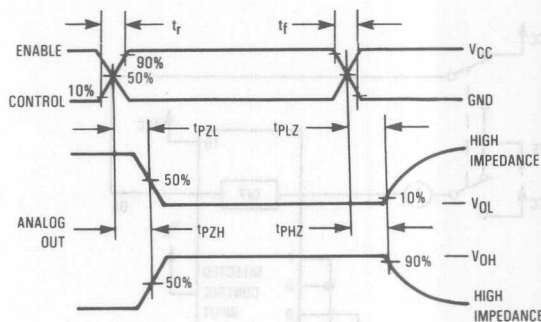
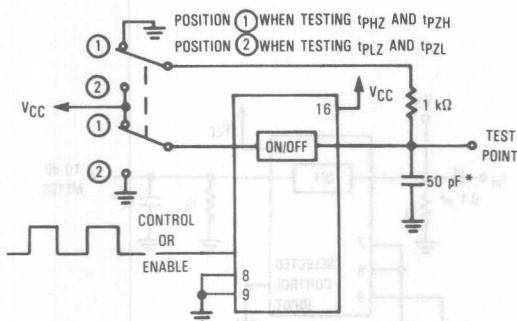
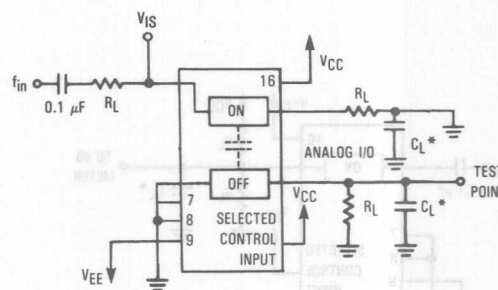


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up (Adjacent Channels Used)

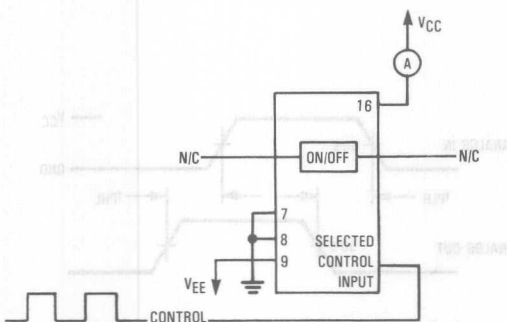
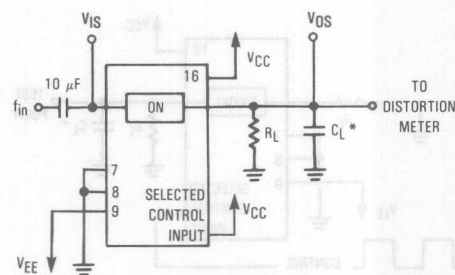


Figure 13. Power Dissipation Capacitance Test Set-Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

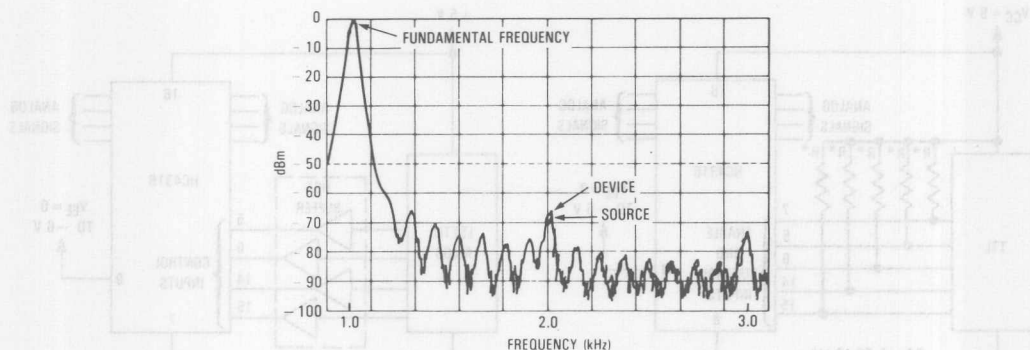


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The Enable and Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or V_{EE} through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below V_{EE} . In the example below,

the difference between V_{CC} and V_{EE} is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the D_x diodes with MO*sorbs (Motorola high current surge protectors). MO*sorbs are fast turn-on devices ideally suited for precise dc protection with no inherent wear out mechanism.

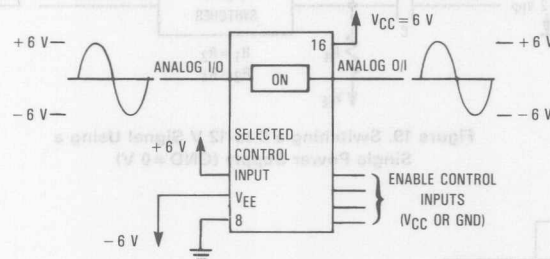


Figure 16

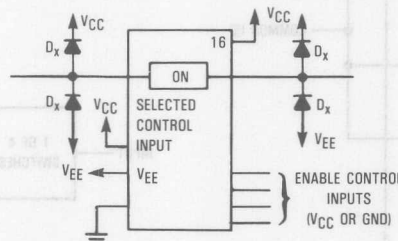


Figure 17. Transient Suppressor Application

MC54/74HC4316

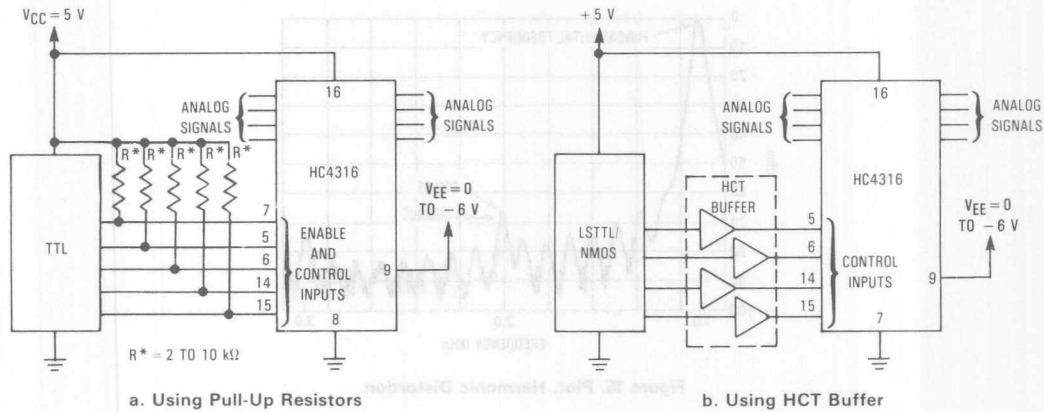


Figure 18. LSTTL/NMOS to HCMOS Interface

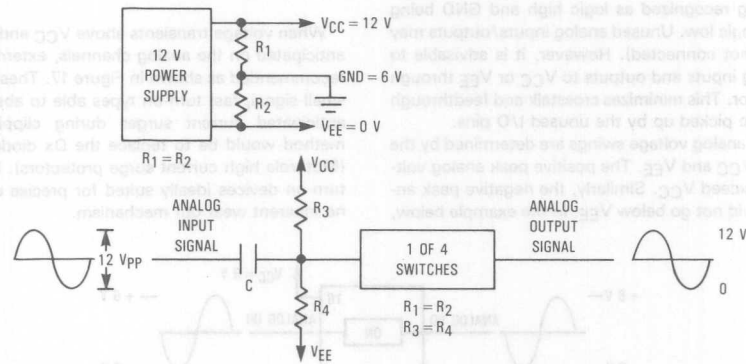


Figure 19. Switching a 0-to-12 V Signal Using a Single Power Supply ($GND \neq 0V$)

5

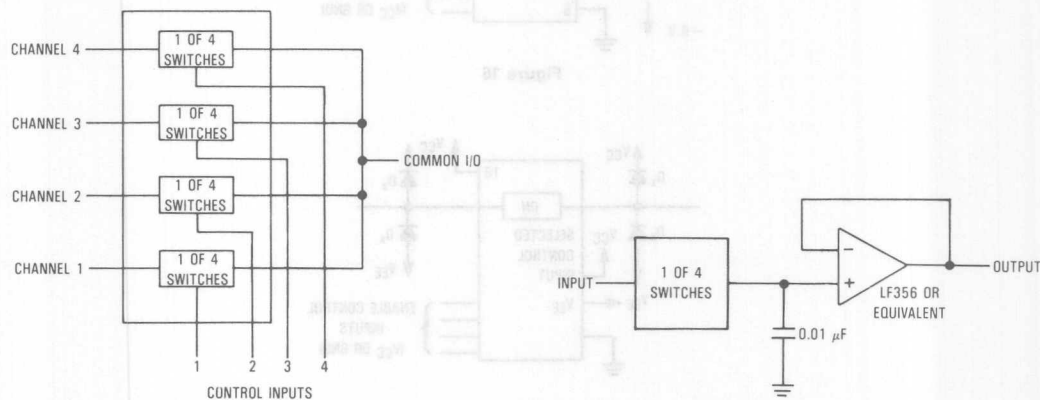


Figure 20. 4-Input Multiplexer

Figure 21. Sample/Hold Amplifier

Advance Information

Analog Multiplexers/ Demultiplexers with Address Latch

High-Performance Silicon-Gate CMOS

The MC54/74HC4351, MC54/74HC4352, and MC54/74HC4353 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. The data at the Channel-Select inputs may be latched by using the active-low Latch Enable pin. When Latch Enable is high, the latch is transparent. When either Enable 1 (active low) or Enable 2 (active high) is inactive, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

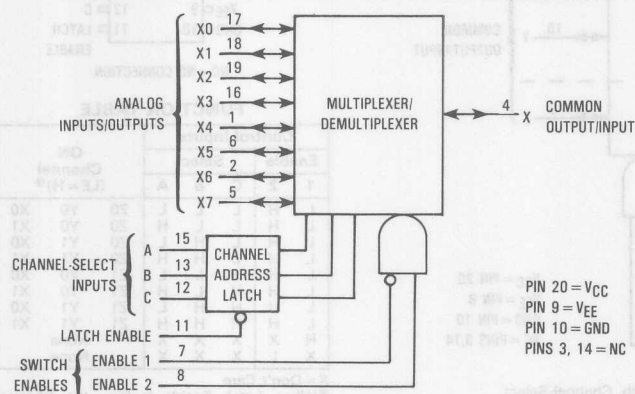
These devices have been designed so that the ON resistance (R_{ON}) is more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

For multiplexers/demultiplexers without latches, see the HC4051, HC4052, and HC4053.

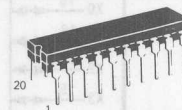
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC} - GND$) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance than Metal-Gate Types
- Low Noise
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: HC4351—222 FETs or 55.5 Equivalent Gates
HC4352—188 FETs or 47 Equivalent Gates
HC4353—186 FETs or 46.5 Equivalent Gates

BLOCK DIAGRAM
MC54/74HC4351

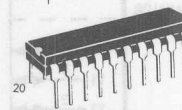
Single-Pole, 8-Position Plus Common Off and Address Latch



MC54/74HC4351 MC54/74HC4352 MC54/74HC4353



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



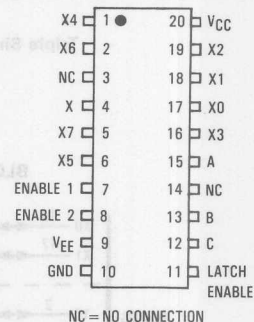
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXXN Plastic
MC54HCXXXXJ Ceramic
MC74HCXXXXDW SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT MC54/74HC4351



FUNCTION TABLE MC54/74HC4351

Control Inputs					ON Channel (LE = H)*
Enable		Select			
1	2	C	B	A	
L	H	L	L	L	X0
L	H	L	L	H	X1
L	H	L	H	L	X2
L	H	L	H	H	X3
L	H	H	L	L	X4
L	H	H	L	H	X5
L	H	H	H	L	X6
L	H	H	H	H	X7
H	X	X	X	X	None
X	L	X	X	X	None

X = don't care

*When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

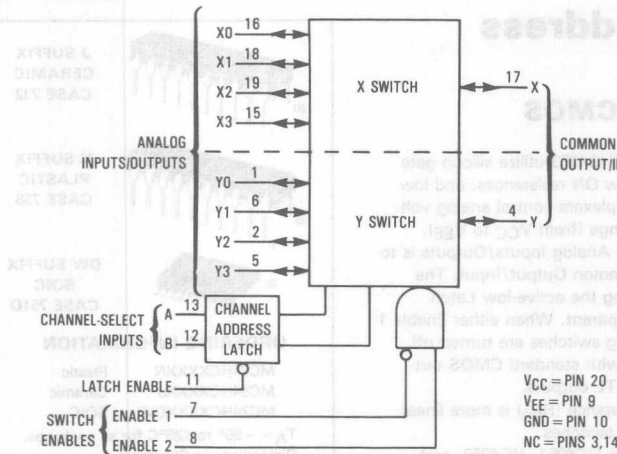
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC4351•MC54/74HC4352•MC54/74HC4353

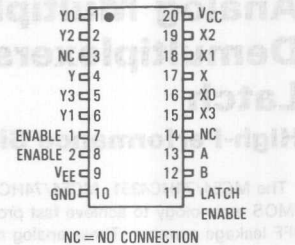
MC54/74HC4352

Double-Pole, 4-Position Plus Common Off and Address Latch

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs				ON Channel (LE = H)*	
Enable		Select			
1	2	B	A		
L	H	L	L	Y0	X0
L	H	L	H	Y1	X1
L	H	H	L	Y2	X2
L	H	H	H	Y3	X3
H	X	X	X	None	
X	L	X	X	None	

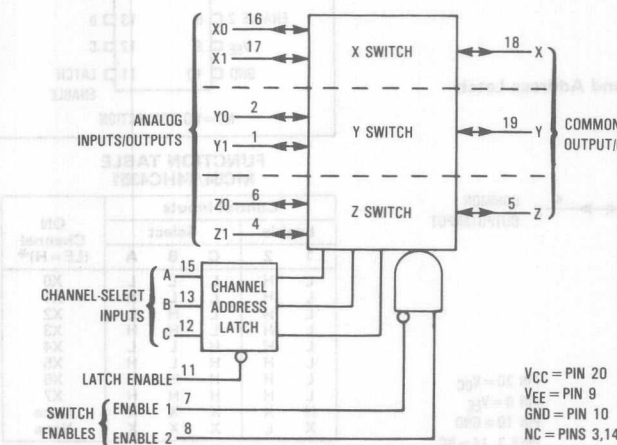
X = Don't Care

*When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

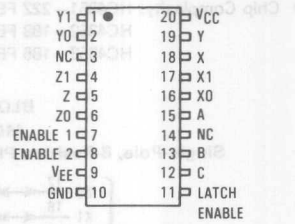
MC54/74HC4353

Triple Single-Pole, Double-Position Plus Common Off and Address Latch

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs					ON Channel (LE = H)*
Enable		Select			
1	2	C	B	A	
L	H	L	L	L	Z0 Y0 X0
L	H	L	L	H	Z0 Y0 X1
L	H	L	H	L	Z0 Y1 X0
L	H	L	H	H	Z0 Y1 X1
L	H	H	L	L	Z1 Y0 X0
L	H	H	L	H	Z1 Y0 X1
L	H	H	H	L	Z1 Y1 X0
L	H	H	H	H	Z1 Y1 X1
H	X	X	X	X	None
X	L	X	X	X	None

X = Don't Care

*When Latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change states.

NOTE:
This device allows independent control of each switch. Channel-Select Input A controls the X Switch, Input B controls the Y Switch, and Input C controls the Z Switch.

MC54/74HC4351•MC54/74HC4352•MC54/74HC4353

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V _{EE})	−0.5 to +7.0 −0.5 to 14.0	V
V _{EE}	Negative DC Supply Voltage (Ref. to GND)	−7.0 to +0.5	V
V _{IS}	Analog Input Voltage	V _{EE} − 0.5 to V _{CC} + 0.5	V
V _{in}	Digital Input Voltage (Ref. to GND)	−1.5 to V _{CC} + 1.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P _D	Power Dissipation in Still Air Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Power Dissipation Temperature Derating:

Plastic "N" Package: −10 mW/°C from 65° to 85°C
Ceramic "J" Package: −10 mW/°C from 100° to 125°C
SOIC "D" Package: −7 mW/°C from 65° to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the ranges indicated in the Recommended Operating Conditions.

Unused digital input pins must be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated. See Applications Information.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V _{EE})	2.0 2.0	6.0 12.0	V
V _{EE}	Negative DC Supply Voltage (Ref. to GND)	−6.0	GND	V
V _{IS}	Analog Input Voltage	V _{EE}	V _{CC}	V
V _{in}	Digital Input Voltage (Ref. to GND)	GND	V _{CC}	V
V _{IO} *	Static or Dynamic Voltage Across Switch	—	1.2	V
T _A	Operating Temperature, All Package Types	−55	+125	°C
t _r , t _f	Input Rise and Fall Time, V _{CC} = 2.0 V Channel Select or Enable V _{CC} = 4.5 V Inputs (Figure 9a) V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R _{on} = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	R _{on} = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
I _{in}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V _{in} = V _{CC} or GND, V _{EE} = −6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V _{CC} or GND Enables = V _{CC} or GND V _{IS} = V _{CC} or GND V _{IO} = 0 V					μA
		V _{EE} = GND	6.0	2	20	40	
		V _{EE} = −6.0	6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4351•MC54/74HC4352•MC54/74HC4353

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Guaranteed Limit			Unit
					25°C to -55°C	≤85°C	≤125°C	
R _{on}	Maximum "ON" Resistance	V _{in} = V _{IL} or V _{IH} V _{IS} = V _{CC} to V _{EE} I _S ≤ 2.0 mA (Figures 1, 2)	4.5	0.0	190	240	280	Ω
			4.5	-4.5	120	150	170	
			6.0	-6.0	100	125	140	
		V _{in} = V _{IL} or V _{IH} V _{IS} = V _{CC} or V _{EE} (Endpoints) I _S ≤ 2.0 mA (Figures 1, 2)	4.5	0.0	150	190	230	Ω
			4.5	-4.5	100	125	140	
			6.0	-6.0	80	100	115	
ΔR _{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V _{in} = V _{IL} or V _{IH} V _{IS} = 1/2 (V _{CC} - V _{EE}) I _S ≤ 2.0 mA	4.5	0.0	30	35	40	Ω
			4.5	-4.5	12	15	18	
			6.0	-6.0	10	12	14	
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel	V _{in} = V _{IL} or V _{IH} V _{IO} = V _{CC} - V _{EE} Switch Off (Figure 3)	6.0	-6.0	0.1	0.5	1.0	μA
	Maximum Off-Channel Leakage Current, Common Channel	V _{in} = V _{IL} or V _{IH} V _{IO} = V _{CC} - V _{EE} Switch Off (Figure 4)	6.0	-6.0	0.2	2.0	4.0	μA
			6.0	-6.0	0.1	1.0	2.0	
			6.0	-6.0	0.1	1.0	2.0	
I _{on}	Maximum On-Channel Leakage Current, Channel to Channel	V _{in} = V _{IL} or V _{IH} Switch to Switch = V _{CC} - V _{EE} (Figure 5)	6.0	-6.0	0.2	2.0	4.0	μA
			6.0	-6.0	0.1	1.0	2.0	
			6.0	-6.0	0.1	1.0	2.0	
			6.0	-6.0	0.1	1.0	2.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit	
			25°C to −55°C	≤85°C	≤125°C		
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Channel-Select to Analog Output (Figure 9)	2.0 4.5 6.0	370 74 63	465 93 79	550 110 94	ns	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Analog Output (Figure 12)	2.0 4.5 6.0	325 65 55	410 82 70	485 97 82	ns	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)	2.0 4.5 6.0	290 58 49	365 73 62	435 87 74	ns	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Enable 1 or 2 to Analog Output (Figure 11)	2.0 4.5 6.0	345 69 59	435 87 74	515 103 87	ns	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF	
C _{I/O}	Maximum Capacitance	Analog I/O Common O/I: HC4351 HC4352 HC4353 Feedthrough	Enable 1 = V _{IH} , Enable 2 = V _{IL}	—	35	35	pF
			—	130	130	130	
			—	80	80	80	
			—	50	50	50	
—	—	—	1.0	1.0	1.0	—	

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) (Figure 14) Used to determine the no-load dynamic power consumption: P _D = C _{PD} V _{CC} ² f + I _{CC} V _{CC} For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		45 (HC4351) 80 (HC4352) 45 (HC4353)	

MC54/74HC4351•MC54/74HC4352•MC54/74HC4353

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Channel-Select to Latch Enable (Figure 12)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Enable to Channel Select (Figure 12)	2.0	0	0	0	ns
		4.5	0	0	0	
		6.0	0	0	0	
t _w	Minimum Pulse Width, Latch Enable (Figure 12)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times, Channel-Select, Latch Enable, and Enables 1 and 2	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

Symbol	Parameter	Test Condition	V _{CC} V	V _{EE} V	Limit*	Unit
					25°C 54/74HC	
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6)	f _{in} = 1 MHz Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{OIS} Increase f _{in} Frequency Until dB Meter Reads -3 dB R _L = 50 Ω, C _L = 10 pF	2.25	-2.25	80 95 120	MHz
			4.50	-4.50	80 95 120	
			6.00	-6.00	80 95 120	
—	Off-Channel Feedthrough Isolation (Figure 7)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF	2.25	-2.25	-50	dB
			4.50	-4.50	-50	
			6.00	-6.00	-50	
—	Feedthrough Noise, Channel Select Input to Common O/I (Figure 8)	V _{in} ≤ 1 MHz Square Wave (t _r = t _f = 6 ns) Adjust R _L at Setup so that I _S = 0 A Enable = GND R _L = 600 Ω, C _L = 50 pF R _L = 10 kΩ, C _L = 10 pF	2.25	-2.25	25	mVpp
			4.50	-4.50	105	
			6.00	-6.00	135	
—	Crosstalk Between Any Two Switches (Figure 13) (Test does not apply to HC4351)	f _{in} = Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1 MHz, R _L = 50 Ω, C _L = 10 pF	2.25	-2.25	-50	dB
			4.50	-4.50	-50	
			6.00	-6.00	-50	
THD	Total Harmonic Distortion (Figure 15)	f _{in} = 1 kHz, R _L = 10 kΩ, C _L = 50 pF THD = THD _{Measured} - THD _{Source} V _{IS} = 4.0 Vpp sine wave V _{IS} = 8.0 Vpp sine wave V _{IS} = 11.0 Vpp sine wave	2.25	-2.25	0.10	%
			4.50	-4.50	0.08	
			6.00	-6.00	0.05	

*Limits not tested. Determined by design and verified by qualification.

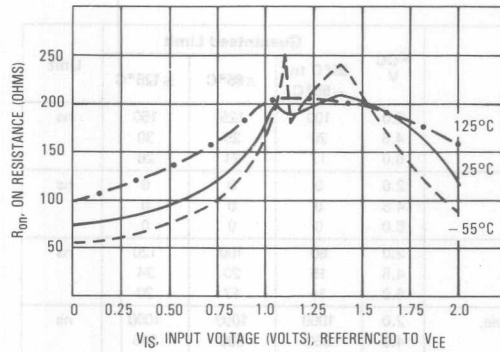


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE} = 2.0$ V

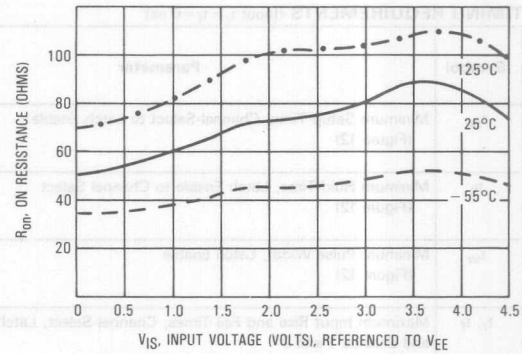


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE} = 4.5$ V

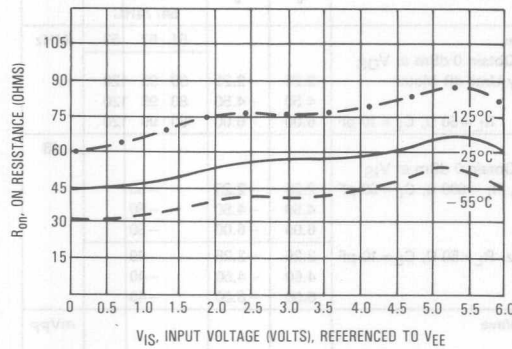


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 6.0$ V

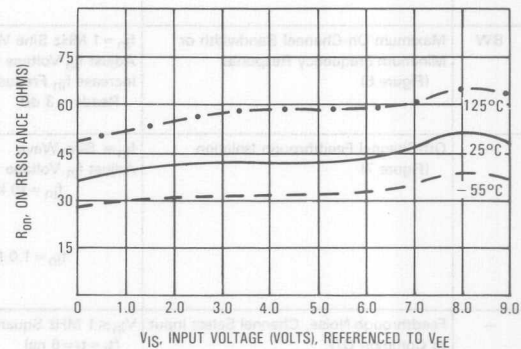


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 9.0$ V

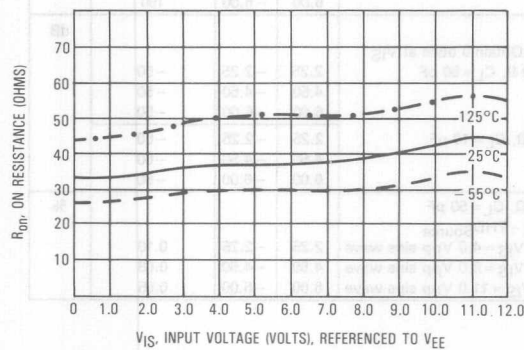


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE} = 12.0$ V

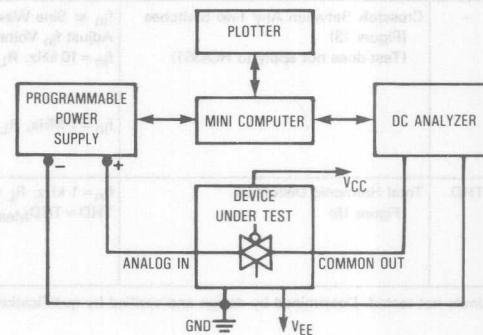


Figure 2. On Resistance Test Set-Up

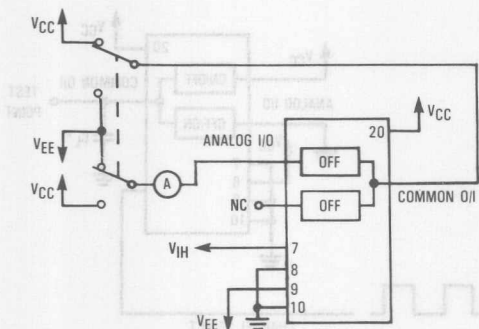


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

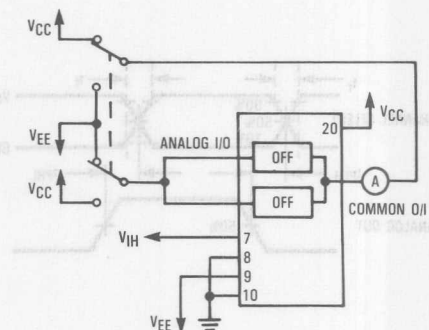


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

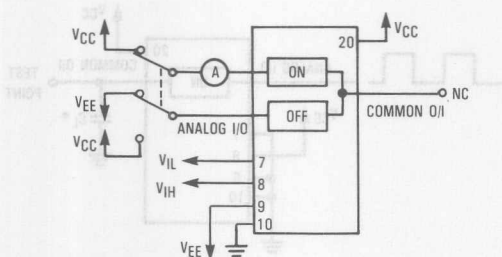
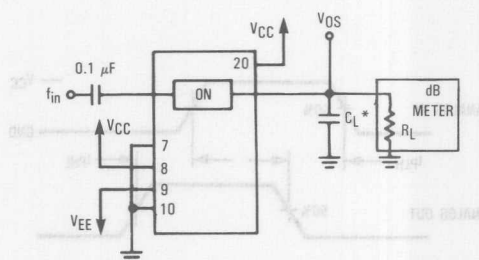
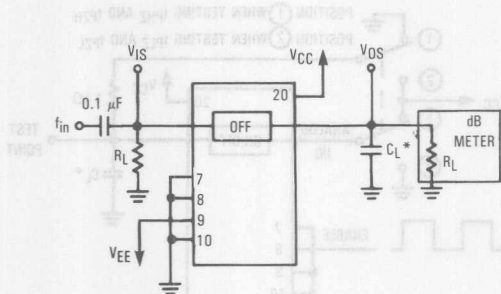


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



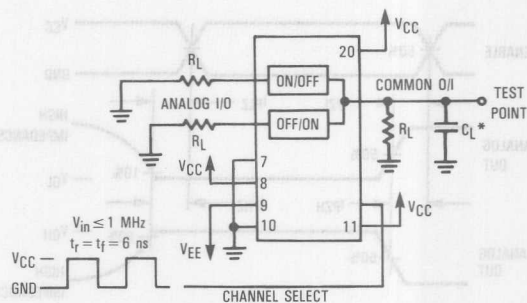
*Includes all probe and jig capacitance.

Figure 6. Maximum On-Channel Bandwidth Test Set-Up



*Includes all probe and jig capacitance.

Figure 7. Off-Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

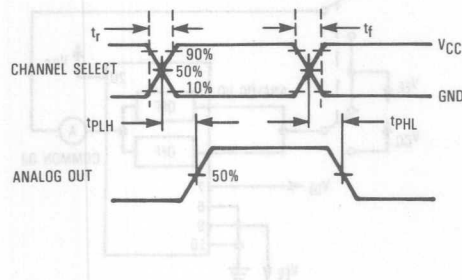
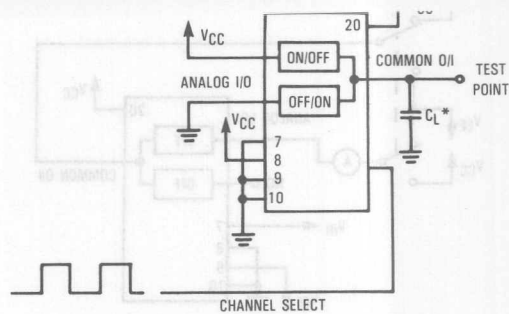


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance.

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

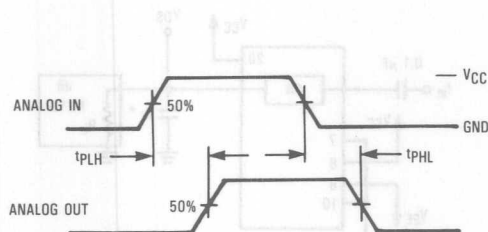
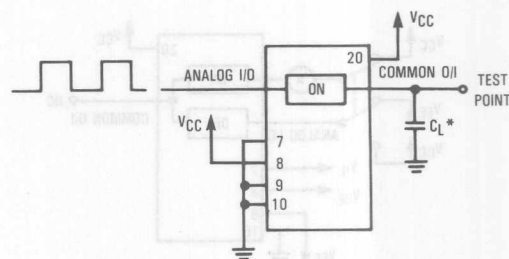


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

5

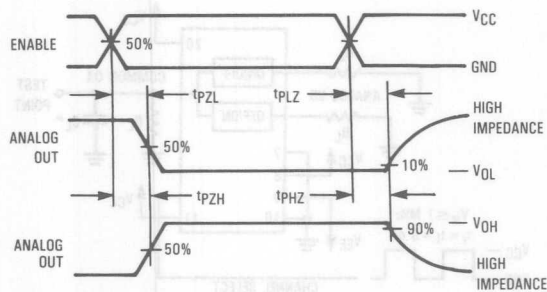
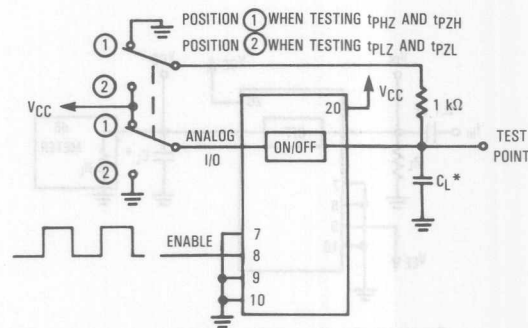
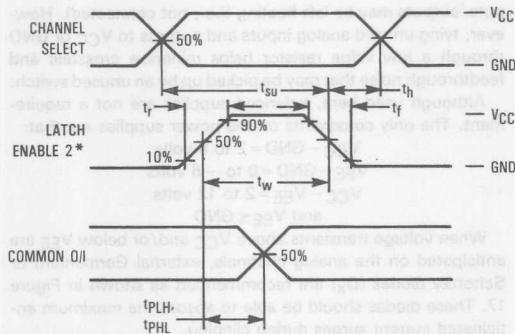


Figure 11a. Propagation Delay, Enable 1 or 2 to Analog Out



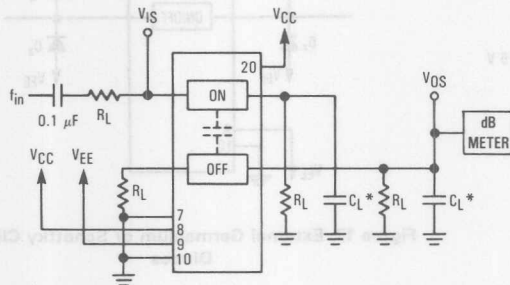
*Includes all probe and jig capacitance.

Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out



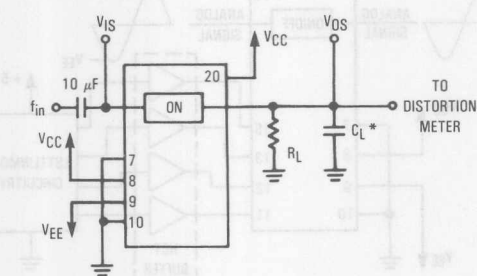
*Latch Enable 1 is a similar waveform except the Latch Enable waveform is inverted.

Figure 12a. Propagation Delay, Latch Enable to Analog Out



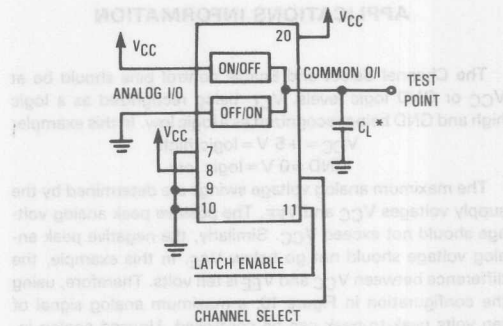
*Includes all probe and jig capacitance.

Figure 13. Crosstalk Between Any Two Switches, Test Set-Up



*Includes all probe and jig capacitance.

Figure 15a. Total Harmonic Distortion, Test Set-Up



*Includes all probe and jig capacitance.

Figure 12b. Propagation Delay, Test Set-Up Latch Enable to Analog Out

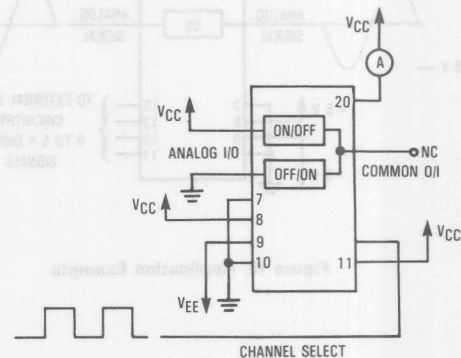


Figure 14. Power Dissipation Capacitance, Test Set-Up

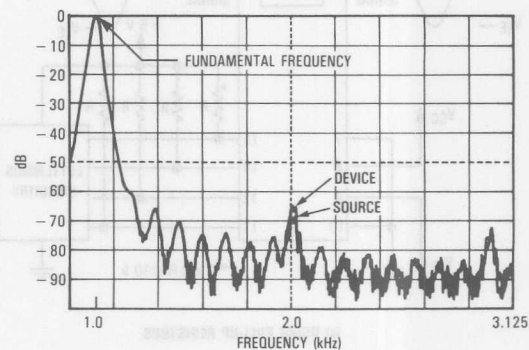


Figure 15b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5 \text{ V} = \text{logic high} \\ \text{GND} &= 0 \text{ V} = \text{logic low} \end{aligned}$$

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below V_{EE} . In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration in Figure 16, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog in-

puts/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{aligned} V_{CC} - \text{GND} &= 2 \text{ to } 6 \text{ volts} \\ V_{EE} - \text{GND} &= 0 \text{ to } -6 \text{ volts} \\ V_{CC} - V_{EE} &= 2 \text{ to } 12 \text{ volts} \\ \text{and } V_{EE} &\leq \text{GND} \end{aligned}$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 17. These diodes should be able to absorb the maximum anticipated current surges during clipping.

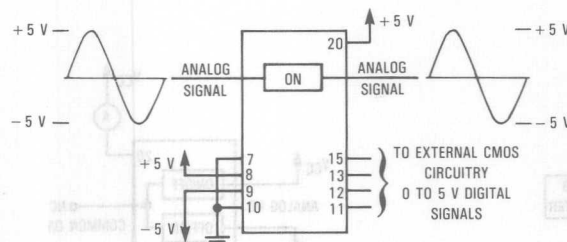


Figure 16. Application Example

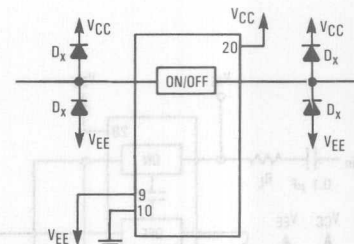
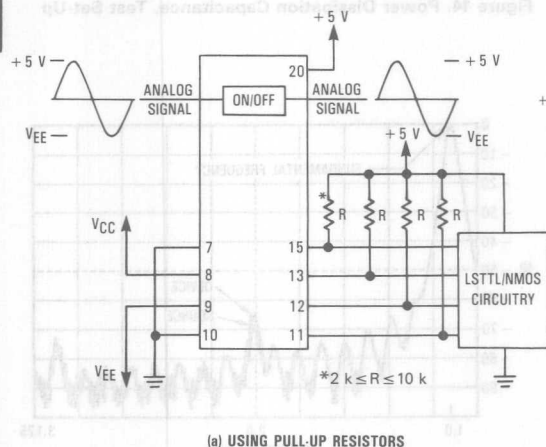
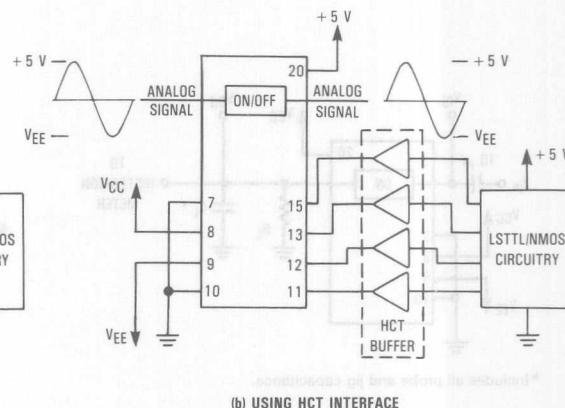


Figure 17. External Germanium or Schottky Clipping Diodes

5



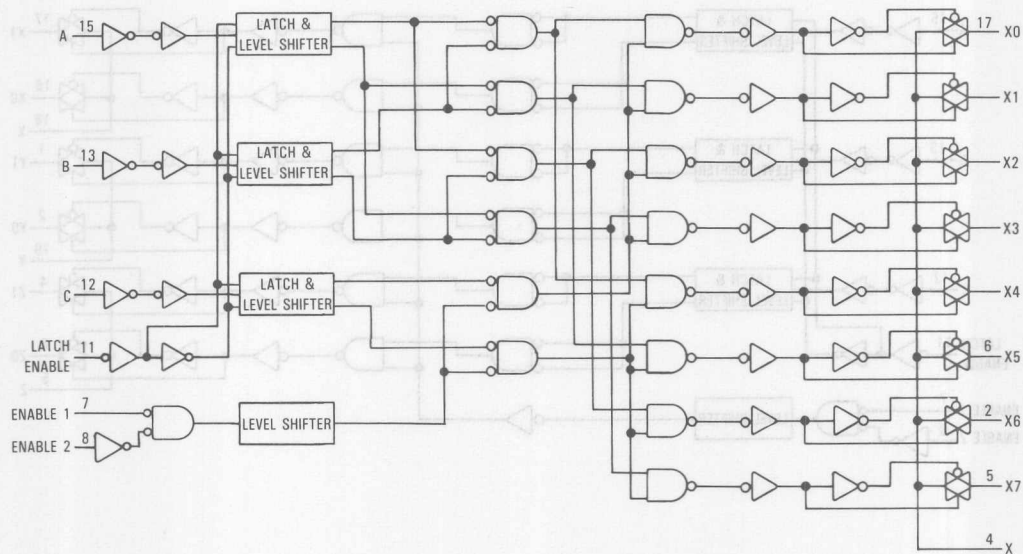
(a) USING PULL-UP RESISTORS



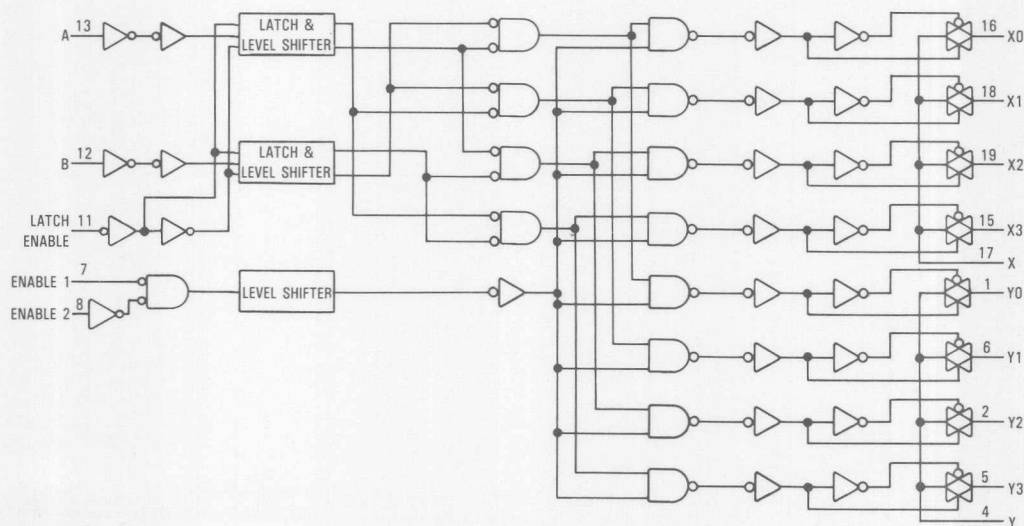
(b) USING HCT INTERFACE

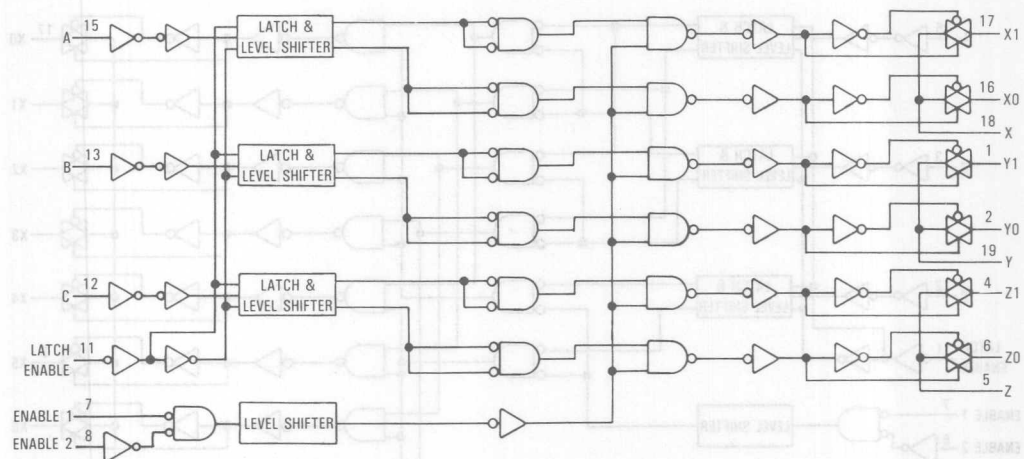
Figure 18. Interfacing LSTTL/NMOS to CMOS Inputs

FUNCTION DIAGRAM HC4351



FUNCTION DIAGRAM HC4352





MC54/74HC4511

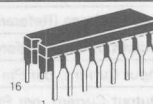
BCD-to-Seven-Segment Latch/ Decoder/Display Driver

High-Performance Silicon-Gate CMOS

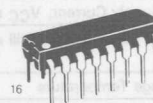
The MC54/74HC4511 is identical in pinout to the MC14511 metal-gate CMOS decoder/driver. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4511 provides the functions of a 4-bit storage latch, a BCD-to-seven-segment decoder, and a display driver. It can be used either directly or indirectly with seven-segment light-emitting diode (LED), incandescent, fluorescent, gas discharge, or liquid-crystal readouts. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn off or pulse modulate the brightness of the display, and to store a BCD code, respectively.

- Latch Storage of BCD Inputs
- Blanking Input
- Lamp Test Input
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B-01

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

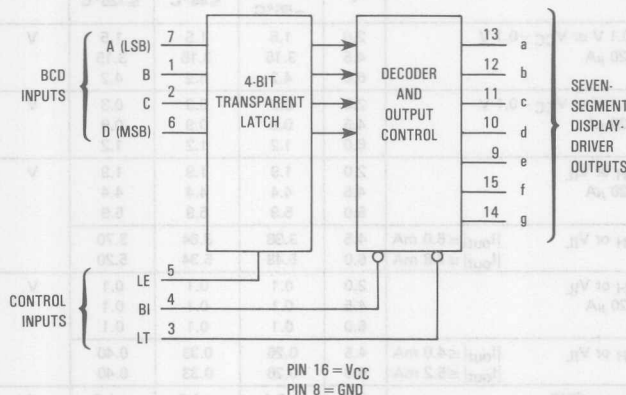
B	1	16	V _{CC}
C	2	15	f
LT	3	14	g
BI	4	13	a
LE	5	12	b
D	6	11	c
A	7	10	d
GND	8	9	e



DISPLAY

0 1 2 3 4 5 6 7 8 9

BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 70	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 3)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4511

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Output (Figures 2 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Blanking Input to Output (Figures 3 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Lamp Test to Output (Figures 4 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 6)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	pF
	70		

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input A, B, C, or D to Latch Enable (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Latch Enable to Input A, B, C, or D (Figure 5)	2.0 4.5 6.0	0 0 0	0 0 0	0 0 0	ns
t _w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 3)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

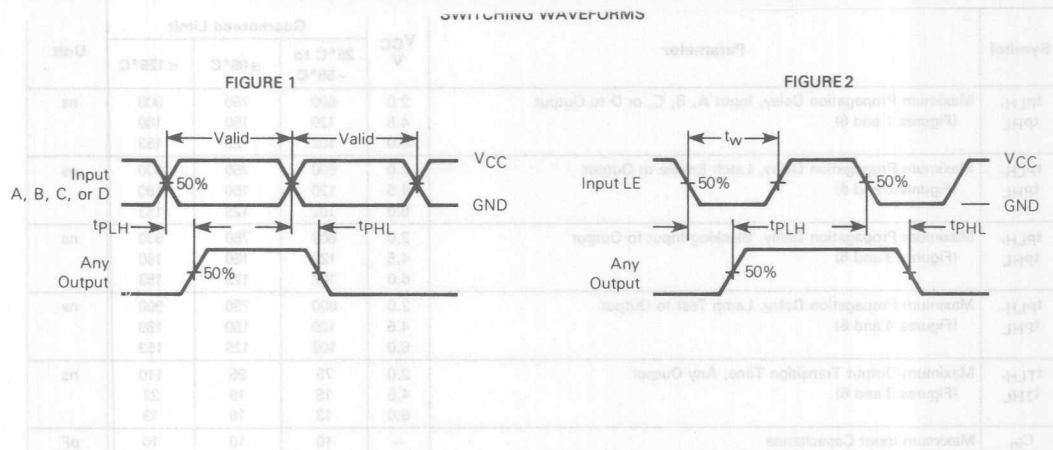


FIGURE 3

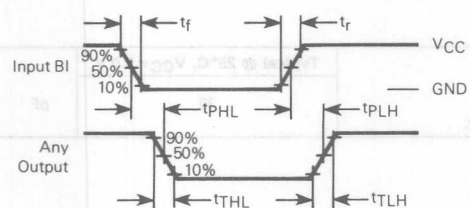
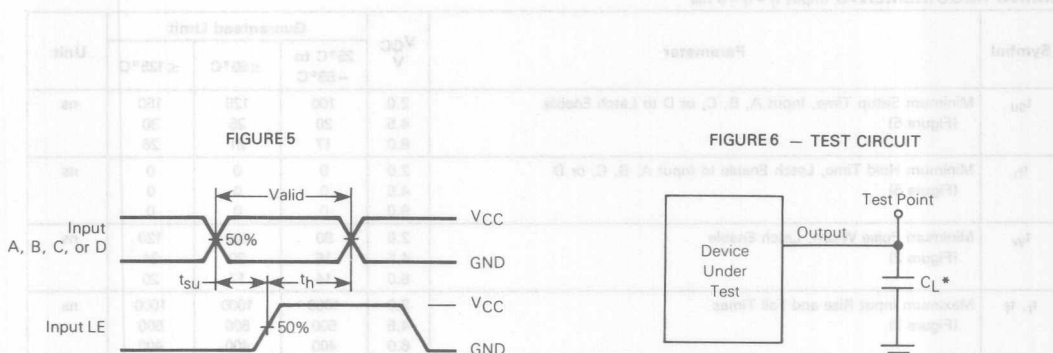
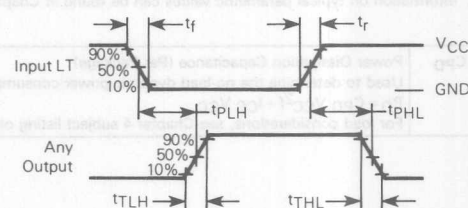


FIGURE 4



* Includes all probe and jig capacitance.

MC54/74HC4511

FUNCTION TABLE

Inputs						Outputs									
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8	
X	L	H	X	X	X	X	L	H	L	L	L	L	L	Blank	
L	H	H	L	L	L	L	L	H	H	H	H	H	L	0	
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1	
L	H	H	L	L	H	L	H	H	L	H	L	H	L	2	
L	H	H	L	L	H	H	H	H	H	L	L	L	H	3	
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4	
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5	
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6	
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7	
L	H	H	H	L	L	L	L	H	H	H	H	H	H	8	
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9	
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank	
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank	
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank	
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank	
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank	
H	H	H	X	X	X	X	*							*	

* = Depends upon the BCD code previously applied while LE was at a low level.

PIN DESCRIPTIONS

INPUTS

A, B, C, D (PINS 7, 1, 2, 6) — BCD inputs. A (pin 7) is the least significant bit and D (pin 6) is the most significant bit. Hexadecimal code A-F at these inputs causes the outputs to assume a low level, offering an alternate method of blanking the display.

OUTPUTS

a, b, c, d, e, f, g (PINS 13, 12, 11, 10, 9, 15, 14) — Decoded, buffered seven-segment display-driver outputs. These outputs, unlike the MC14511, have CMOS drivers, which produce typical CMOS output voltage levels. These outputs are connected to various displays as shown in Figure 7.

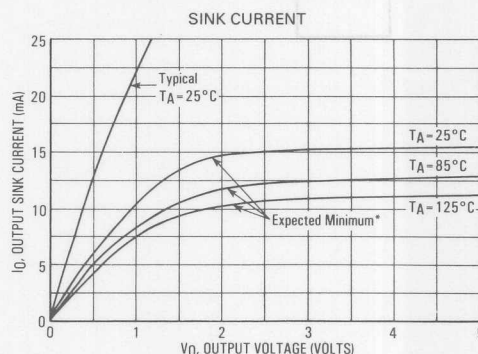
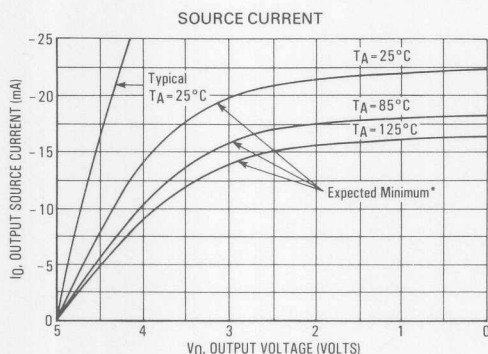
CONTROL INPUTS

BI (PIN 4) — Active-low display blanking input. A low level on this input will cause all outputs to be held low, thereby blanking the display. LT is the only input that overrides the BI input.

LT (PIN 3) — Active-low lamp test. A low level on this input causes all outputs to assume a high level. This input allows the user to test all segments of a display with a single control input. This input is independent of all other inputs.

LE (PIN 5) — Latch enable input. This input controls the 4-bit transparent latch. A high level on this input latches the code present at the A, B, C and D inputs; a low level allows the code to be transmitted through the latch to the decoder.

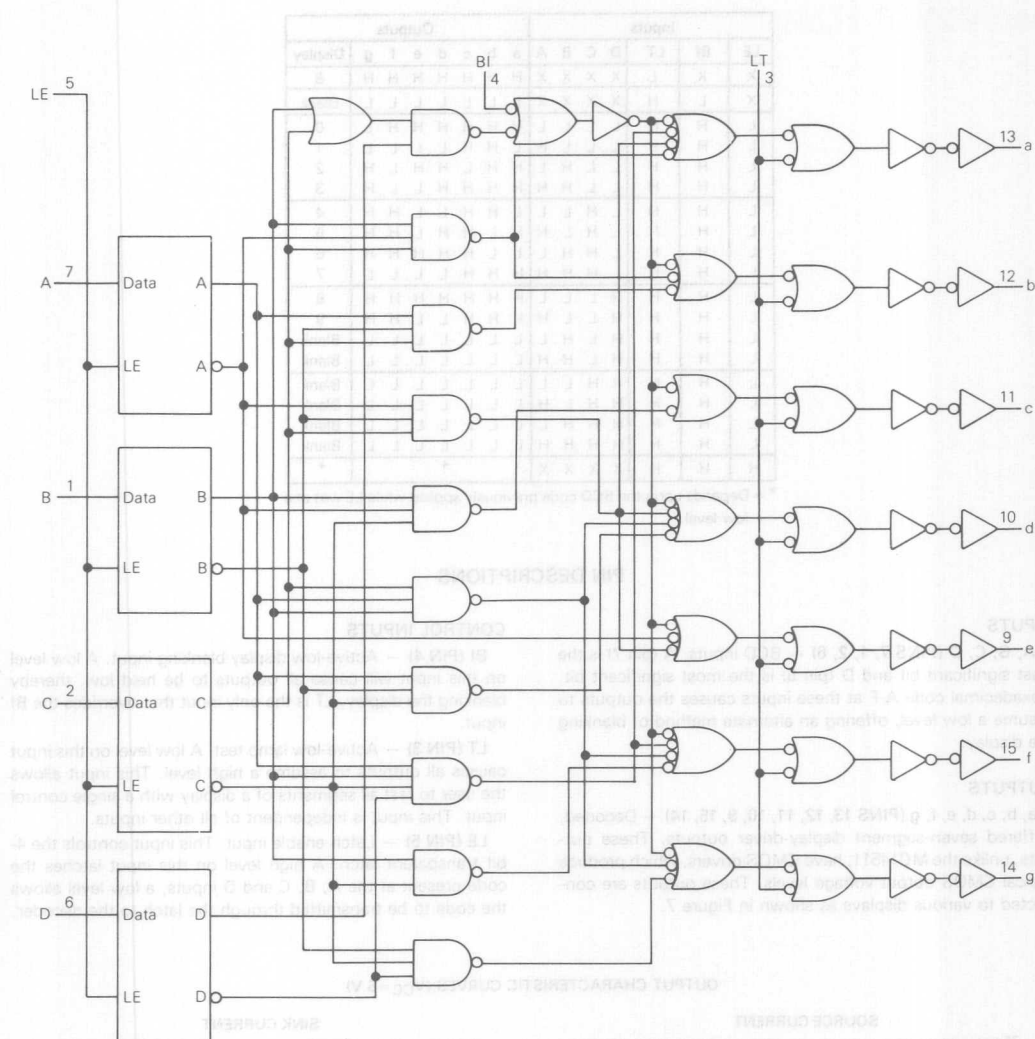
OUTPUT CHARACTERISTIC CURVES ($V_{CC} = 5\text{ V}$)



* The expected minimum curves are not guarantees, but are design aids.

MC54/74HC4511

EXPANDED LOGIC DIAGRAM



5

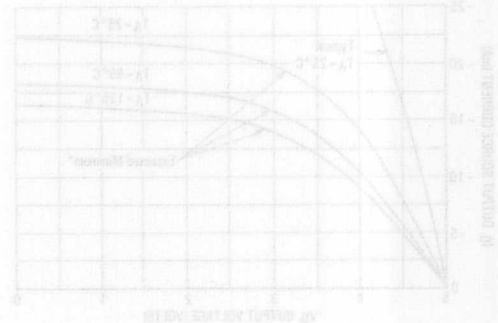
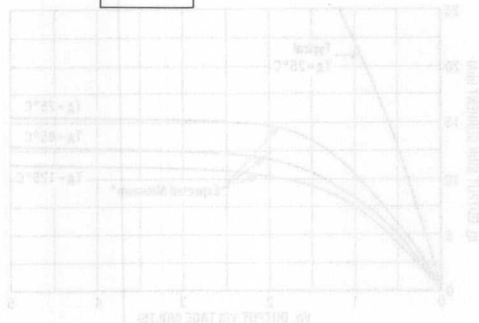
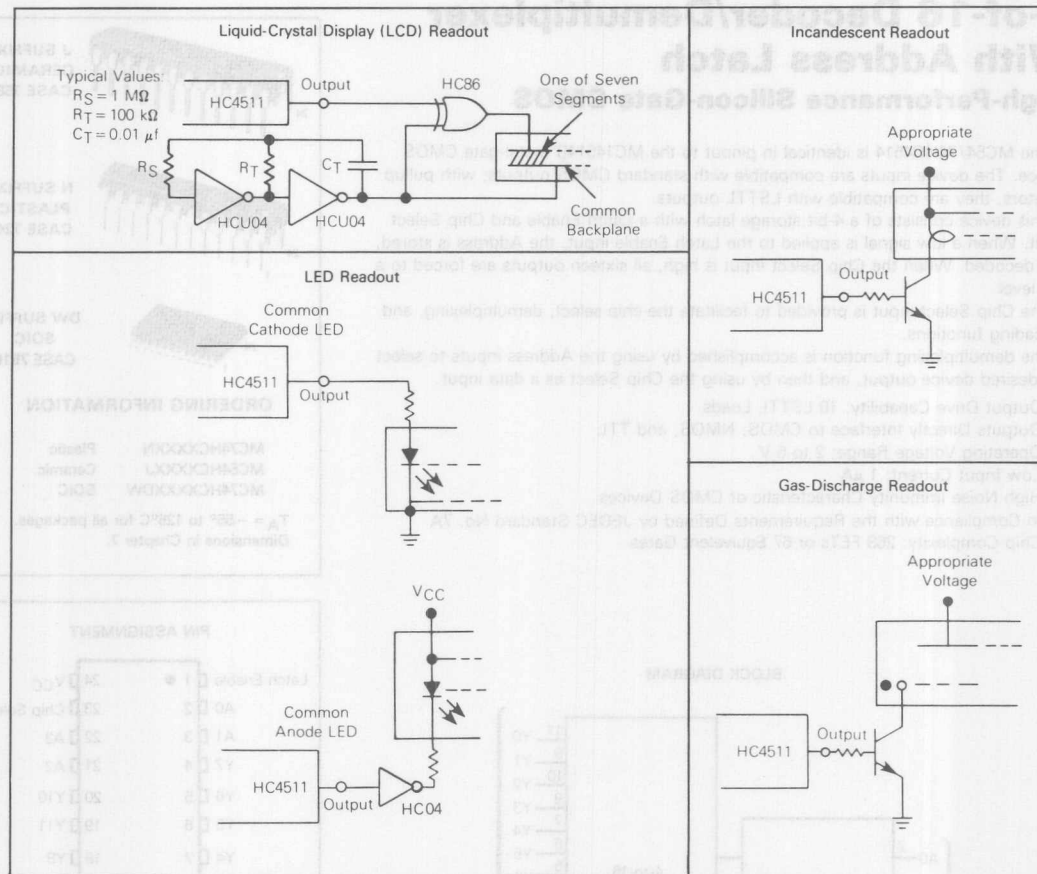


FIGURE 7 — CONNECTIONS TO VARIOUS DISPLAY READOUTS



1-of-16 Decoder/Demultiplexer With Address Latch High-Performance Silicon-Gate CMOS

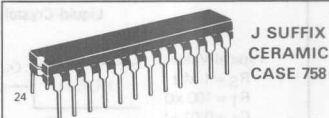
The MC54/74HC4514 is identical in pinout to the MC14514B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of a 4-bit storage latch with a Latch Enable and Chip Select input. When a low signal is applied to the Latch Enable input, the Address is stored, and decoded. When the Chip Select input is high, all sixteen outputs are forced to a low level.

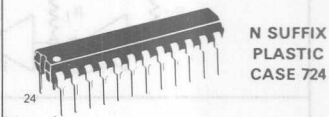
The Chip Select input is provided to facilitate the chip-select, demultiplexing, and cascading functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using the Chip Select as a data input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 268 FETs or 67 Equivalent Gates



J SUFFIX
CERAMIC
CASE 758



N SUFFIX
PLASTIC
CASE 724



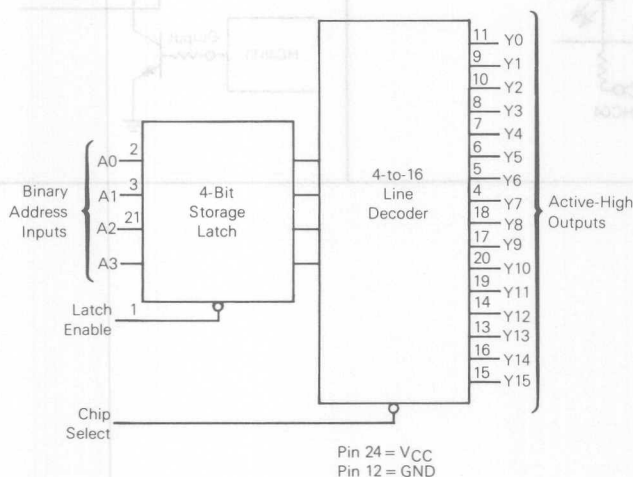
DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

BLOCK DIAGRAM



PIN ASSIGNMENT

Latch Enable	1	24	VCC
A0	2	23	Chip Select
A1	3	22	A3
A2	21	21	A2
A3	20	20	Y10
	19	19	Y11
	18	18	Y8
	17	17	Y9
	16	16	Y14
	15	15	Y15
	14	14	Y12
	13	13	Y13
GND	12		

MC54/74HC4514

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	−55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V 0 V _{CC} = 4.5 V 0 V _{CC} = 6.0 V 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4514

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Chip Select to Output Y (Figures 1 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 5)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t _{PHL}		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 3 and 5)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t _{PHL}		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance		10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		70	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input A to Latch Enable (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Enable to Input A (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Latch Enable (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

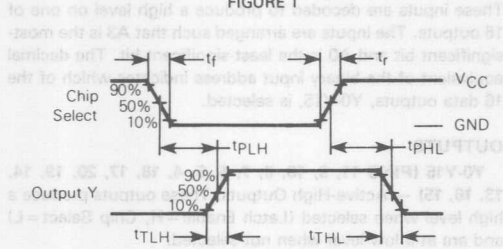
MC54/74HC4514

FUNCTION TABLE

SWITCHING WAVEFORMS

ADDRESS INPUTS

These inputs are decoded such that a high level on one of the inputs is decoded as a high level on one of the outputs. The inputs are decoded such that a high level on one of the inputs is decoded as a high level on one of the outputs. The inputs are decoded such that a high level on one of the inputs is decoded as a high level on one of the outputs.



CONTROL INPUTS

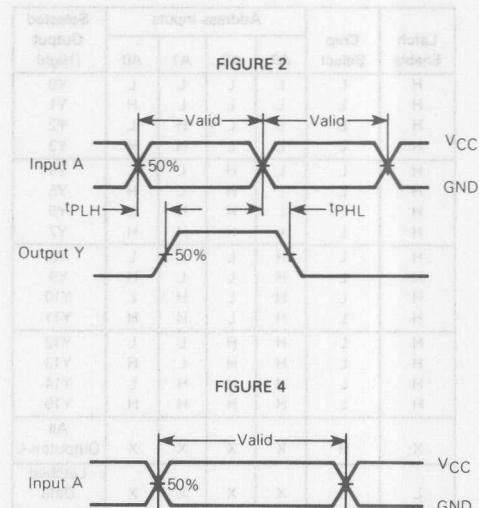
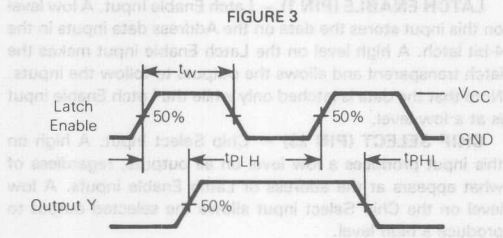
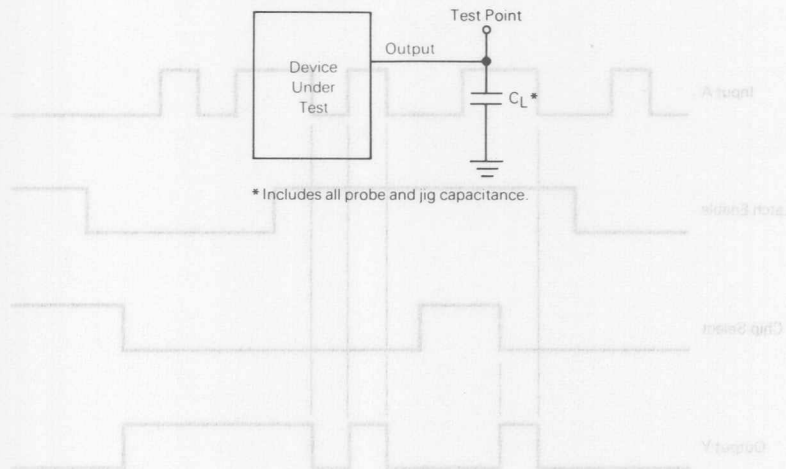


FIGURE 5 — TEST CIRCUIT



Latch Enable	Chip Select	Address Inputs				Selected Output (High)
		A3	A2	A1	A0	
H	L	L	L	L	L	Y0
H	L	L	L	L	H	Y1
H	L	L	L	H	L	Y2
H	L	L	L	H	H	Y3
H	L	L	H	L	L	Y4
H	L	L	H	L	H	Y5
H	L	L	H	H	L	Y6
H	L	L	H	H	H	Y7
H	L	H	L	L	L	Y8
H	L	H	L	L	H	Y9
H	L	H	L	H	L	Y10
H	L	H	L	H	H	Y11
H	L	H	H	L	L	Y12
H	L	H	H	L	H	Y13
H	L	H	H	H	L	Y14
H	L	H	H	H	H	Y15
X	H	X	X	X	X	All Outputs = L
L	L	X	X	X	X	Latched Data

ADDRESS INPUTS

A0, A1, A2, A3 (PINS 2, 3, 21, 22) — Address Inputs. These inputs are decoded to produce a high level on one of 16 outputs. The inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. The decimal equivalent of the binary input address indicates which of the 16 data outputs, Y0-Y15, is selected.

OUTPUTS

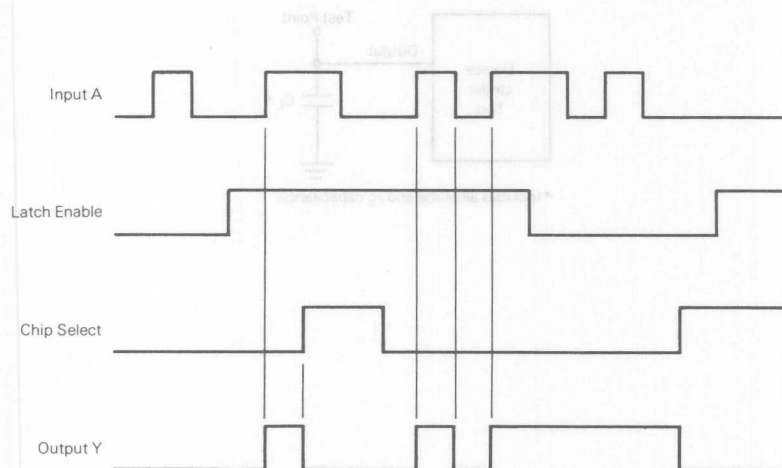
Y0-Y15 (PINS 11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15) — Active-High Outputs. These outputs produce a high level when selected (Latch Enable = H, Chip Select = L) and are at a low level when not selected.

CONTROL INPUTS

LATCH ENABLE (PIN 1) — Latch Enable Input. A low level on this input stores the data on the Address data inputs in the 4-bit latch. A high level on the Latch Enable input makes the latch transparent and allows the outputs to follow the inputs. Note that the data is latched only while the Latch Enable input is at a low level.

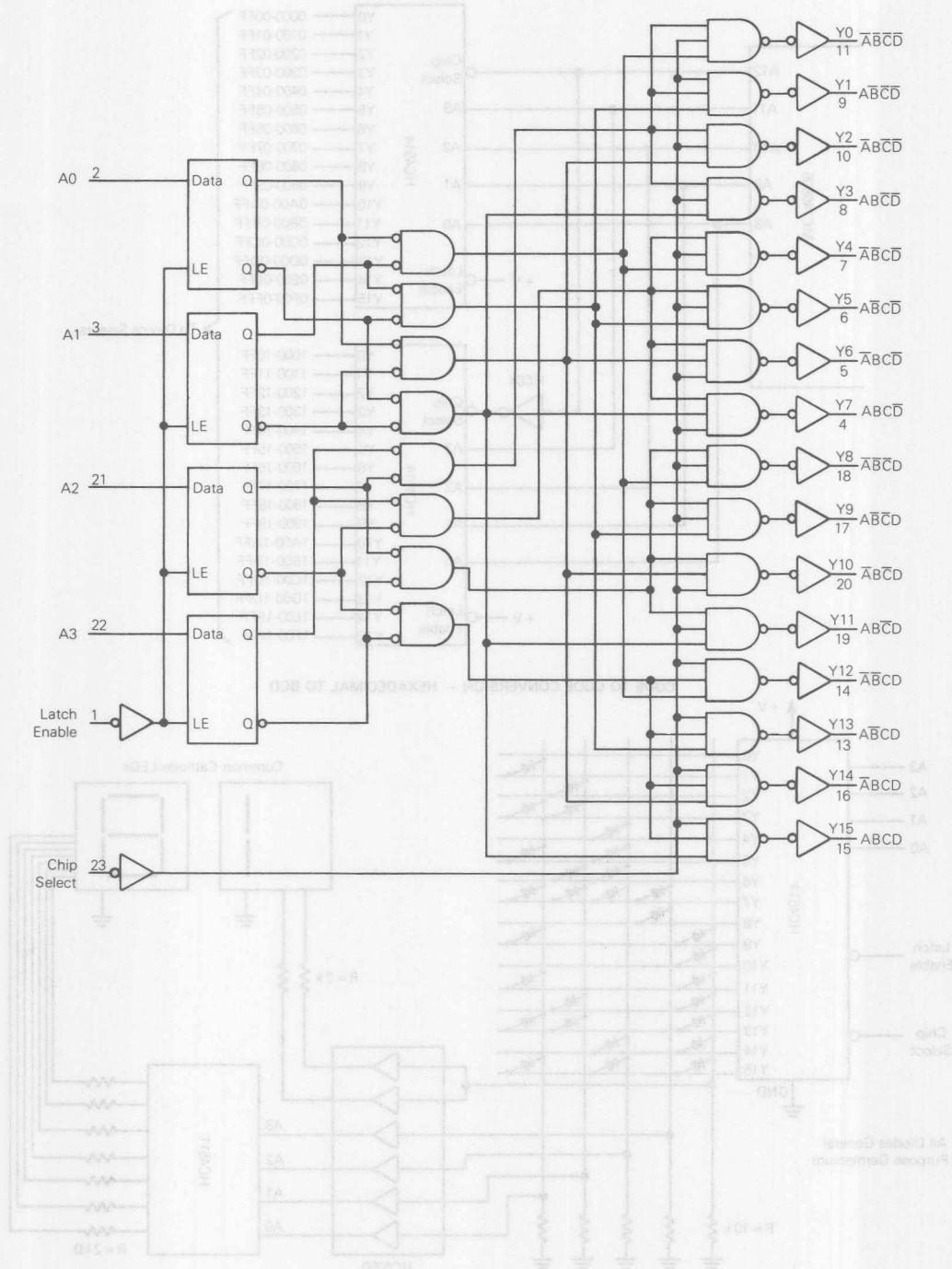
CHIP SELECT (PIN 23) — Chip Select Input. A high on this input produces a low level on all outputs, regardless of what appears at the address or Latch Enable inputs. A low level on the Chip Select input allows the selected output to produce a high level.

TIMING DIAGRAM



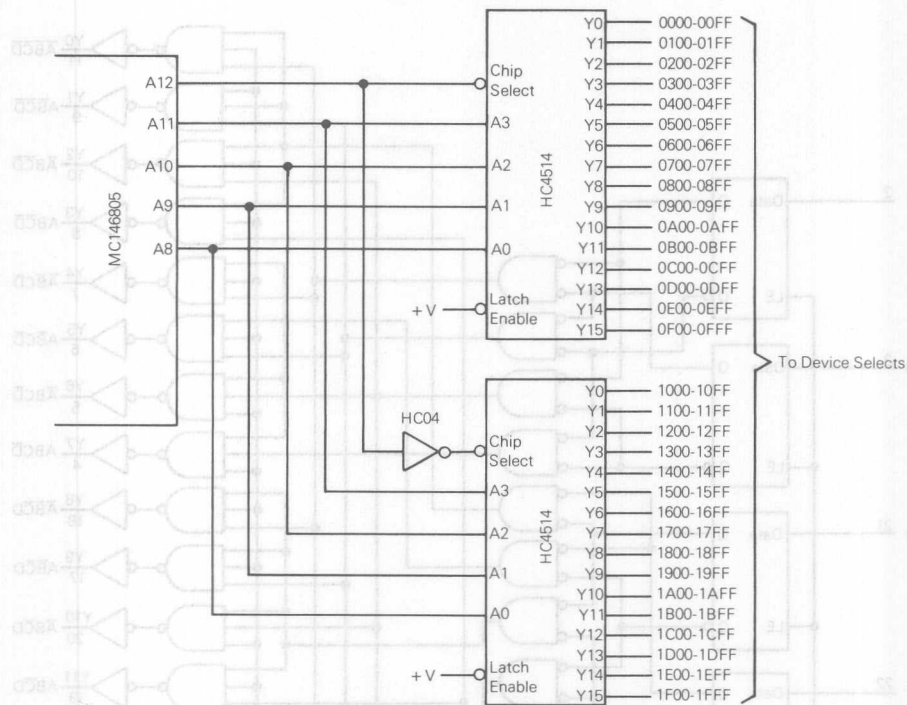
MC54/74HC4514

EXPANDED LOGIC DIAGRAM

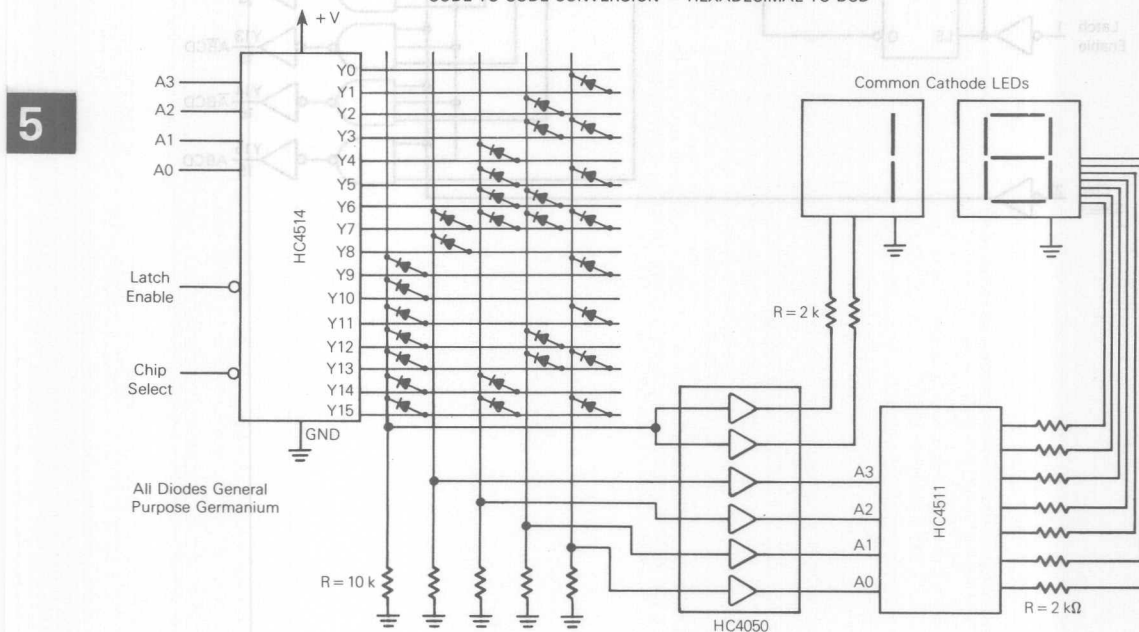


MC54/74HC4514

MICROPROCESSOR MEMORY DECODING



CODE TO CODE CONVERSION — HEXADECIMAL TO BCD



MC54/74HC4538

**Dual Precision Monostable
Multivibrator (Retriggerable,
Resettable)**

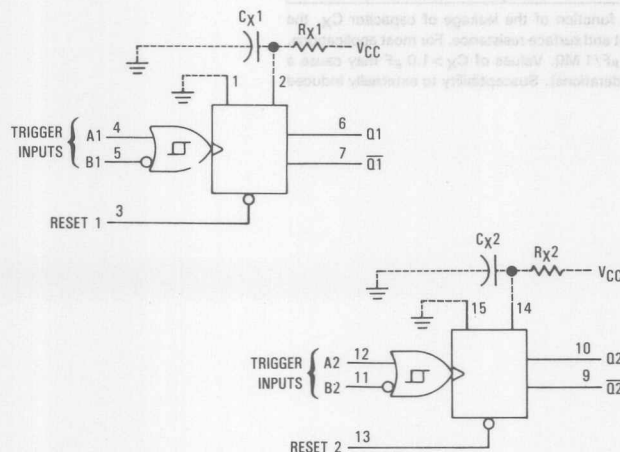
High-Performance Silicon-Gate CMOS

The MC54/74HC4538 is identical in pinout to the MC14538B and the MC14528B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

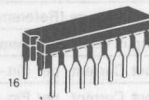
This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and produces a precision output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger-input rise and fall time restrictions. The output pulse width is determined by the external timing components, R_X and C_X . The device has a reset function which forces the Q output low and the \bar{Q} output high, regardless of the state of the output pulse circuitry.

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse Width is Independent of the Trigger Pulse Width
- $\pm 10\%$ Guaranteed Pulse Width Variation from Part to Part (Using the Same Test Jig)
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: $1 \mu A$
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 145 FETs or 36 Equivalent Gates

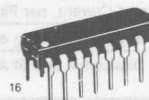
BLOCK DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND
 R_X AND C_X ARE EXTERNAL COMPONENTS
PIN 1 AND PIN 15 MUST BE HARD WIRED TO GND



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC74HCXXXN Plastic
MC54HCXXXJ Ceramic
MC74HCXXXDW SOIC

$T_A = -55^\circ$ to $125^\circ C$ for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

GND	1	16	V_{CC}
C_X1/R_X1	2	15	GND
RESET 1	3	14	C_X2/R_X2
A1	4	13	RESET 2
B1	5	12	A2
Q1	6	11	B2
$\bar{Q}1$	7	10	Q2
GND	8	9	$\bar{Q}2$

FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	\bar{Q}
H	H	H		
H	H	L	Not Triggered	Not Triggered
H	L	H	Not Triggered	Not Triggered
H	L	L	Not Triggered	Not Triggered
L	X	X	L	H
X	X	X	Not Triggered	Not Triggered

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin—A, B, Reset	± 20	mA
I_{in}	DC Input Current, per Pin— C_X/R_X	± 30	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

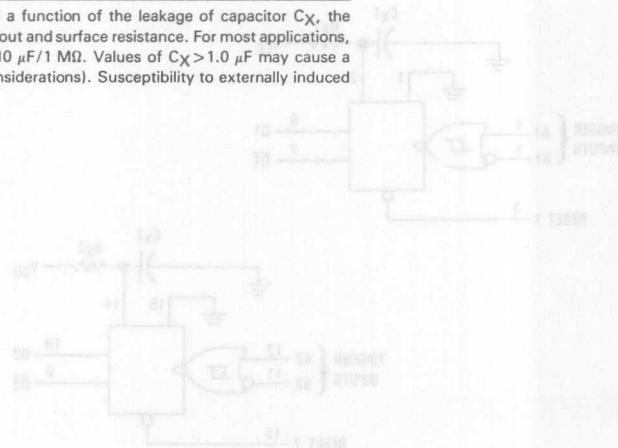
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time—Reset (Figure 5)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	
		A or B (Figure 5)	—	no limit	
R _X	External Timing Resistor	V _{CC} < 4.5 V	2.0	*	kΩ
		V _{CC} ≥ 4.5 V	1.0	*	
C _X	External Timing Capacitor	0	*	μF	

*The maximum allowable values of R_X and C_X are a function of the leakage of capacitor C_X , the leakage of the HC4538, and leakage due to board layout and surface resistance. For most applications, C_X/R_X should be limited to a maximum value of 10 $\mu\text{F}/1 \text{ M}\Omega$. Values of $C_X > 1.0 \mu\text{F}$ may cause a problem during power down (see Power-Down Considerations). Susceptibility to externally induced noise signals may occur for $R_X > 1 \text{ M}\Omega$.

5

FUNCTION TABLE				
Outputs		Inputs		
Q	Q'	B	A	Reset
				
				
Not Triggered		L	X	H
Not Triggered		X	H	H
Not Triggered		H	X	H
Not Triggered		X	X	H
L		L	X	L
Not Triggered		X	X	L



MC54/74HC4538

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current (A, B, Reset)	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{in}	Maximum Input Leakage Current (C _X /R _X)	V _{in} = V _{CC} or GND	6.0	± 50	± 500	± 500	nA
I _{CC}	Maximum Quiescent Supply Current (per Package) Standby State	V _{in} = V _{CC} or GND Q1 and Q2 = Low I _{out} = 0 μA	6.0	130	220	350	μA
I _{CC}	Maximum Supply Current (per Package) Active State	V _{in} = V _{CC} or GND Q1 and Q2 = High I _{out} = 0 μA Pins 2 and 14 = 0.5 V _{CC}	6.0	150	250	400	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH}	Maximum Propagation Delay, Input A or B to Q (Figures 4 and 6)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
t _{PHL}	Maximum Propagation Delay, Input A or B to \bar{Q} (Figures 4 and 6)	2.0 4.5 6.0	275 55 47	345 69 59	415 83 71	ns
t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 5 and 6)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
t _{PLH}	Maximum Propagation Delay, Reset to \bar{Q} (Figures 5 and 6)	2.0 4.5 6.0	275 55 47	345 69 59	415 83 71	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 5 and 6)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance (A, B, Reset) (C _X , R _X)	— —	10 25	10 25	10 25	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Multivibrator)	Typical @ 25°C, V _{CC} = 5.0 V	pF
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	150	

MC54/74HC4538

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{rr}^*	Minimum Retrigger Time, Input A or B (Figure 5)	2.0 4.5 6.0	— — —	— — —	— — —	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to A or B (Figure 5)	2.0 4.5 6.0	0 0 0	0 0 0	0 0 0	ns
t_w	Minimum Pulse Width, Input A or B (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 5)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times, Reset (Figure 5)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	
	A or B (Figure 5)	2.0	No Limit			
		4.5				
		6.0				

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

$$*t_{rr} \text{ (ns)} \approx 72 + \frac{V_{CC} \text{ (volts)} \cdot C_X \text{ (pF)}}{30.5}$$

OUTPUT PULSE WIDTH CHARACTERISTICS ($C_L = 50$ pF)

Symbol	Parameter	Conditions		Temperature						Unit
		Timing Components	VCC V	25°C		−40° to 85°C		−55° to 125°C		
				Min	Max	Min	Max	Min	Max	
τ	Output Pulse Width* (Figures 4 and 6)	R _X = 10 k Ω , C _X = 0.1 μ F	5.0	0.63	0.77	0.60	0.80	0.59	0.81	ms
—	Pulse Width Match Between Circuits in the Same Package	—	—	± 5						%
—	Pulse Width Match Variation (Part to Part)	—	—	± 10						%

*For output pulse widths greater than 100 μ s, typically $\tau = kR_X C_X$, where the value of k may be found in Figure 1.

5

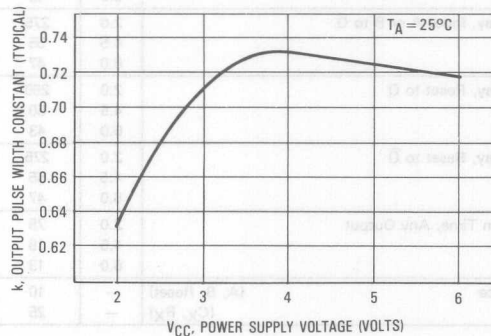


Figure 1. Typical Output Pulse Width Constant, k,
versus Supply Voltage
(For output pulse widths ≥ 100 μ s: $\tau = kR_X C_X$)

MC54/74HC4538

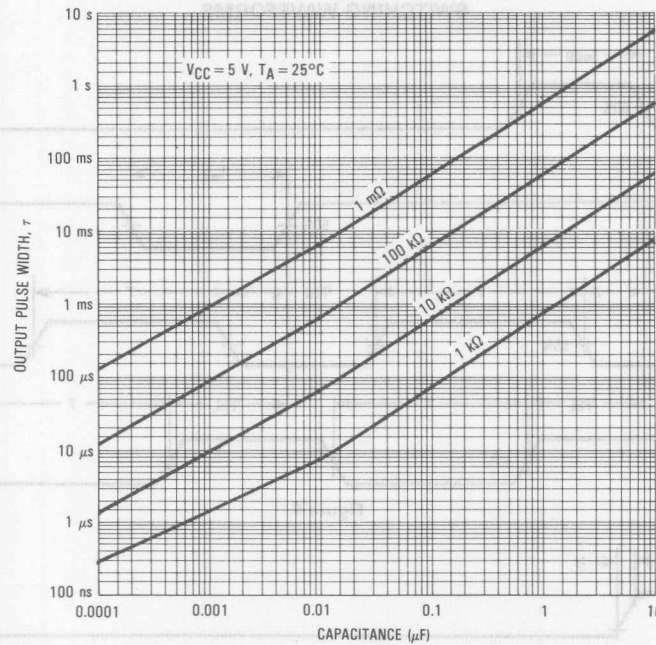


Figure 2. Output Pulse Width vs. Timing Capacitance

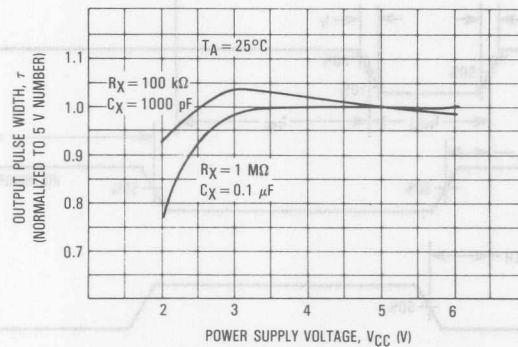


Figure 3. Normalized Output Pulse Width versus Power Supply Voltage

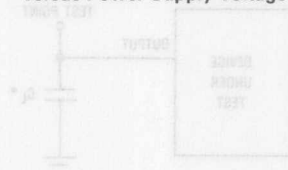


Figure 4. Test Circuit

MC54/74HC4538

SWITCHING WAVEFORMS

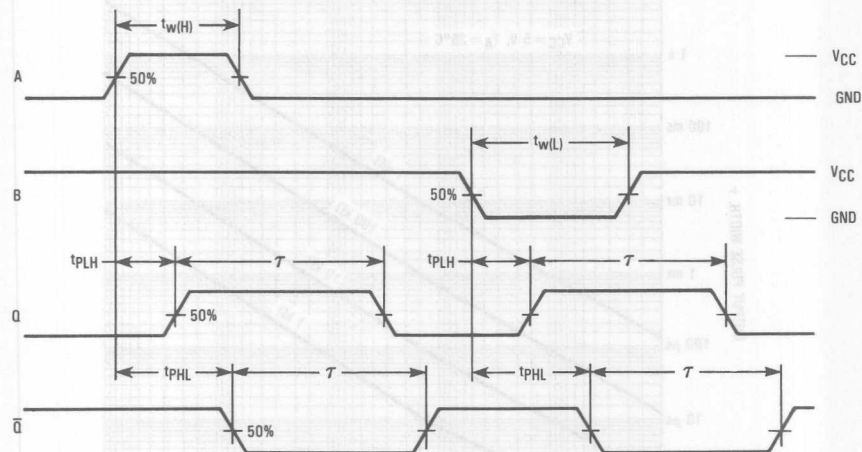


Figure 4

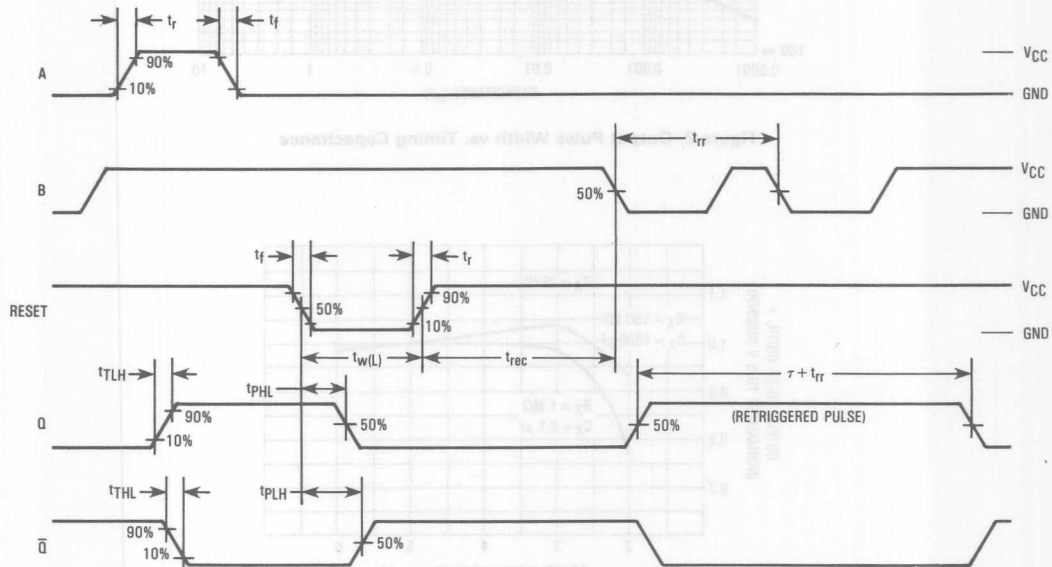
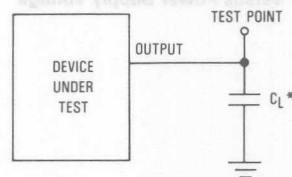


Figure 5



*Includes all probe and jig capacitance.

Figure 6. Test Circuit

MC54/74HC4538

PIN DESCRIPTIONS

INPUTS

A1, A2 (PINS 4, 12) — Positive-edge trigger inputs. A rising-edge signal on either of these pins triggers the corresponding multivibrator when there is a high level on the B1 or B2 input.

B1, B2 (PINS 5, 11) — Negative-edge trigger inputs. A falling-edge signal on either of these pins triggers the corresponding multivibrator when there is a low level on the A1 or A2 input.

RESET 1, RESET 2 (PINS 3, 13) — Reset inputs (active low). When a low level is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low level and the \bar{Q} output is set to a high level.

C_X1/R_X1 and C_X2/R_X2 (PINS 2 and 14) — External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram). Polystyrene capacitors are recommended for optimum

pulse width control. Electrolytic capacitors are not recommended due to high leakages associated with these type capacitors.

GND (PINS 1 and 15) — External ground. The external timing capacitors discharge to ground through these pins.

OUTPUTS

Q1, Q2 (PINS 6, 10) — Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R_X and C_X.

Q1, Q2 (PINS 7, 9) — Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

LOGIC DETAIL (½ the Device)

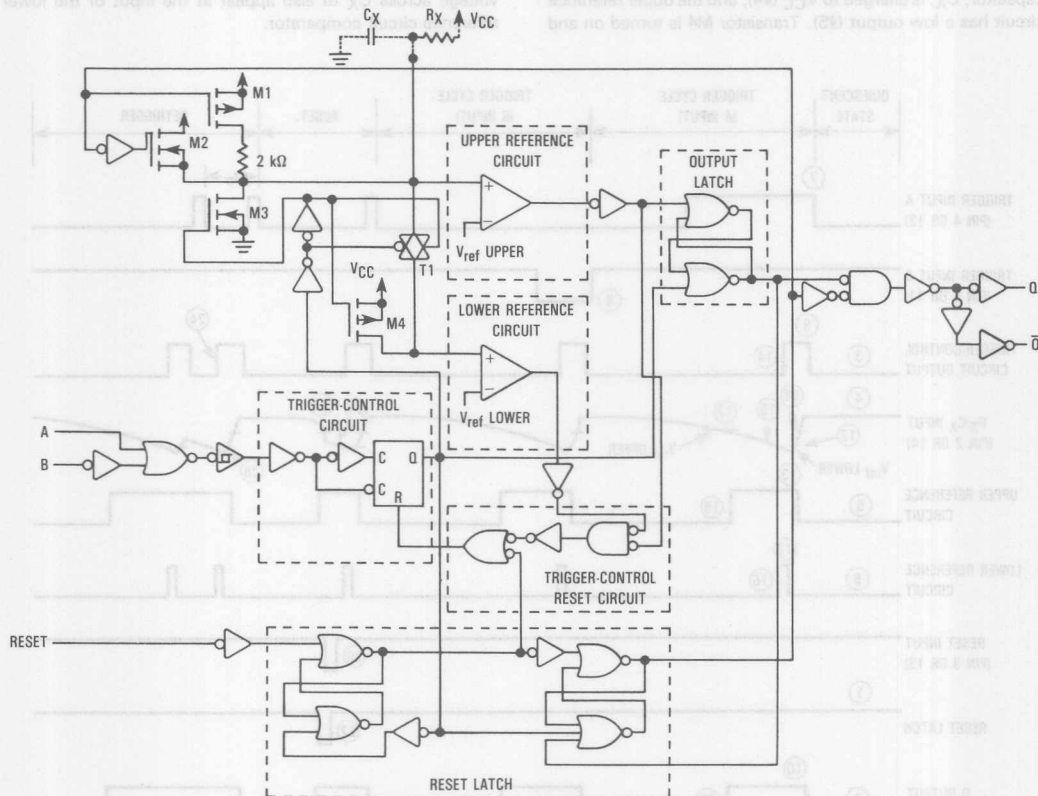


Figure 7

Figure 10 shows the HC4538 configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 7): In the quiescent state, the external timing capacitor, C_X , is charged to V_{CC} . When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage ($V_{ref\ Lower} \approx 1/3 V_{CC}$). C_X then charges, through R_X , back up to the upper reference voltage ($V_{ref\ Upper} \approx 2/3 V_{CC}$), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic detail (Figure 7) and the timing diagram (Figure 8).

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 8). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 8).

The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X , is charged to V_{CC} (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and

transmission gate T1 is turned off. Thus the lower reference circuit has V_{CC} at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The HC4538 is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the HC4538 to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X , to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.

5

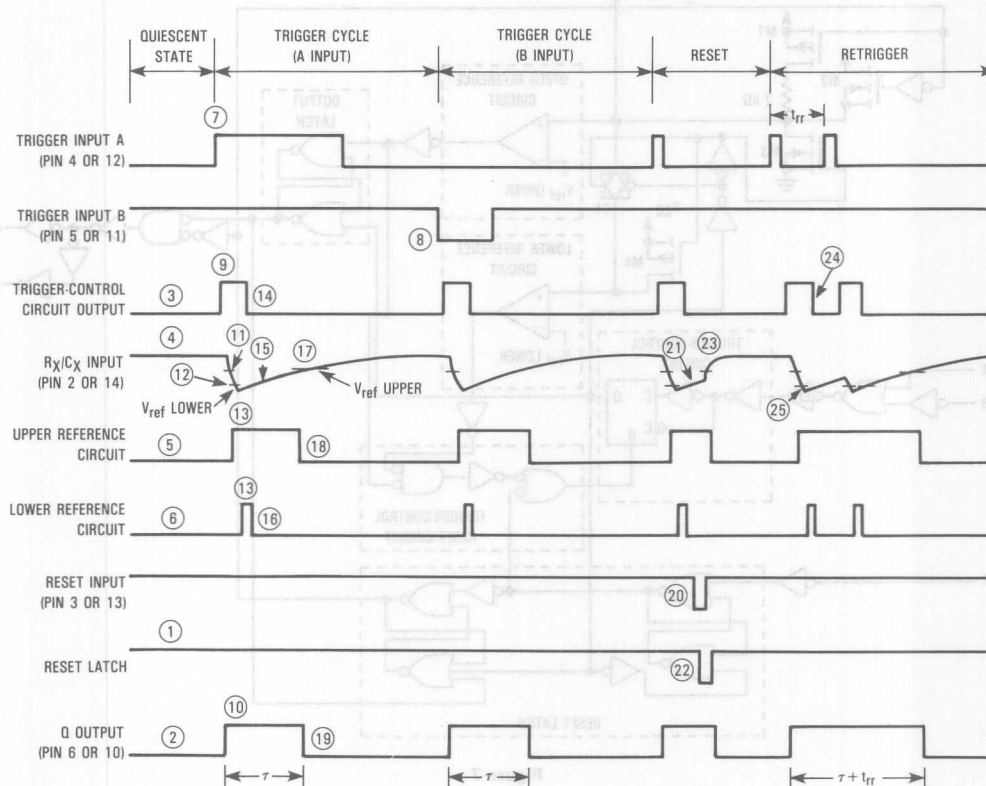


Figure 8. Timing Diagram

MC54/74HC4538

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{CC} , with a time constant $t = R_X C_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the HC4538 to a low state (#19), and completing the time-out cycle.

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the HC4538 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \cdot C_X / (30 \text{ mA})$. For example, if $V_{CC} = 5 \text{ V}$ and $C_X = 15 \mu\text{F}$, the V_{CC} supply must turn off no faster than $t = (5 \text{ V}) \cdot (15 \mu\text{F}) / 30 \text{ mA} = 2.5 \text{ ms}$. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{CC} to zero volts occurs, the HC4538 may sustain damage. To avoid this possibility, use an external damping diode, D_X , connected as shown in Figure 9. Best results can be achieved if diode D_X is chosen to be a germanium or Schottky type diode able to withstand large current surges.

RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the HC4538 to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{CC} (#23) to await the next trigger signal.

RETRIGGER OPERATION

When used in the retriggerable mode (Figure 10), the HC4538 may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rr} (Figure 5) is a function of internal propagation delays and the discharge time of C_X :

$$t_{rr} (\text{ns}) \approx 72 + \frac{V_{CC} (\text{volts}) \cdot C_X (\text{pF})}{30.5}, \text{ at room temperature}$$

Figure 11 shows the device configured in the nonretriggerable mode.

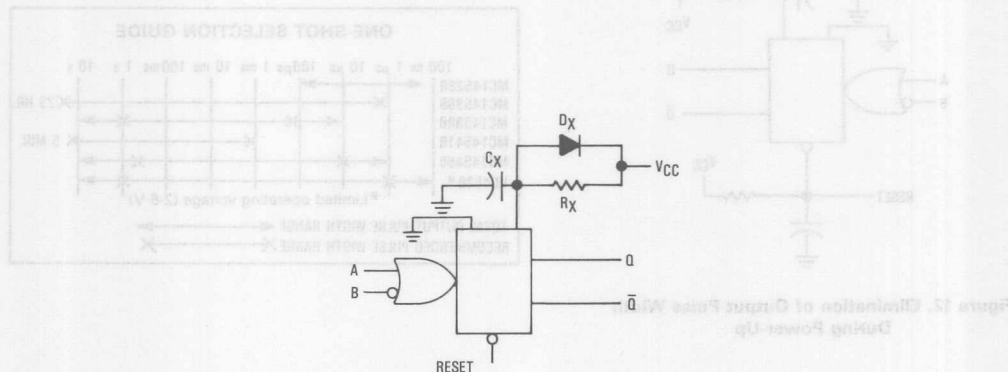


Figure 9. Discharge Protection During Power Down

TYPICAL APPLICATIONS

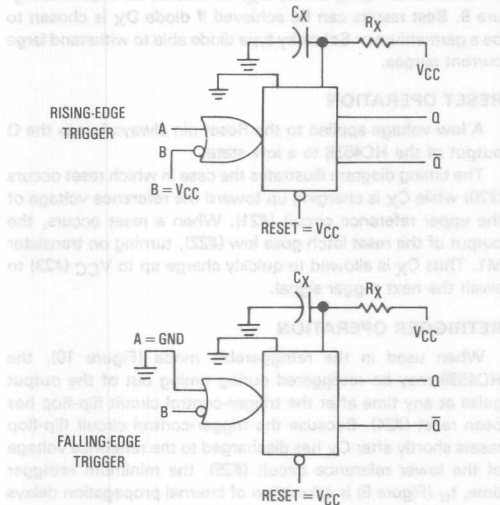


Figure 10. Retriggerable Monostable Circuitry

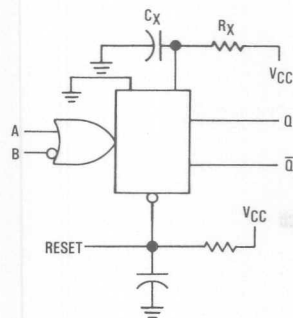


Figure 12. Elimination of Output Pulse Width During Power-Up

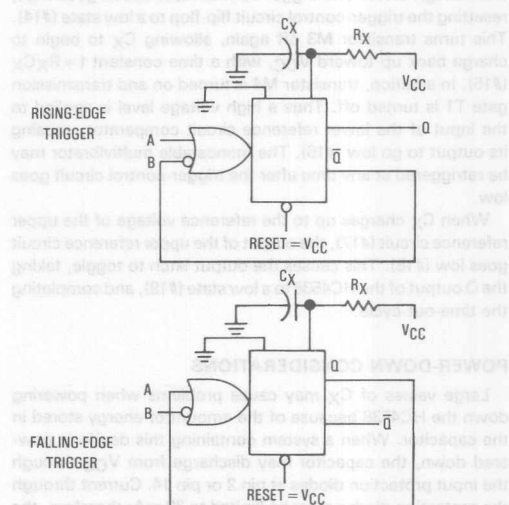
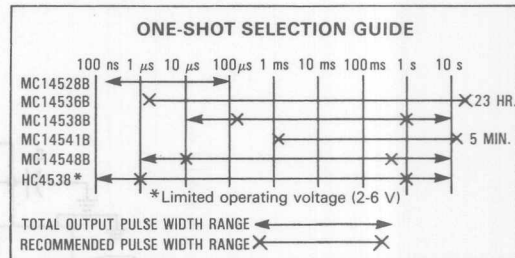


Figure 11. Nonretriggerable Monostable Circuitry



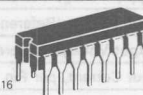
MC54/74HC4543

BCD-to-Seven-Segment Latch/ Decoder/Display Driver for LCDs

High-Performance Silicon-Gate CMOS

The MC54/74HC4543 is compatible in both function and pinout with the MC14543B metal-gate CMOS decoder/driver. This device is designed for use with liquid-crystal display (LCD) readouts. The HC4543 provides a 4-bit storage latch, a BCD-to-seven-segment decoder, and an LCD driver. The blanking input (BI) and latch enable (LE, active low) are used to blank the display and store the BCD code, respectively. A square wave is applied to the phase input (Ph) of the HC4543 and electrically common backplane of the LCD.

- Latch Storage of BCD Inputs
- Blanking Input
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 252 FETs or 63 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620



N SUFFIX
PLASTIC
CASE 648



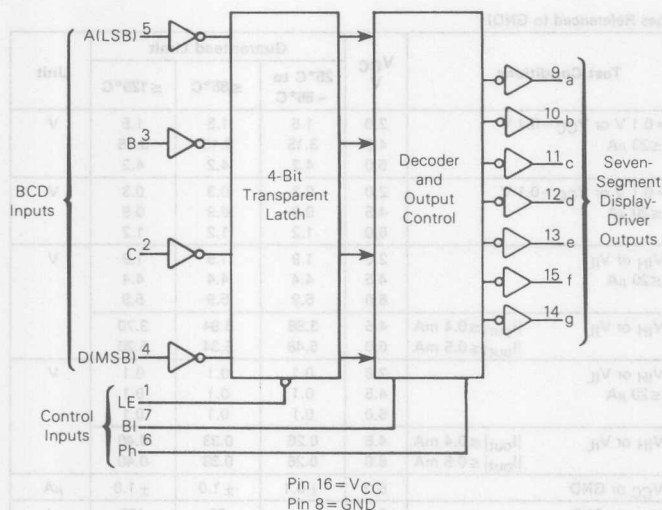
D SUFFIX
SOIC
CASE 751

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

BLOCK DIAGRAM

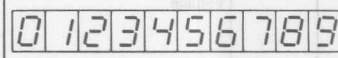


PIN ASSIGNMENT

LE	1	16	V_{CC}
C	2	15	f
B	3	14	g
D	4	13	e
A	5	12	d
Ph	6	11	c
BI	7	10	b
GND	8	9	a



DISPLAY



V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 3)	V _{CC} = 2.0 V 0 V _{CC} = 4.5 V 0 V _{CC} = 6.0 V 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 0.4 \text{ mA}$ $ I_{out} \leq 0.5 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 0.4 \text{ mA}$ $ I_{out} \leq 0.5 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4543

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 5)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	130	153	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, LE to Output (Figures 2 and 5)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	130	153	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, BI or Ph to Output (Figures 3 and 5)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	130	153	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	130	153	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

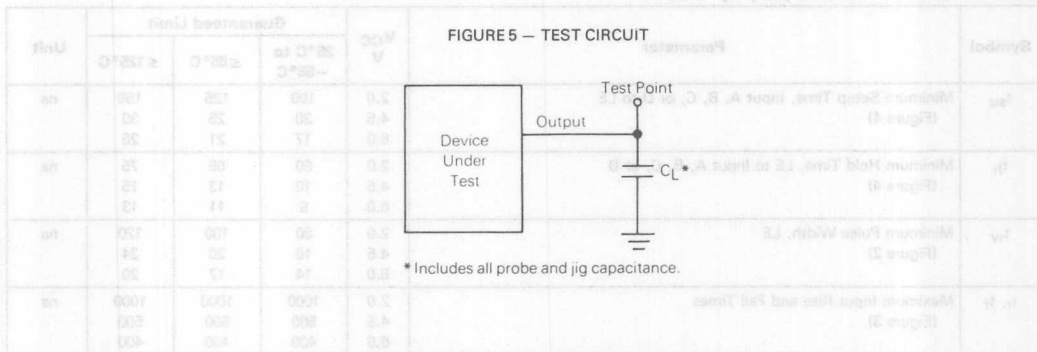
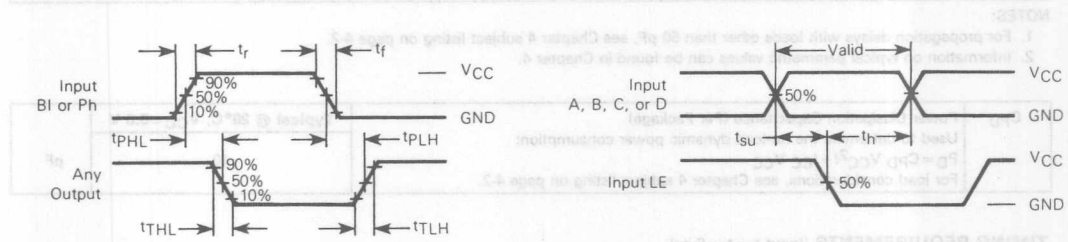
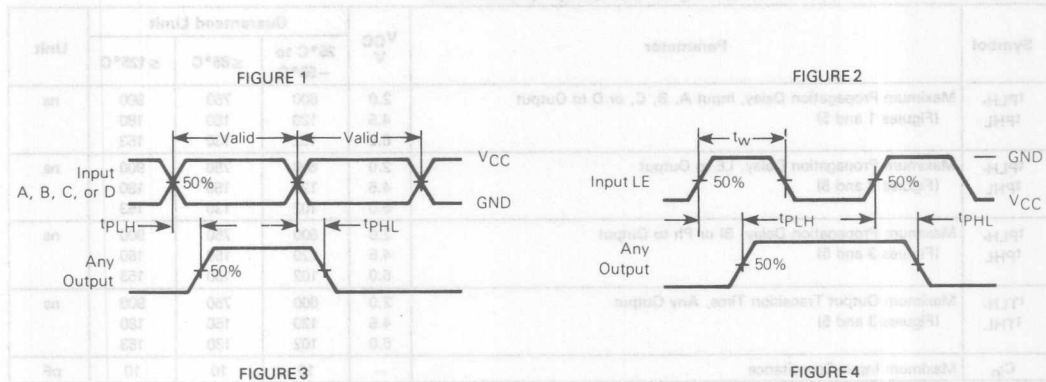
TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Input A, B, C, or D to LE (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, LE to Input A, B, C, or D (Figure 4)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _w	Minimum Pulse Width, LE (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 3)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC4543

SWITCHING WAVEFORMS



MC54/74HC4543

FUNCTION TABLE

Inputs						Outputs								
LE	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	L	L	0
H	L	L	L	L	L	H	L	H	L	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	L	2
H	L	L	L	L	H	H	H	H	H	L	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	L	H	L	H	H	L	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	L	H	L	L	H	H	H	L	L	H	H	9
H	L	L	L	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	L	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	L	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	L	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	**							**
†	†	H	†				Inverse of Output Combinations Above							Display as above

X = Don't care

† = Above Combinations

* = For liquid crystal readouts, apply a square wave to Ph.

** = Depends upon the code previously applied when LE = H

PIN DESCRIPTIONS

INPUTS

A, B, C, D (PINS 5, 3, 2, 4) — BCD inputs. These are the inputs to be decoded. The data on these pins is decoded to a seven-segment output when the LE pin is high and is latched when LE is low. For inputs greater than hexadecimal 9 or for BI input high, the output is blanked. A (pin 5) is the least-significant data bit and D (pin 4) is the most-significant data bit.

OUTPUTS

a, b, c, d, e, f, g (PINS 9, 10, 11, 12, 13, 15, 14) — Decoded seven-segment display-driver outputs. For liquid-crystal displays (LCD's), these outputs are tied directly to the LCD segment pins. For other type displays, see Figure 6.

CONTROL INPUTS

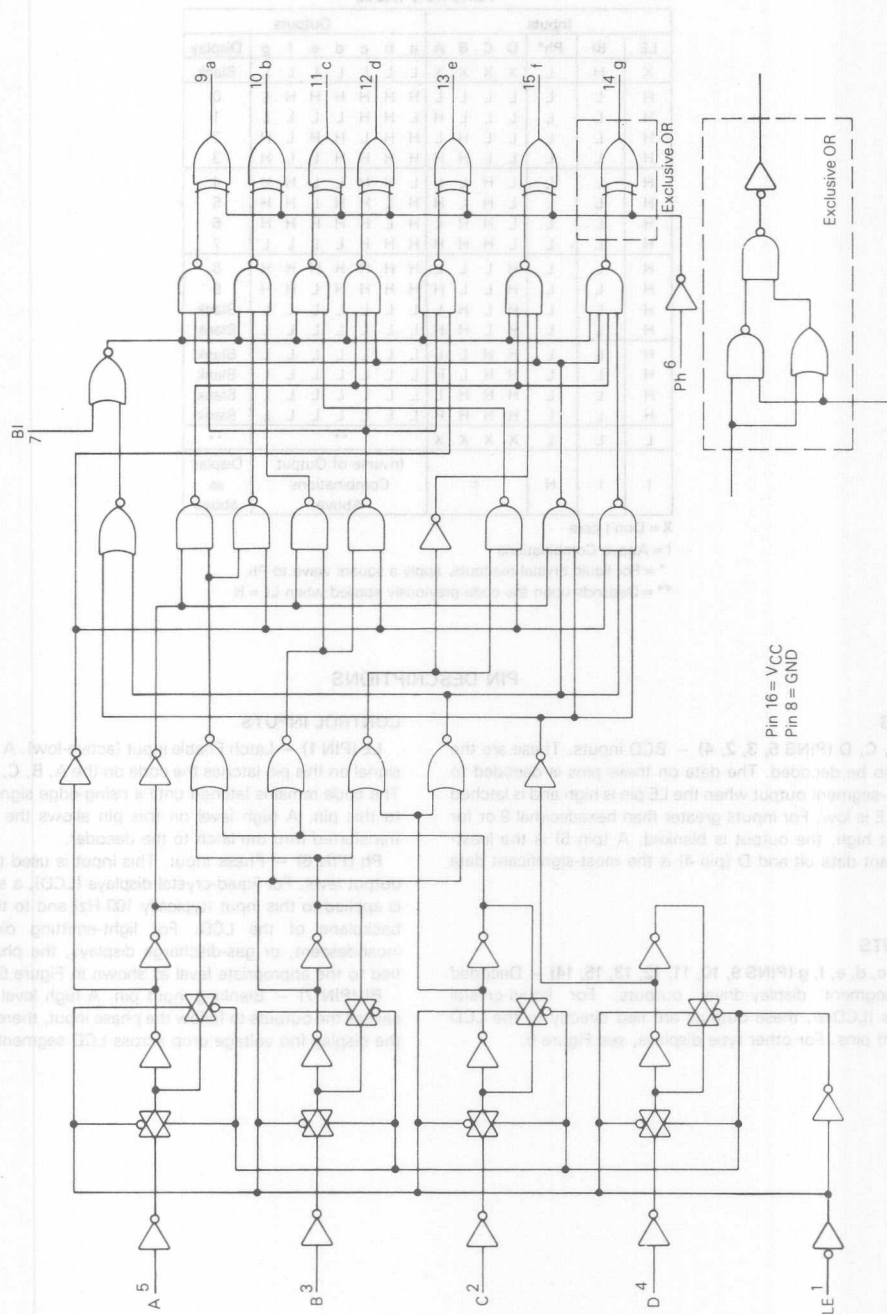
LE (PIN 1) — Latch Enable input (active-low). A falling-edge signal on this pin latches the code on the A, B, C, and D pins. The code remains latched until a rising-edge signal is applied to this pin. A high level on this pin allows the code to be transferred thru the latch to the decoder.

Ph (PIN 6) — Phase input. This input is used to invert the output level. For liquid-crystal displays (LCD), a square wave is applied to this input (typically 100 Hz) and to the common backplane of the LCD. For light-emitting diode (LED), incandescent, or gas-discharge displays, the phase input is tied to the appropriate level as shown in Figure 6.

BI (PIN 7) — Blanking input pin. A high level on this pin causes the outputs to follow the phase input, thereby blanking the display (no voltage drop across LCD segments).

MC54/74HC4543

EXPANDED LOGIC DIAGRAM



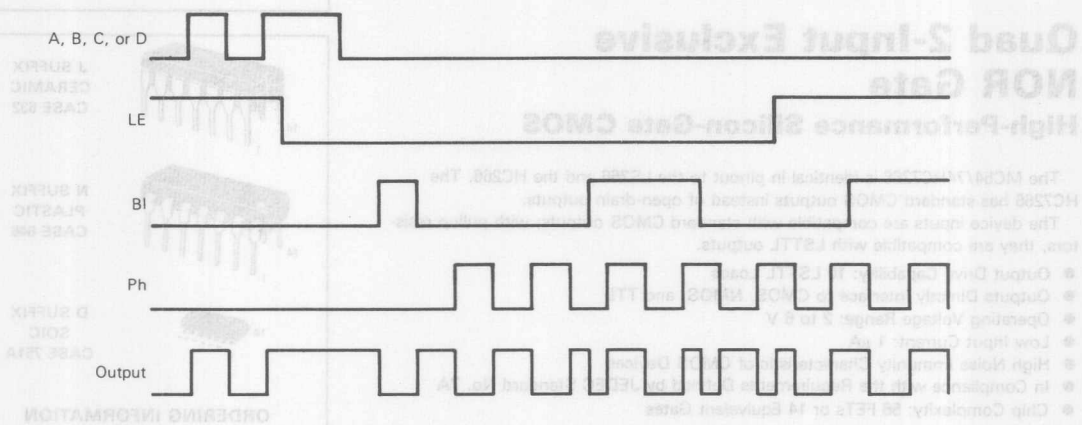
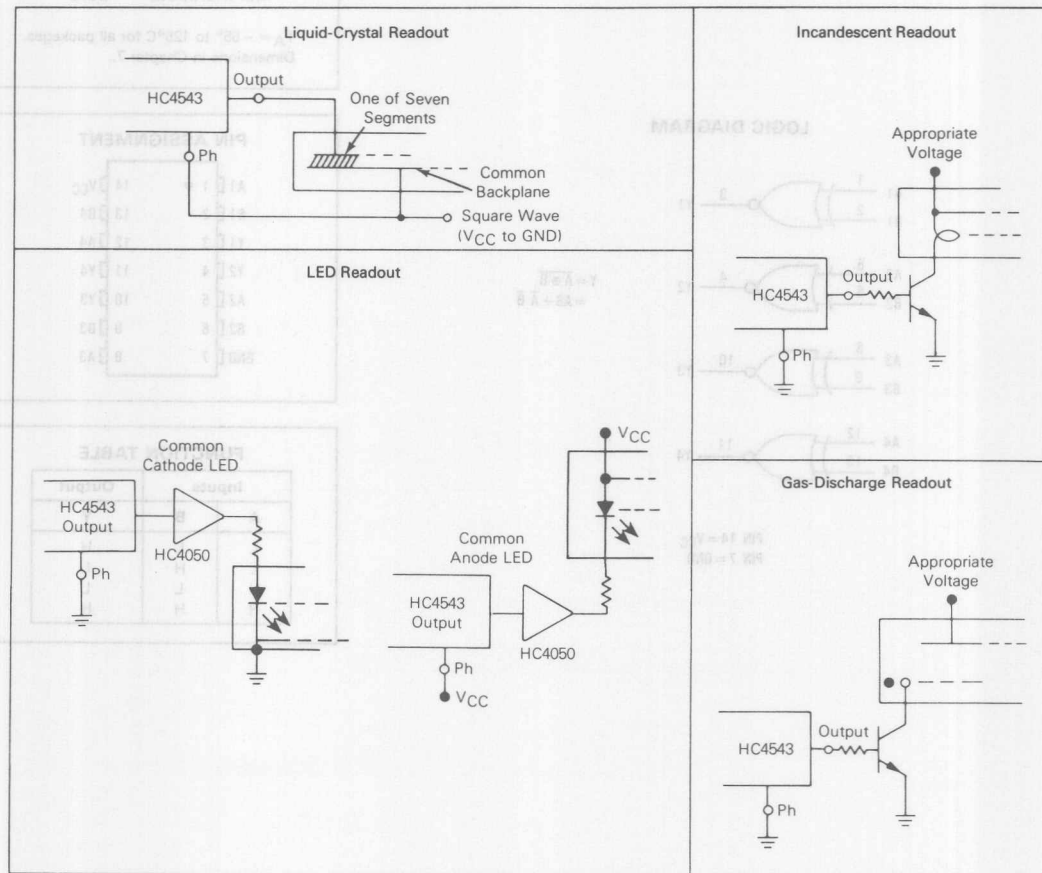


FIGURE 6 — CONNECTIONS TO VARIOUS DISPLAY READOUTS



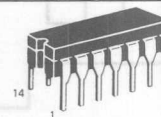
Quad 2-Input Exclusive NOR Gate

High-Performance Silicon-Gate CMOS

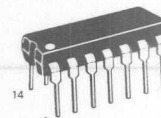
The MC54/74HC266 is identical in pinout to the LS266 and the HC266. The HC266 has standard CMOS outputs instead of open-drain outputs.

The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 56 FETs or 14 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632



N SUFFIX
PLASTIC
CASE 646



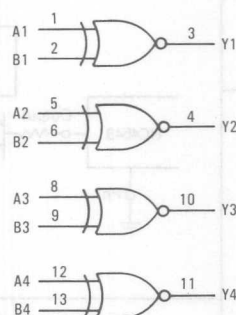
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAM



$$Y = A \oplus B \\ = AB + \bar{A}\bar{B}$$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
B1	2	13	B4
Y1	3	12	A4
Y2	4	11	Y4
A2	5	10	Y3
B2	6	9	B3
GND	7	8	A3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

MC54/74HC7266

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} ,V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC7266

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		33	

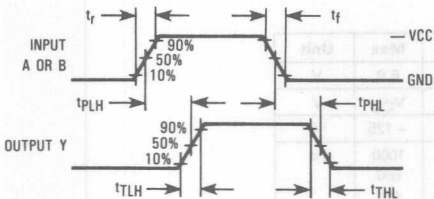


Figure 1. Switching Waveforms

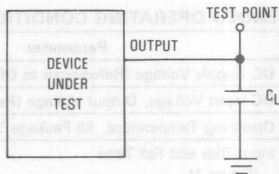
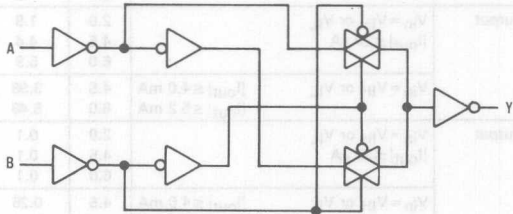


Figure 2. Test Circuit

5

LOGIC DETAIL
(1/4 of Device)



indicates a logic zero; a negative-going transition indicates a logic one (see Figure 4).

The Bi ϕ -L signal must be phase coherent (i.e., no glitches). Therefore, NRZ-L and clock transitions must be coincident.

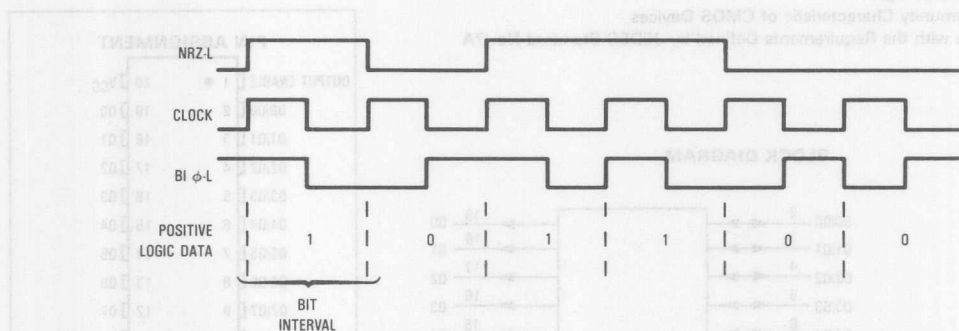
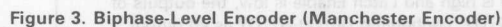


Figure 4. Timing Diagram

Product Preview

Octal 3-State Noninverting Transparent Latch with Readback

High-Performance Silicon-Gate CMOS

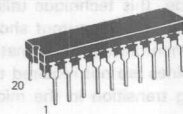
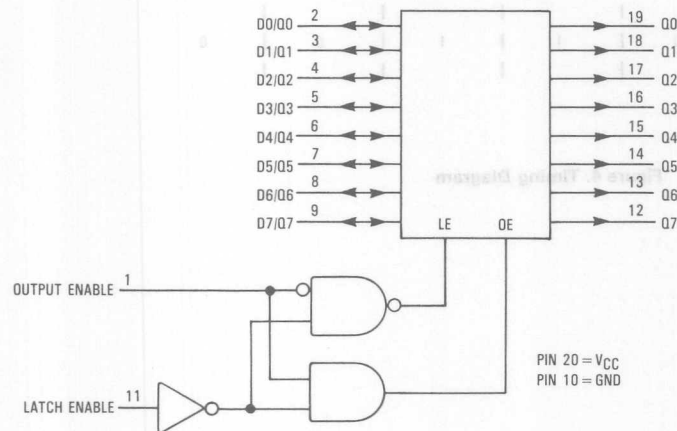
The MC54/74HC793 consists of eight noninverting transparent latches with read-back. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable and Output Enable are low. Data meeting the setup and hold time is latched when either Latch Enable or Output Enable is high.

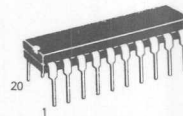
The HC7793 can enable its output data back onto its input bus via the I/O port configuration. Output Enable and Latch Enable determine how pins D0/Q0-D7/Q7 are configured. When Output Enable is high and Latch Enable is low, the outputs of the latches are enabled on D0/Q0-D7/Q7, configuring D0/Q0-D7/Q7 as an output bus so that the output data can be read back by the host.

- Output Drive Capability: 10 LSTTL Loads (Q0-Q7)
15 LSTTL Loads (D0/Q0-D7/Q7)
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A

BLOCK DIAGRAM



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

OUTPUT ENABLE	1	20	V_{CC}
D0/Q0	2	19	Q0
D1/Q1	3	18	Q1
D2/Q2	4	17	Q2
D3/Q3	5	16	Q3
D4/Q4	6	15	Q4
D5/Q5	7	14	Q5
D6/Q6	8	13	Q6
D7/Q7	9	12	Q7
GND	10	11	LATCH ENABLE

FUNCTION TABLE

Inputs			Outputs	
Output Enable	Latch Enable	D/Q	D/Q	Q
L	L	L	Input	L
L	L	H	Input	H
L	H	X	Input	Q*
H	L	Output	Q*	Q*
H	H	X	Input	Q*

*Q represents the previous latched state.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74HC7793

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin (Pins 1, 11)	± 20	mA
I_{out}	DC Output Current, per Pin (Pins 12-19)	± 25	mA
$I_{I/O}$	DC Output Current, per Pin (Pins 2-9)	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} ,V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} Pins 2-9 $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
		$V_{in} = V_{IH}$ or V_{IL} Pins 12-19 $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} Pins 2-9 $ I_{out} \leq 6.0$ mA $ I_{out} \leq 7.8$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
		$V_{in} = V_{IH}$ or V_{IL} Pins 12-19 $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μ A
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10.0	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	6.0	8	80	160	μ A

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

MC54/74HC7793

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input Data to Q (Figures 1 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable or Output Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Latch Enable or Output Enable to D0/Q0-D7/Q7 (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Latch Enable or Output Enable to D0/Q0-D7/Q7 (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, D0/Q0-D7/Q7	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q0-Q7 (Figures 1 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance (Pins 1, 11)	—	10	10	10	pF
C _{out}	Maximum I/O Capacitance (I/O in High-Impedance State)	—	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		TBD	

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, Input Data to Latch Enable (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Latch Enable to Input Data (Figure 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC7793

SWITCHING WAVEFORMS

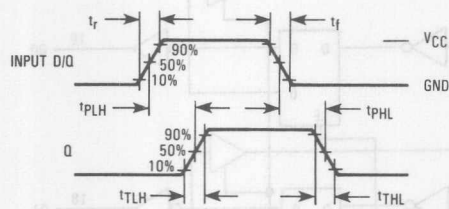


Figure 1

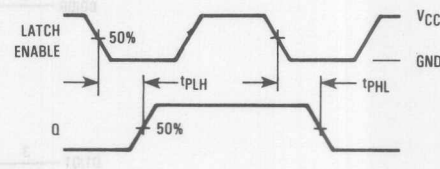


Figure 2

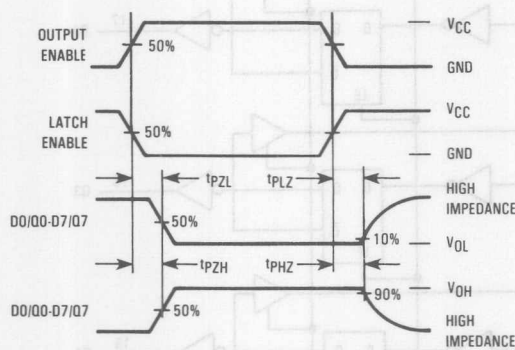


Figure 3

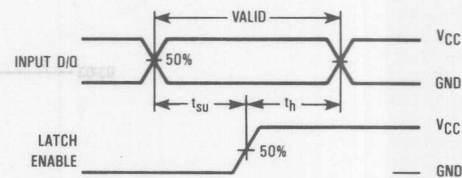
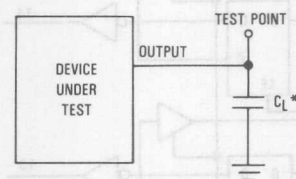
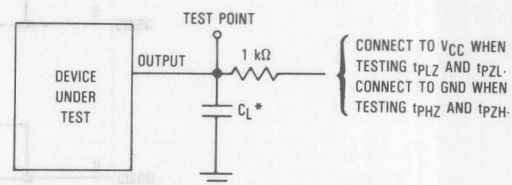


Figure 4



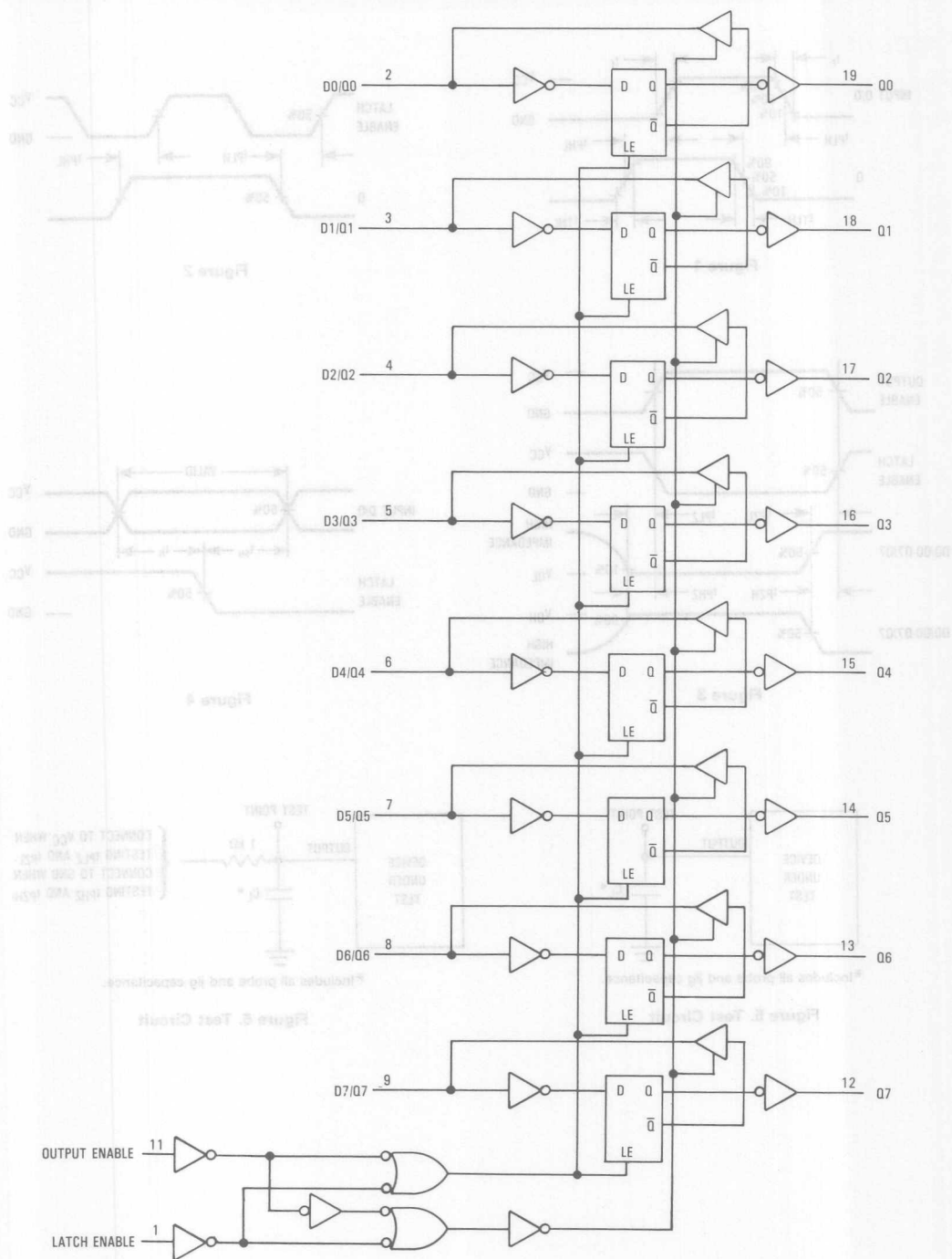
*Includes all probe and jig capacitance.

Figure 5. Test Circuit



*Includes all probe and jig capacitance.

Figure 6. Test Circuit



Product Preview

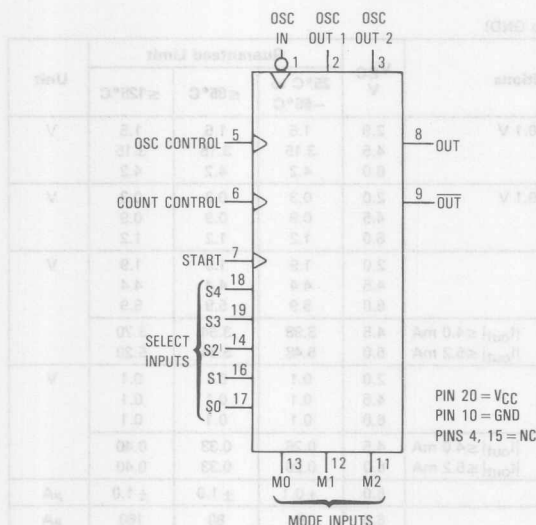
Programmable Timer

High-Performance Silicon-Gate CMOS

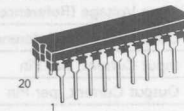
The MC54/74HC9000 is a precision programmable timer that, when used in conjunction with a 32 kHz to 20 MHz crystal, can provide time durations from 4.2 minutes to 100 ns. Using the on-chip oscillator function and external RC components, even longer time durations can be obtained. Both true and complementary outputs are available for use with the edge-sensitive oscillator control and count control. These control pins facilitate several timer and "one-shot" type configurations (see Application Information).

- Has On-Chip Crystal or RC Oscillator Capability; or may be Driven by External Frequency Source
- More Accurate than Monostable Multivibrators when used with a Crystal
- Low Power Consumption Characteristic of CMOS Devices
- Wide Operating Voltage Range: 2.5 to 6 Volts
- OUT and $\overline{\text{OUT}}$ Drive Capability: 10 LSTTL Loads
- High Noise Immunity Characteristics of CMOS Devices
- Very Low Power Consumption in Standby Mode
- Double Diode Protection on all Inputs
- Divide Range of 2 to 2²⁴
- Select Inputs (S0, S1, S2, S3, S4) Facilitate Programming and Incoming Inspection
- Mode Inputs (M0, M1, M2) for Functional Versatility
- Chip Complexity: 923 FETs or 231 Equivalent Gates

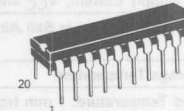
LOGIC DIAGRAM



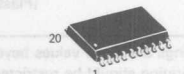
MC54/74HC9000



J SUFFIX
 CERAMIC
 CASE 732



N SUFFIX
 PLASTIC
 CASE 738



DW SUFFIX
 SOIC
 CASE 751D

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

T_A = -55° to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT

OSC IN	1	20	VCC
OSC OUT 1	2	19	S3
OSC OUT 2	3	18	S4
NC	4	17	S0
OSC CONTROL	5	16	S1
COUNT CONTROL	6	15	NC
START	7	14	S2
OUT	8	13	M0
$\overline{\text{OUT}}$	9	12	M1
GND	10	11	M2

NC = NO CONNECTION

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.5*	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2.0 V	0	1000	ns
	Except OSC IN and START (Figure 1)	V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	
		Input Rise and Fall Time (OSC IN or START)	0	No Limit	

*The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 1 with an external clock source.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage (OUT, $\overline{\text{OUT}}$)	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage (OUT, $\overline{\text{OUT}}$)	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND, $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC9000

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Projected Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (Modes 1-7) (50% Duty Cycle) (Figures 1 and 2)	2.0	4.0	3.2	2.6	MHz
		4.5	20	16	13	
		6.0	24	19	15	
f _{max}	Maximum Clock Frequency (Mode 0) (50% Duty Cycle) (Figures 1 and 2)	2.0	2.0	1.6	1.3	MHz
		4.5	10	8.0	6.7	
		6.0	11.8	9.4	7.9	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, OSC IN to OUT or $\overline{\text{OUT}}$ (One Stage Selected) (Figures 1 and 2)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, START to OUT or $\overline{\text{OUT}}$ (One Shot Mode) (Figures 3 and 2)	2.0	250	315	375	ns
		4.5	50	63	75	
		6.0	43	54	64	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		TBD	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Projected Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, S0-S4 or M0-M2 to START (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _d	Minimum Delay Time, START to OUT or $\overline{\text{OUT}}$ (Figure 3)	2.0	500	625	750	ns
		4.5	100	125	150	
		6.0	85	106	128	
t _b	Minimum Burst Time, Count Control (Figure 3)	2.0	500	625	750	ns
		4.5	100	125	150	
		6.0	85	106	128	
t _w	Minimum Pulse Width, START (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, OSC IN (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, OUT or $\overline{\text{OUT}}$ (One-Shot Mode) (Figure 3)	2.0	500	625	750	ns
		4.5	100	125	150	
		6.0	85	106	128	
t _w	Minimum Pulse Width, OUT or $\overline{\text{OUT}}$ (Delayed Multiple Pulse Mode) (Figure 3)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _r , t _f	Maximum Input Rise and Fall Times, Except OSC IN or START	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	
t _r , t _f	Maximum Input Rise and Fall Times, OSC IN or START (Figure 1)	—	No Limit			—

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

OSC IN, OSC OUT 1, OSC OUT 2 (Pins 1, 2, 3)

These pins, used in conjunction with external components, form an on-chip reference oscillator. The frequency of this oscillator and the number of counters selected determines the amount of time-out desired (see Figures 7 and 8). An external generator may be used instead of the internal oscillator. In this case, the signal should swing from ground to V_{CC} and should be fed into OSC IN. OSC OUT 1 and OSC OUT 2 must be left floating (see Figure 9). With the crystal oscillator configuration shown in Figure 7, OSC OUT 2 must be left open-circuited.

OSC CONTROL (Pin 5)

This pin is used to enable or disable the oscillator. A low-to-high transition on this pin resets all counters and shuts down the oscillator. This puts the device into a low-power standby condition.

COUNT CONTROL (Pin 6)

A low-to-high transition on this pin also resets all counters. The oscillator continues to run, but the counters do not increment. This condition eliminates oscillator start-up delay time.

START (Pin 7)

A low-to-high transition on this pin causes the oscillator to start up, if previously disabled, and timing begins. The START

pin, when using only one or two stages of delay, it is recommended that an external time base, synchronized with the start pulse, be used. With no synchronization, a start pulse occurring when the clock is high produces a different initial delay than when the start pulse occurs when the clock is low. This effect causes less error as more delay stages are selected.

M0, M1, M2 (Pins 13, 12, 11)

Mode inputs. These pins determine the timer's mode of operation (see Table 1).

S0, S1, S2, S3, S4 (Pins 17, 16, 14, 19, 18)

Select inputs. These pins select the exact divide ratio desired (see Table 2).

OUT (Pin 8)

This pin is the output of the timer. OUT can be fed back to either OSC CONTROL or COUNT CONTROL to inhibit counting.

OUT (Pin 9)

\overline{OUT} is the complement of OUT. \overline{OUT} can also be fed back to OSC CONTROL or COUNT CONTROL to inhibit counting.

NC (Pins 4, 15)

No connect pins. These pins are not connected internally.

Table 1. Output Mode Selection Table

Mode	Mode Inputs			Output Pulse Description	Figure
	M2	M1	M0		
0	0	0	0	Delayed Pulse ($t_W = 1/2f$)	11, 13
1	0	0	1	Delayed Pulse ($t_W = 2/f$)	11, 13
2	0	1	0	Delayed Pulse ($t_W = 8/f$)	11, 13
3	0	1	1	Monostable Multivibrator	10
4	1	0	0	Delayed Burst Pulse ($t_W = 1/2f$) $t_{delay} = t_{burst}$	14
5	1	0	1	Delayed Burst Pulse ($t_W = 2/f$) $t_{delay} = t_{burst}$	14
6	1	1	0	Delayed Burst Pulse ($t_W = 8/f$) $t_{delay} = t_{burst}$	14
7	1	1	1	Programmable Counter or Test Mode (50% Output Duty Cycle)	12, 15, 17

MC54/74HC9000

Table 2. Select Divide Range

Select Inputs					Number of Counter Stages Selected, N ($\div 2N$)
S4	S3	S2	S1	S0	
0	0	0	0	0	1
0	0	0	0	1	2
0	0	0	1	0	3
0	0	0	1	1	4
0	0	1	0	0	5
0	0	1	0	1	6
0	0	1	1	0	7
0	0	1	1	1	8
0	1	0	0	0	9
0	1	0	0	1	10
0	1	0	1	0	11
0	1	0	1	1	12
0	1	1	0	0	13
0	1	1	0	1	14
0	1	1	1	0	15
0	1	1	1	1	16

Select Inputs					Number of Counter Stages Selected, N ($\div 2N$)
S4	S3	S2	S1	S0	
1	0	0	0	0	17
1	0	0	0	1	18
1	0	0	1	0	19
1	0	0	1	1	20
1	0	1	0	0	21
1	0	1	0	1	22
1	0	1	1	0	23
1	0	1	1	1	24
1	1	0	0	0	1*
1	1	0	0	1	2*
1	1	0	1	0	3*
1	1	0	1	1	4*
1	1	1	0	0	5*
1	1	1	0	1	6*
1	1	1	1	0	7*
1	1	1	1	1	8*

*Configured internally such that the 24 stage counter is parallel clocked as three 8-bit counters. This allows for shorter incoming inspection testing times.

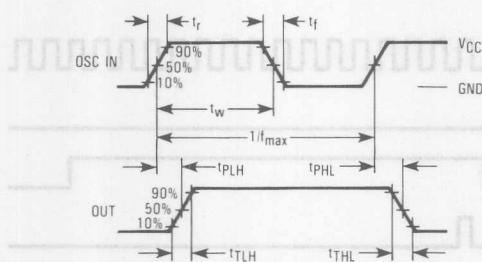
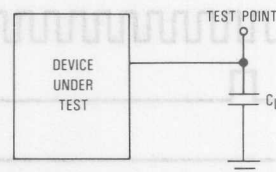


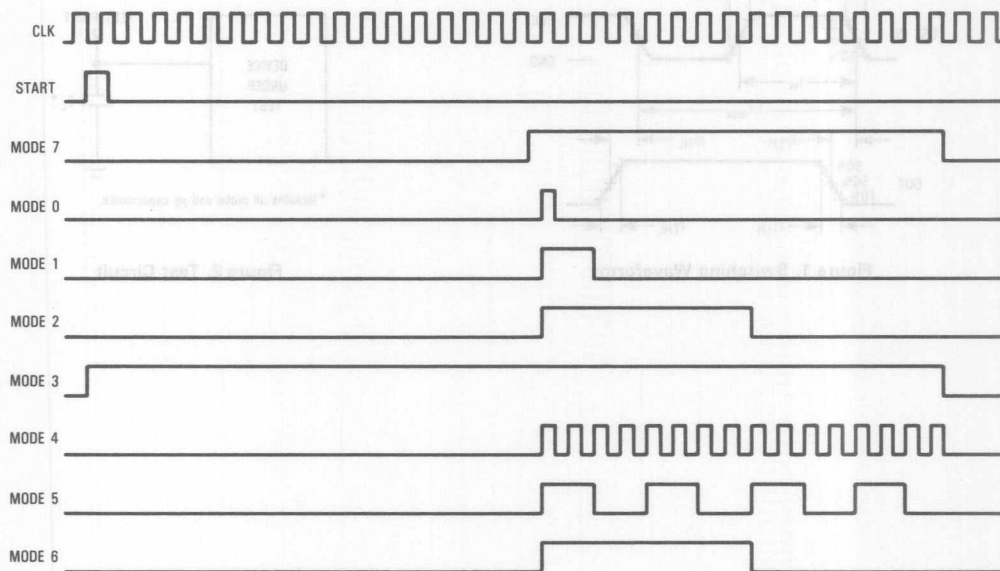
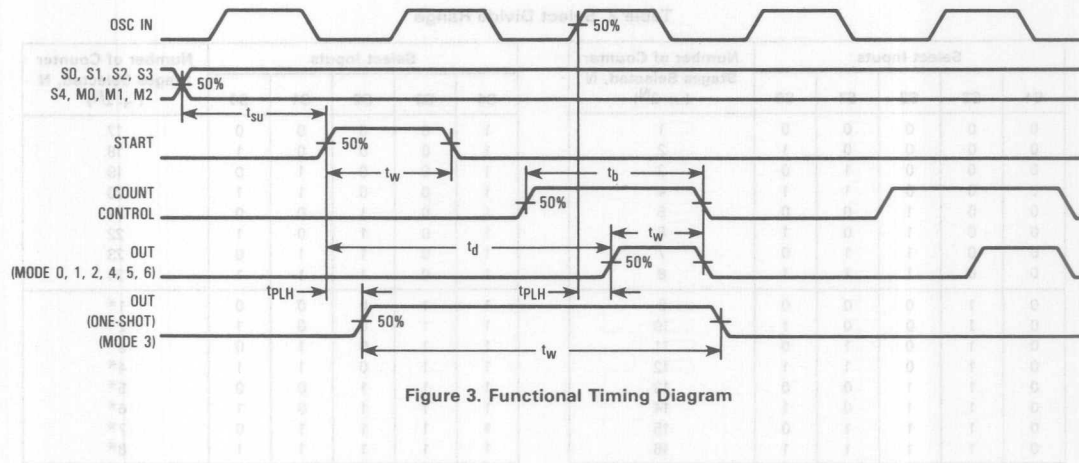
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

MC54/74HC9000



NOTE: Five stages of delay counter selected (S4, S3, S2, S1, S0 = 00100).

Figure 4. Timing Diagram Using Feedback

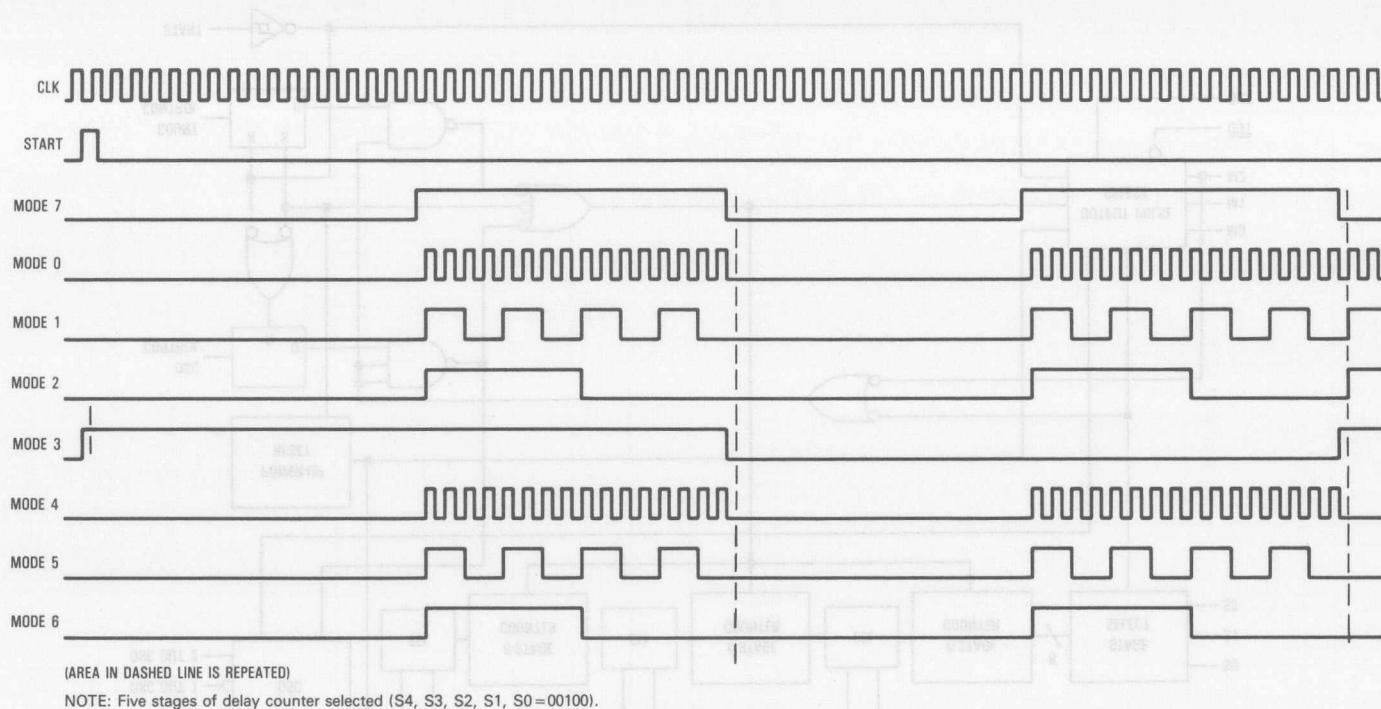


Figure 5. Timing Diagram Using No Feedback

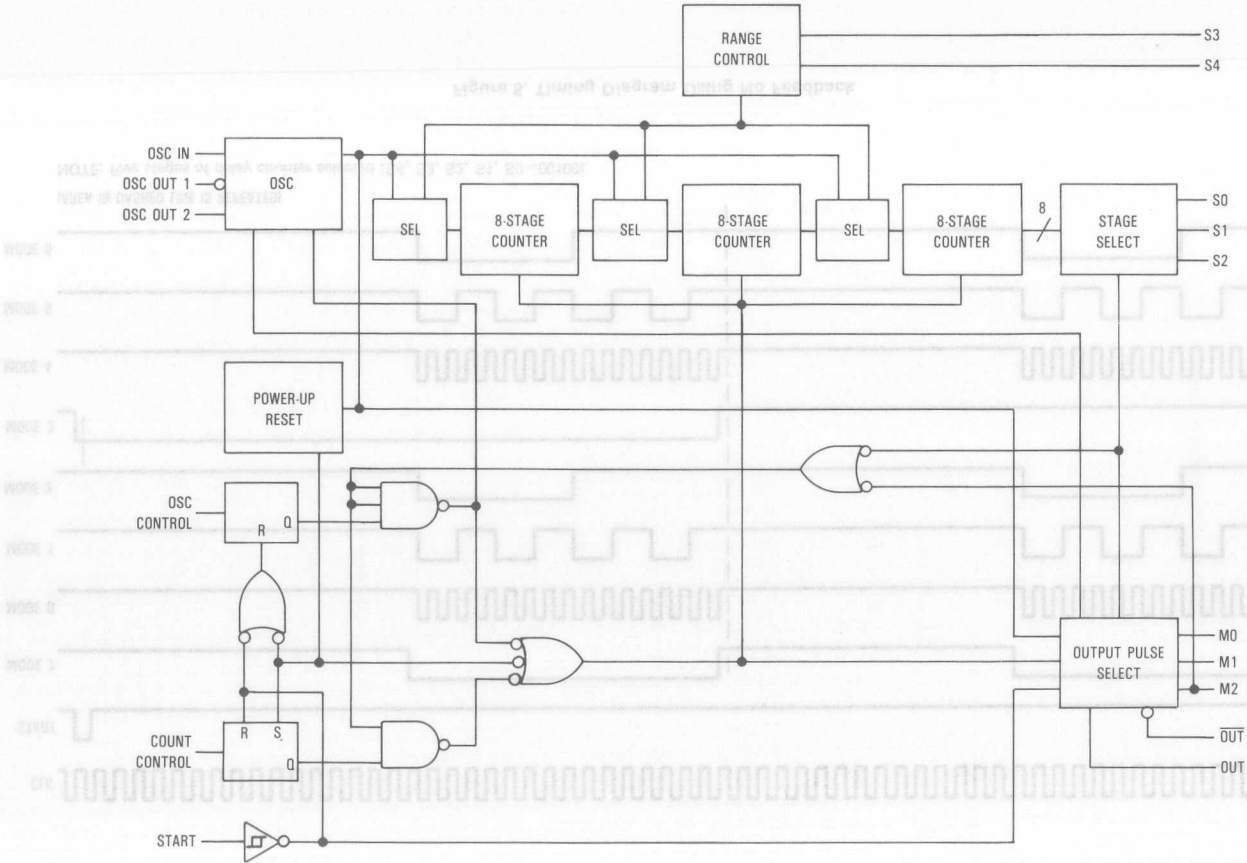


Figure 6. Block Diagram

MC54/74HC9000

OSCILLATOR DESIGN INFORMATION

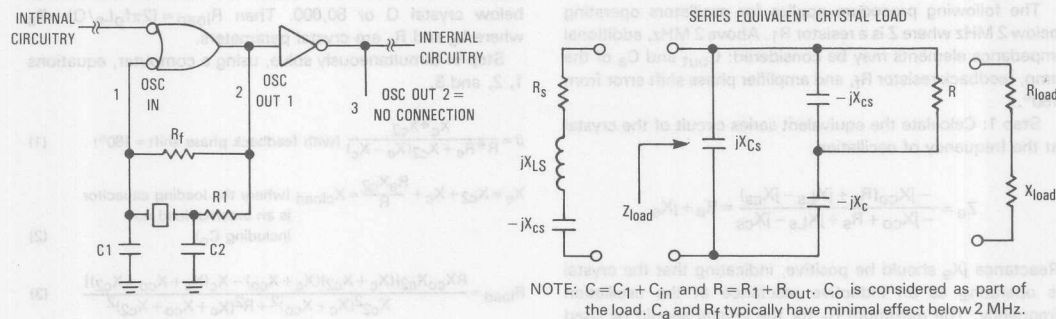
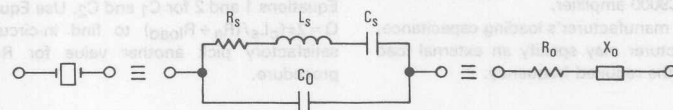
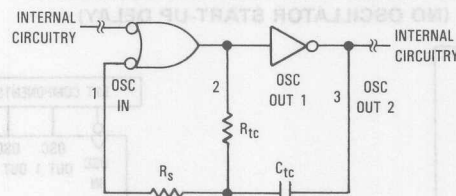


Figure 7. Pierce Oscillator

EQUIVALENT CIRCUIT FOR CRYSTAL NEAR RESONANCE



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).



$$10 R_{tc} > R_s > 2 R_{tc}$$

$$400 \text{ Hz} \leq f \leq 400 \text{ kHz}$$

$$f = \frac{1}{2.3 R_{tc} C_{tc}} \quad (\text{f in Hz, } R_{tc} \text{ in ohms, } C_{tc} \text{ in farads})$$

The formula may vary for other frequencies.

Figure 8. RC Oscillator

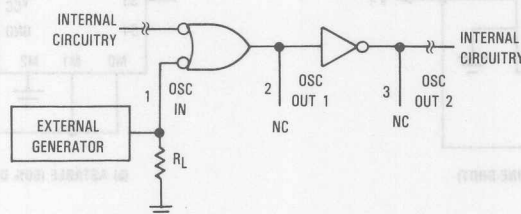


Figure 9. External Generator

DESIGN PROCEDURE

The following procedure applies for oscillators operating below 2 MHz where Z is a resistor R_1 . Above 2 MHz, additional impedance elements may be considered: C_{out} and C_a of the amp, feedback resistor R_f , and amplifier phase shift error from 180° .

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{co}(R_s + jX_{Ls} - jX_{Cs})}{-jX_{co} + R_s + jX_{Ls} - jX_{Cs}} = R_e + jX_e$$

Reactance jX_e should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R_s for the crystal should be used in the equation.

Step 2: Determine β , the attenuation, of the feedback network. For a closed loop gain of 2, $A_V\beta = 2$, $\beta = 2/A_V$ where A_V is the gain of the HC9000 amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: a manufacturer may specify an external load capacitance of 32 pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R_{load} . For example: a manufacturer specifies a crystal Q of 100,000. The desired in-circuit Q is set at 20% below crystal Q or 80,000. Then $R_{load} = (2\pi f_0 L_s / Q) - R_s$ where L_s and R_s are crystal parameters.

Step 5: Simultaneously solve, using a computer, equations 1, 2, and 3.

$$\beta = \frac{X_c * X_{c2}}{R * R_e + X_{c2}(X_e - X_c)} \quad (\text{with feedback phase shift} = 180^\circ) \quad (1)$$

$$X_e = X_{c2} + X_c + \frac{R_e X_{c2}}{R} = X_{load} \quad (\text{where the loading capacitor is an external load not including } C_o) \quad (2)$$

$$R_{load} = \frac{RX_{co}X_{c2}[(X_c + X_{c2})(X_c + X_{co}) - X_c(X_c + X_{co} + X_{c2})]}{X_{c2}^2(X_c + X_{co})^2 + R^2(X_c + X_{co} + X_{c2})^2} \quad (3)$$

Here $R = R_{out} + R_1$. R_{out} is amp output resistance, R_1 is Z. The C corresponding to X_c is given by $C = C_1 + C_{in}$.

Alternately, pick a value for R_1 (i.e. let $R_1 = R_s$). Solve Equations 1 and 2 for C_1 and C_2 . Use Equation 3 and the fact $Q = 2\pi f_0 L_s / (R_s + R_{load})$ to find in-circuit Q. If Q is not satisfactory pick another value for R_1 and repeat the procedure.

APPLICATIONS INFORMATION

APPLICATIONS WITH FREE-RUN OSCILLATOR (NO OSCILLATOR START-UP DELAY)

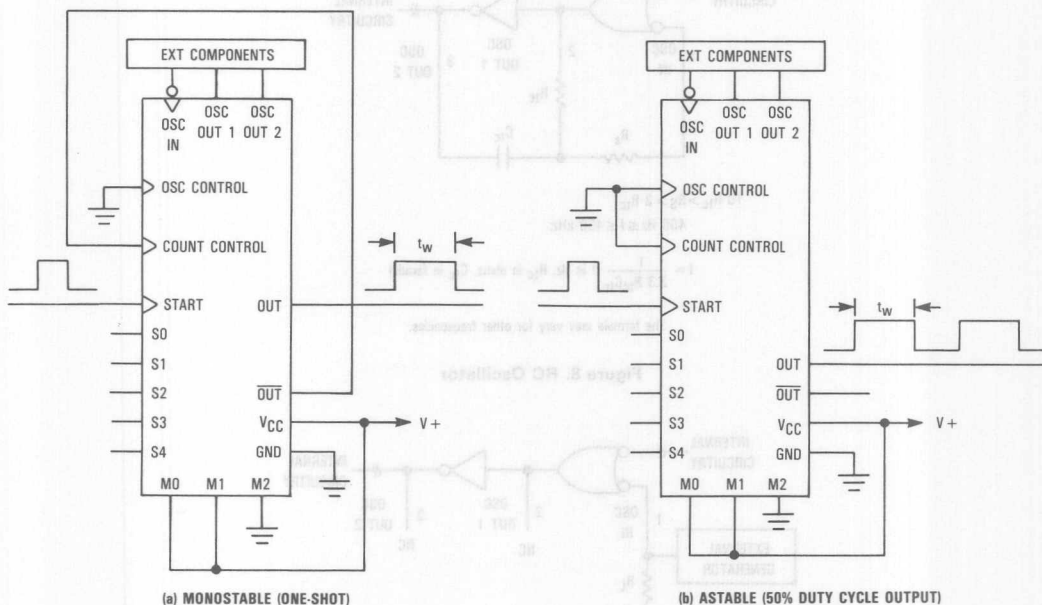
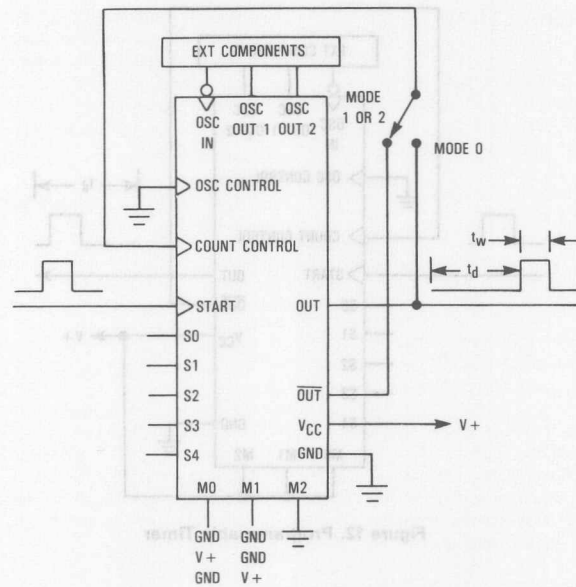
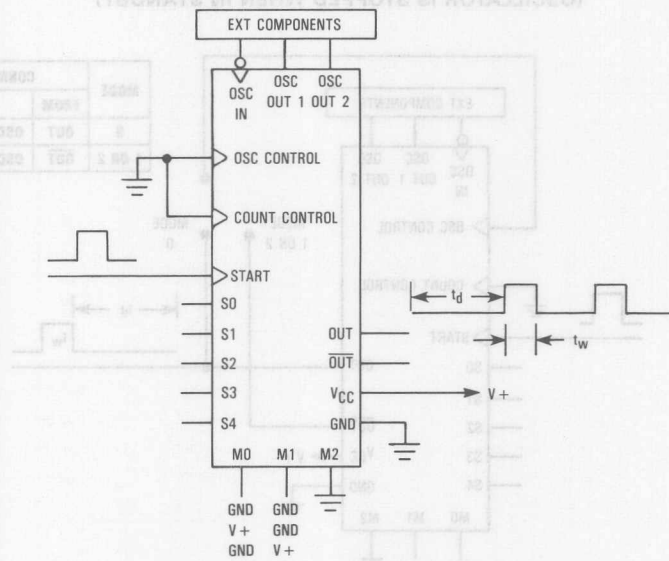


Figure 10. Multivibrator Configurations

MC54/74HC9000



(a) DELAYED SINGLE PULSE



(b) DELAYED MULTIPLE PULSE

Figure 11. Delayed Pulse Configurations

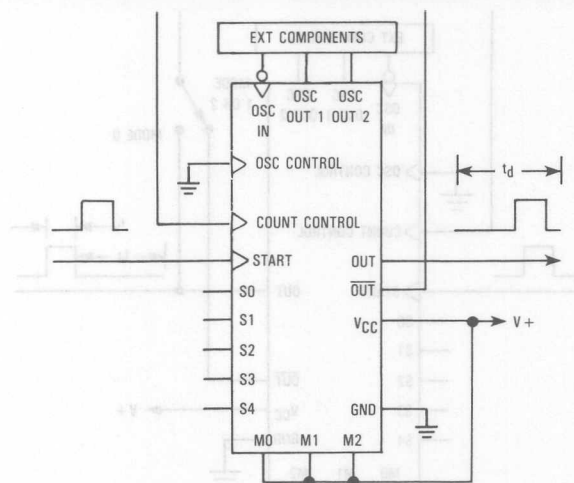


Figure 12. Programmable Timer

LOW STANDBY POWER APPLICATIONS (OSCILLATOR IS STOPPED WHEN IN STANDBY)

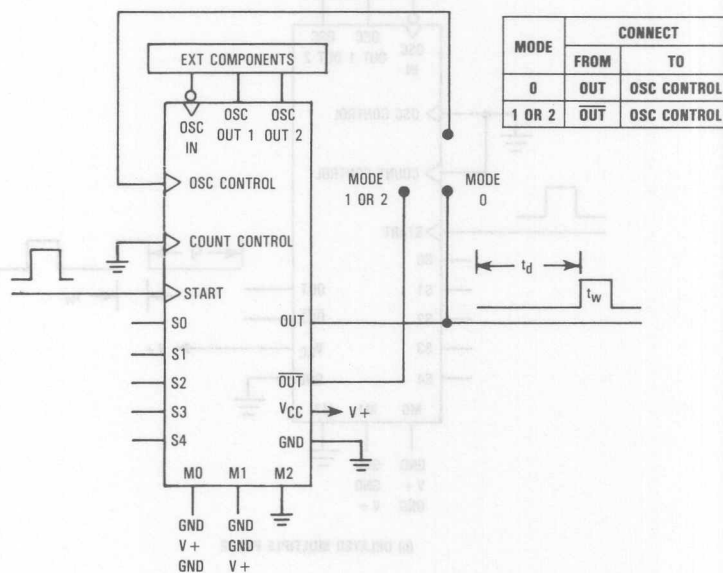


Figure 13. Delayed Single-Pulse Configuration

MC54/74HC9000

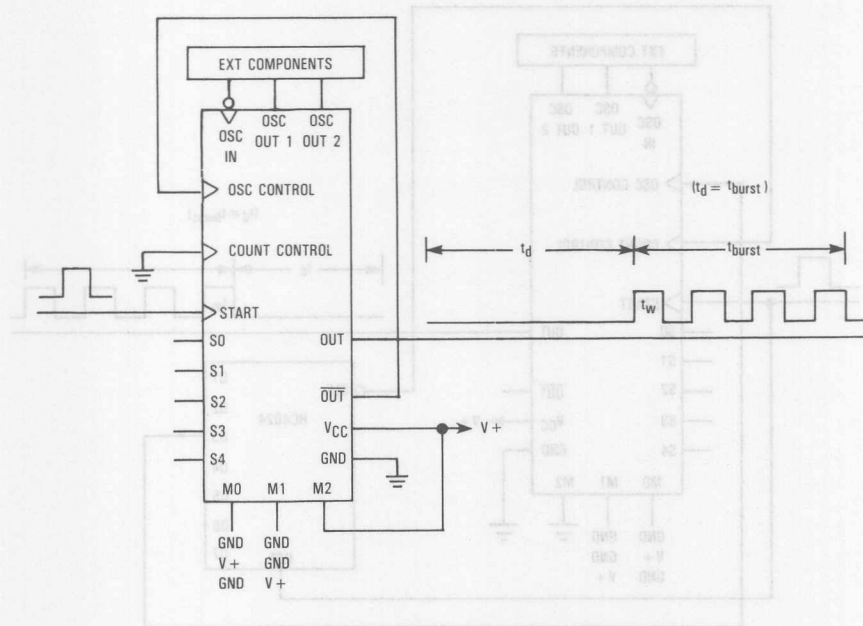


Figure 14. Burst Delayed-Pulse Configuration

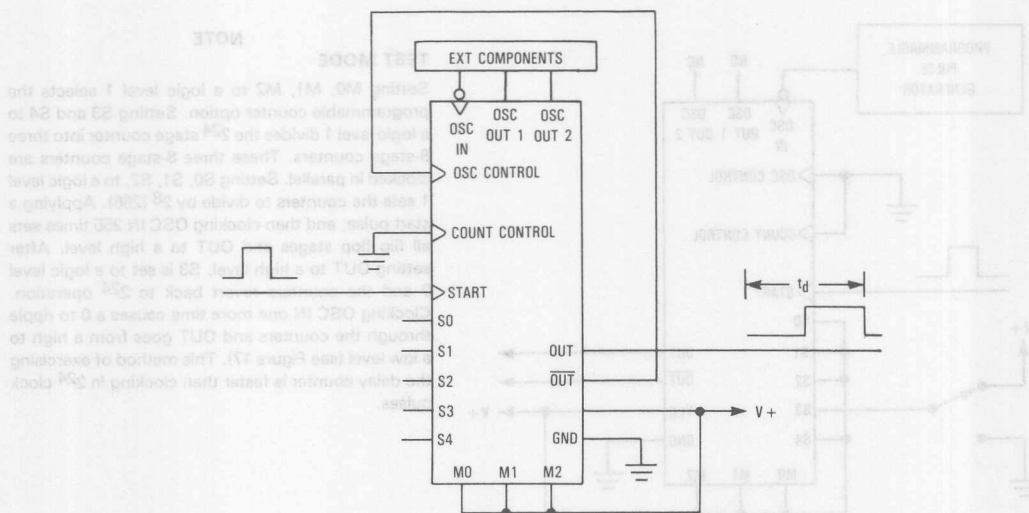


Figure 15. Programmable Timer

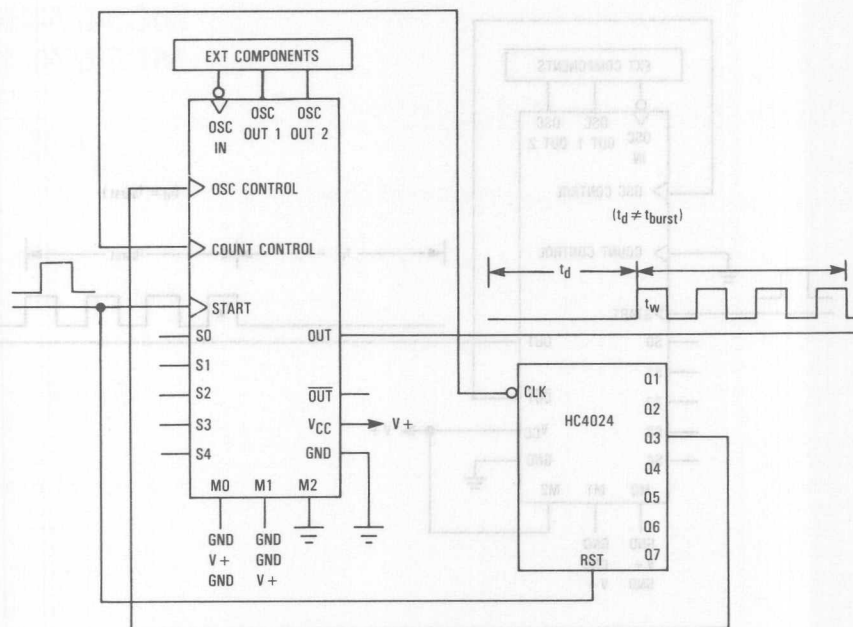


Figure 16. Delayed Multiple Pulse Configuration
(4-Pulse Configured)

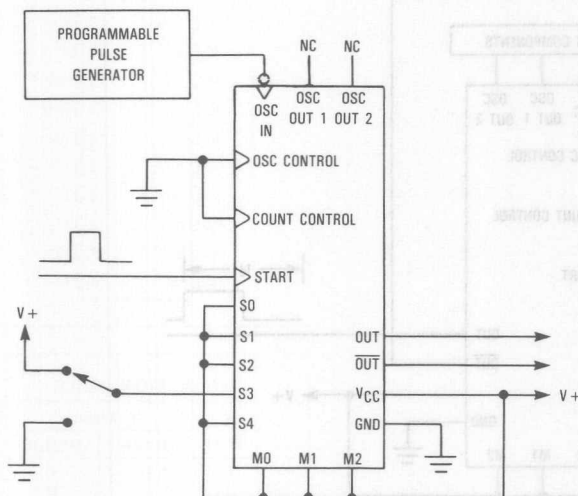


Figure 17. Test Mode (2^8 Divider Configuration)

NOTE

TEST MODE

Setting M0, M1, M2 to a logic level 1 selects the programmable counter option. Setting S3 and S4 to a logic level 1 divides the 2^{24} stage counter into three 8-stage counters. These three 8-stage counters are clocked in parallel. Setting S0, S1, S2, to a logic level 1 sets the counters to divide by 2^8 (256). Applying a start pulse, and then clocking OSC IN 255 times sets all flip flop stages and OUT to a high level. After setting OUT to a high level, S3 is set to a logic level 0 and the counters revert back to 2^{24} operation. Clocking OSC IN one more time causes a 0 to ripple through the counters and OUT goes from a high to a low level (see Figure 17). This method of exercising the delay counter is faster than clocking in 2^{24} clock pulses.

Product Preview

Nine-Wide Schmitt-Trigger Buffers

High-Performance Silicon-Gate CMOS

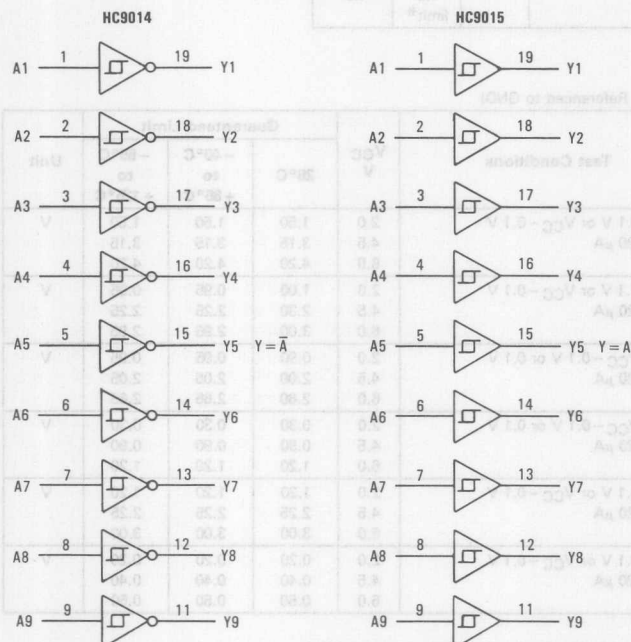
The MC54/74HC9014 consists of nine inverting Schmitt-Trigger Buffers, and the MC54/74HC9015 consists of nine noninverting Schmitt-Trigger Buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices have hysteresis and can, therefore, be used to enhance noise immunity or to square up slowly changing waveforms.

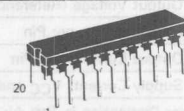
Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 90 FETs or 22.5 Equivalent Gates (HC9014)
108 FETs or 27 Equivalent Gates (HC9015)

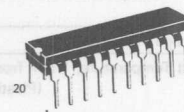
LOGIC DIAGRAMS



MC54/74HC9014 MC54/74HC9015



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

A1	1	20	V_{CC}
A2	2	19	Y1
A3	3	18	Y2
A4	4	17	Y3
A5	5	16	Y4
A6	6	15	Y5
A7	7	14	Y6
A8	8	13	Y7
A9	9	12	Y8
GND	10	11	Y9

FUNCTION TABLE

A Inputs	Y Outputs	
	HC9014	HC9015
L	H	L
H	L	H

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	no limit*	ns

*When $V_{in} = 0.5 V_{CC}$, $I_{CC} > >$ quiescent current.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C	-40°C to +85°C	-55°C to +125°C	
V_{T+max}	Maximum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V_{T+min}	Minimum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.00 2.30 3.00	0.95 2.25 2.95	0.95 2.25 2.95	V
V_{T-max}	Maximum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1 \text{ V or } 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.90 2.00 2.60	0.95 2.05 2.65	0.95 2.05 2.65	V
V_{T-min}	Minimum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1 \text{ V or } 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.30 0.90 1.20	0.30 0.90 1.20	0.30 0.90 1.20	V
V_{Hmax} Note 2	Maximum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.20 2.25 3.00	1.20 2.25 3.00	1.20 2.25 3.00	V
V_{Hmin} Note 2	Minimum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.20 0.40 0.50	0.20 0.40 0.50	0.20 0.40 0.50	V

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- $V_{Hmin} > (V_{T+min}) - (V_{Tmax})$; $V_{Hmax} = (V_{T+max}) - (V_{T-min})$.

MC54/74HC9014•MC54/74HC9015

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{OH}	Minimum High-Level Output Voltage	V _{in} ≤ V _{T- min} or V _{in} ≥ V _{T+ max} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} ≤ V _{T- min} or V _{in} ≥ V _{T+ max} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
		V _{in} ≥ V _{T+ max} or V _{in} ≤ V _{T- min} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} ≥ V _{T+ max} or V _{in} ≤ V _{T- min} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} ≥ V _{T+ max} or V _{in} ≤ V _{T- min} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
		V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Projected Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	HC9014	2.0	85	105	ns
			4.5	17	21	
			6.0	14	18	
		HC9015	2.0	95	120	
			4.5	19	24	
			6.0	16	20	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

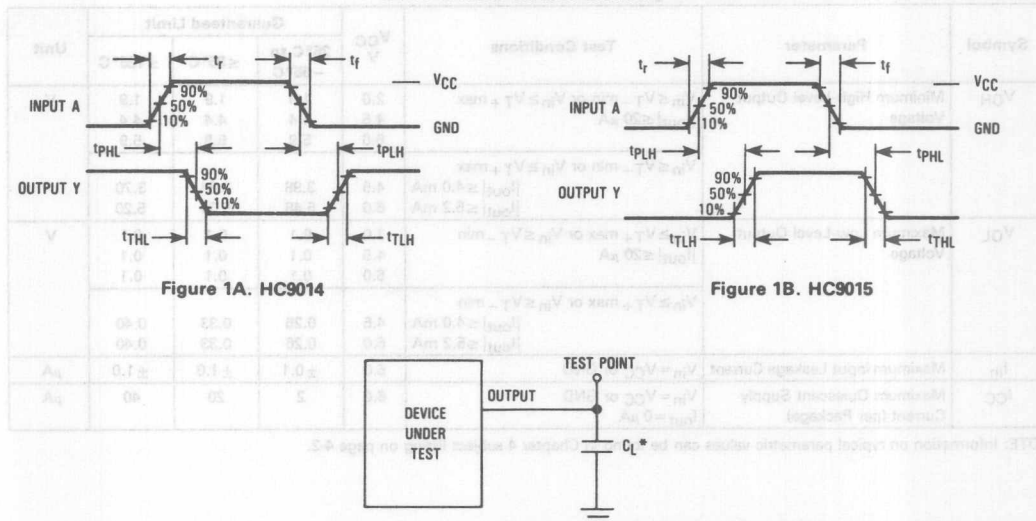
NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		30	

MC54/74HC9014•MC54/74HC9015

SWITCHING WAVEFORMS



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

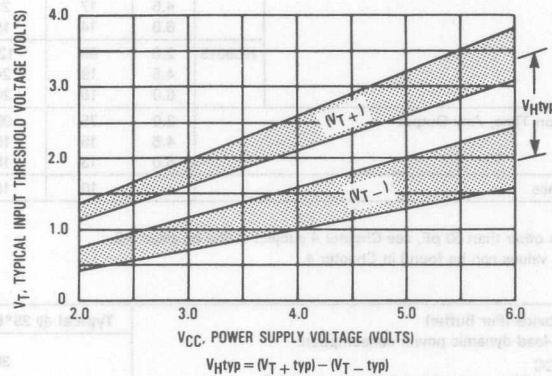
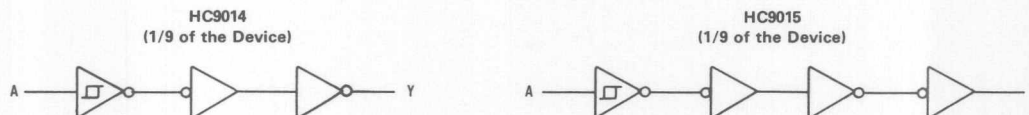


Figure 3. Typical Input Threshold, V_{T+} , V_{T-} Versus Power Supply Voltage

EXPANDED LOGIC DIAGRAMS



Advance Information

Nine-Wide Buffers

High-Performance Silicon-Gate CMOS

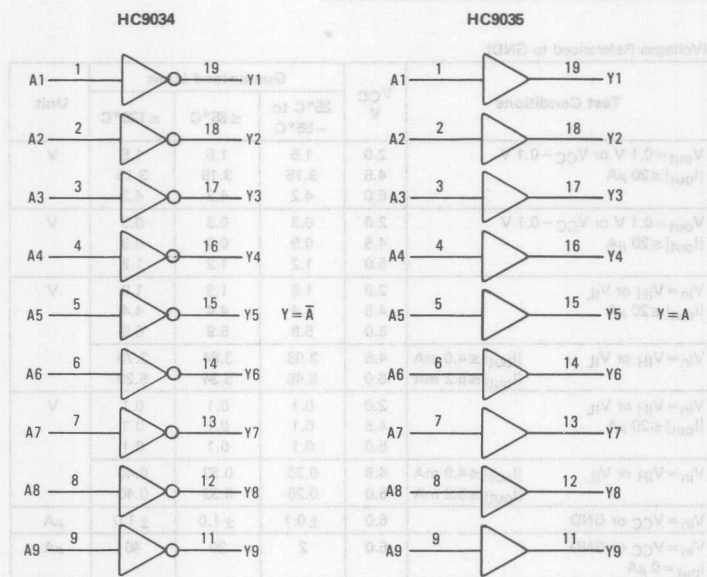
The MC54/74HC9034 consists of nine inverting buffers and the MC54/74HC9035 consists of nine noninverting buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices find primary use as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data are needed and an extra bit is required for parity, control, or handshake.

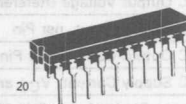
Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 54 FETs or 13.5 Equivalent Gates (HC9034)
72 FETs or 18 Equivalent Gates (HC9035)

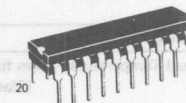
LOGIC DIAGRAMS



MC54/74HC9034 MC54/74HC9035



J SUFFIX
 CERAMIC
 CASE 732



N SUFFIX
 PLASTIC
 CASE 738



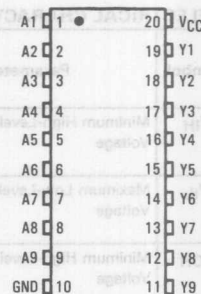
DW SUFFIX
 SOIC
 CASE 751D

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

T_A = -55° to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

A Input	Y Outputs	
	HC9034	HC9035
L	H	L
H	L	H

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V _{CC}	V
T _A	Operating Temperature, All Package Types		− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC9034•MC54/74HC9035

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	HC9034	2.0	80	100	ns
			4.5	16	20	
			6.0	14	17	
		HC9035	2.0	90	115	
			4.5	18	23	
			6.0	15	20	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)		2.0	75	95	ns
			4.5	15	19	
			6.0	13	16	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		30	

SWITCHING WAVEFORMS

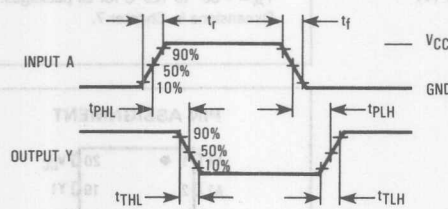


Figure 1A. HC9034

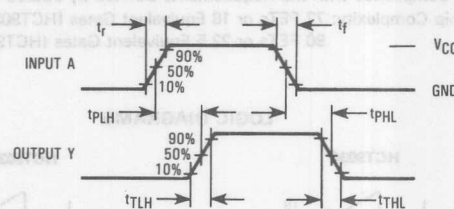
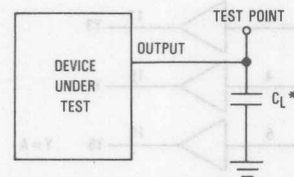


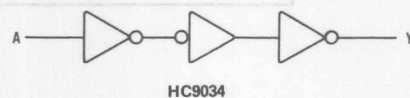
Figure 1B. HC9035



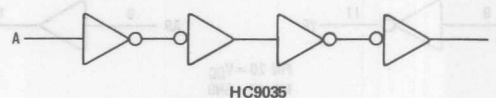
*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAMS (1/9 of the Device)



HC9034



HC9035

Advance Information **Nine Wide Buffers** **with LSTTL Compatible Inputs** **High-Performance Silicon-Gate CMOS**

The MC54/74HCT9034 and MC54/74HCT9035 may be used as level converters for interfacing TTL or NMOS outputs to CMOS inputs.

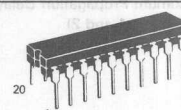
The HCT9034 consists of nine inverting buffers, and the HCT9035 consists of nine noninverting buffers.

These devices find primary use as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data is needed and an extra bit is required for parity, control or handshake.

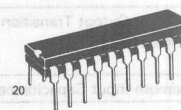
Using Nine Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates (HCT9034)
90 FETs or 22.5 Equivalent Gates (HCT9035)

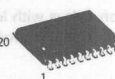
MC54/74HCT9034 **MC54/74HCT9035**



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



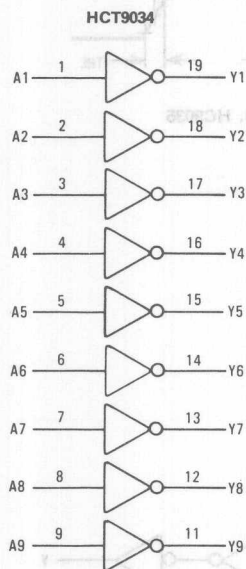
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

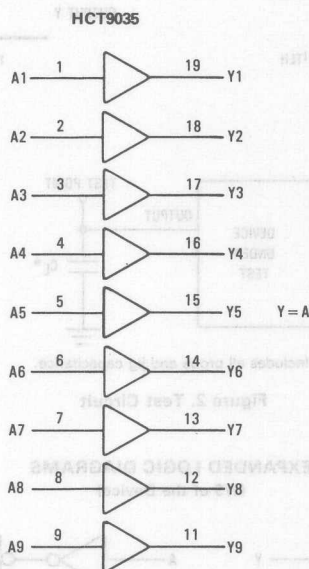
MC74HCTXXXXN	Plastic
MC54HCTXXXXJ	Ceramic
MC74HCTXXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAMS



$$Y = \bar{A}$$



$$Y = A$$

PIN 20 = V_{CC}
PIN 10 = GND

PIN ASSIGNMENT

A1	1	20	V_{CC}
A2	2	19	Y1
A3	3	18	Y2
A4	4	17	Y3
A5	5	16	Y4
A6	6	15	Y5
A7	7	14	Y6
A8	8	13	Y7
A9	9	12	Y8
GND	10	11	Y9

FUNCTION TABLE

A Input	Y Outputs	
	HCT9034	HCT9035
L	H	L
H	L	H

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HCT9034•MC54/74HCT9035

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	5.5	2	20	40	μA
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or GND, Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	$\geq -55^\circ\text{C}$ 2.9	25°C to 125°C 2.4		mA

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

Symbol	Parameter	Guaranteed Limit			Unit
		25°C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	23	29	35	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} =5.0 V 38	pF
-----	--	--	----

SWITCHING WAVEFORMS

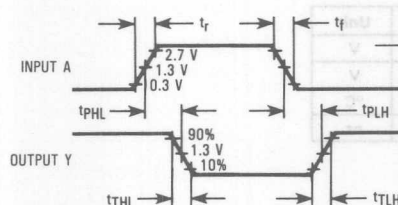


Figure 1A. HCT9034

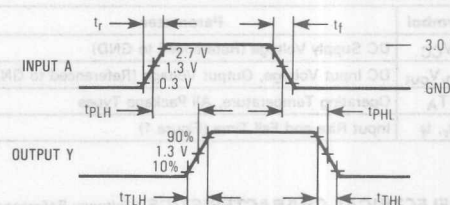
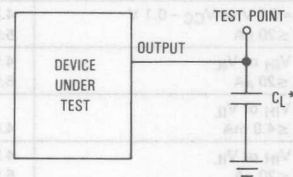


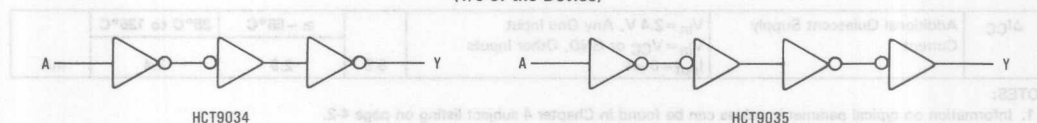
Figure 1B. HCT9035



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAMS (1/9 of the Device)



Product Preview

Nine-Wide Schmitt-Trigger Buffers with Open-Drain Outputs High-Performance Silicon-Gate CMOS

The MC54/74HC9114 consists of nine inverting Schmitt-Trigger Buffers, and the MC54/74HC9115 consists of nine noninverting Schmitt-Trigger Buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

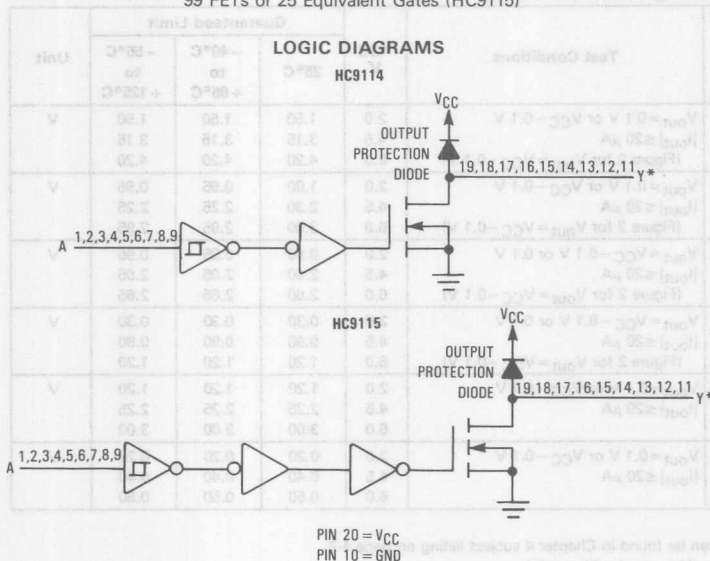
These devices have hysteresis and can, therefore, be used to enhance noise immunity or to square up slowly changing waveforms.

Primary use for these devices are as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data are needed and an extra bit is required for parity, control, or handshake.

Each of the HC9114 and HC9115 outputs are fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable output pullup resistor, these gates can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

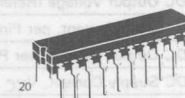
Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

- Output Drive Capability: 10 LSTTL Loads — with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 81 FETs or 20 Equivalent Gates (HC9114)
99 FETs or 25 Equivalent Gates (HC9115)

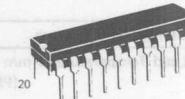


*Denotes open-drain outputs

MC54/74HC9114 MC54/74HC9115



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

A1	1	20	V _{CC}
A2	2	19	Y1
A3	3	18	Y2
A4	4	17	Y3
A5	5	16	Y4
A6	6	15	Y5
A7	7	14	Y6
A8	8	13	Y7
A9	9	12	Y8
GND	10	11	Y9

FUNCTION TABLE

A Inputs	Y Outputs	
	HC9114	HC9115
L	Z	L
H	L	Z

Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	no limit*	ns

*When $V_{in} = 0.5 V_{CC}$, $I_{CC} > I_{quiescent}$ current.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C	-40°C to +85°C	-55°C to +125°C	
V_{T+max}	Maximum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1 V$ or $V_{CC} - 0.1 V$ $ I_{out} \leq 20 \mu A$ (Figure 2 for $V_{out} = V_{CC} - 0.1 V$)	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	V
V_{T+min}	Minimum Positive-Going Input Threshold Voltage (Figure 3)	$V_{out} = 0.1 V$ or $V_{CC} - 0.1 V$ $ I_{out} \leq 20 \mu A$ (Figure 2 for $V_{out} = V_{CC} - 0.1 V$)	2.0 4.5 6.0	1.00 2.30 3.00	0.95 2.25 2.95	0.95 2.25 2.95	V
V_{T-max}	Maximum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1 V$ or $0.1 V$ $ I_{out} \leq 20 \mu A$ (Figure 2 for $V_{out} = V_{CC} - 0.1 V$)	2.0 4.5 6.0	0.90 2.00 2.60	0.95 2.05 2.65	0.95 2.05 2.65	V
V_{T-min}	Minimum Negative-Going Input Threshold Voltage (Figure 3)	$V_{out} = V_{CC} - 0.1 V$ or $0.1 V$ $ I_{out} \leq 20 \mu A$ (Figure 2 for $V_{out} = V_{CC} - 0.1 V$)	2.0 4.5 6.0	0.30 0.90 1.20	0.30 0.90 1.20	0.30 0.90 1.20	V
V_{Hmax} Note 2	Maximum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1 V$ or $V_{CC} - 0.1 V$ $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	1.20 2.25 3.00	1.20 2.25 3.00	1.20 2.25 3.00	V
V_{Hmin} Note 2	Minimum Hysteresis Voltage (Figure 3)	$V_{out} = 0.1 V$ or $V_{CC} - 0.1 V$ $ I_{out} \leq 20 \mu A$	2.0 4.5 6.0	0.20 0.40 0.50	0.20 0.40 0.50	0.20 0.40 0.50	V

NOTES:

- Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.
- $V_{Hmin} > (V_{T+min}) - (V_{T-max})$; $V_{Hmax} = (V_{T+max}) - (V_{T-min})$.

MC54/74HC9114•MC54/74HC9115

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{OL}	Maximum Low-Level Output Voltage	$V_{in} \geq V_{T+} \text{ max or } V_{in} \leq V_{T-} \text{ min}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} \geq V_{T+} \text{ max or } V_{in} \leq V_{T-} \text{ min}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0 \mu\text{A}$	6.0	2	20	40	μA
I _{OZ}	Maximum Output Leakage Current	$A = V_{T+} \text{ min or } V_{T-} \text{ max}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	±0.5	±5.0	±10.0	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter		V _{CC} V	Projected Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
t _{PLZ} , t _{PZL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	HC9114	2.0	115	145	175	ns
			4.5	23	29	35	
			6.0	20	25	30	
		HC9115	2.0	125	155	190	
			4.5	25	31	38	
			6.0	21	26	32	
t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)		2.0	75	95	110	ns
			4.5	15	19	22	
			6.0	13	16	19	
C _{in}	Maximum Input Capacitance		—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)		—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		15	

5

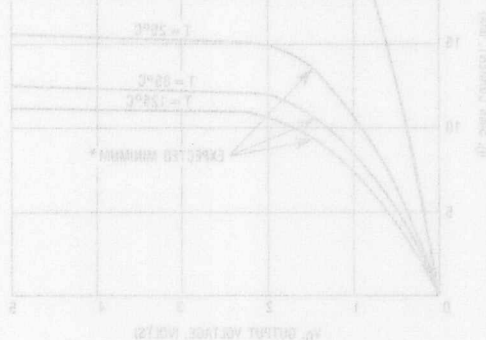
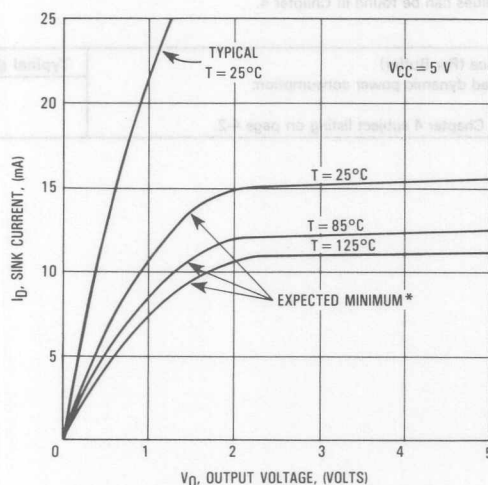
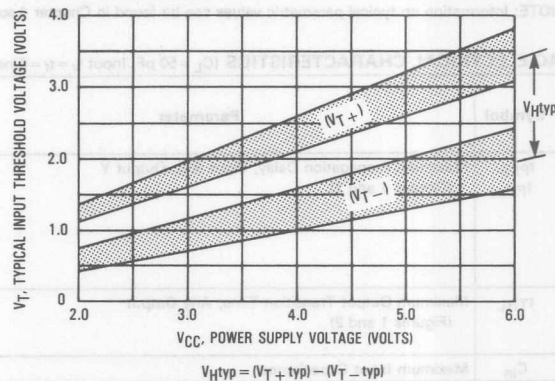
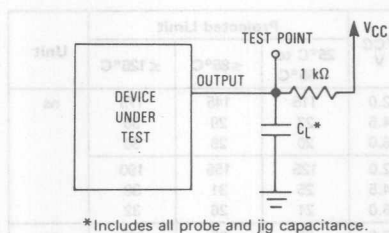
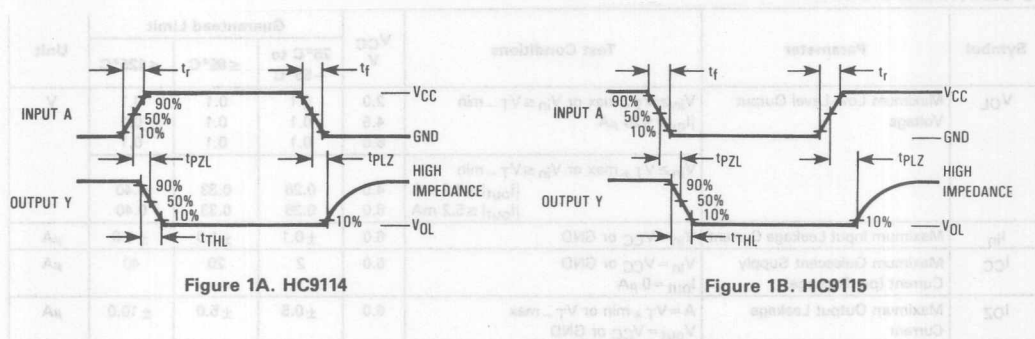


Figure 4. Open-Drain Output Characteristics
*The expected minimum current is not guaranteed but is shown only for reference.



*The expected minimum curves are not guarantees, but are design aids.

Product Preview

Nine-Wide Buffers with Open-Drain Outputs

High-Performance Silicon-Gate CMOS

The MC54/74HC9134 consists of nine inverting buffers and the MC54/74HC9135 consists of nine noninverting buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

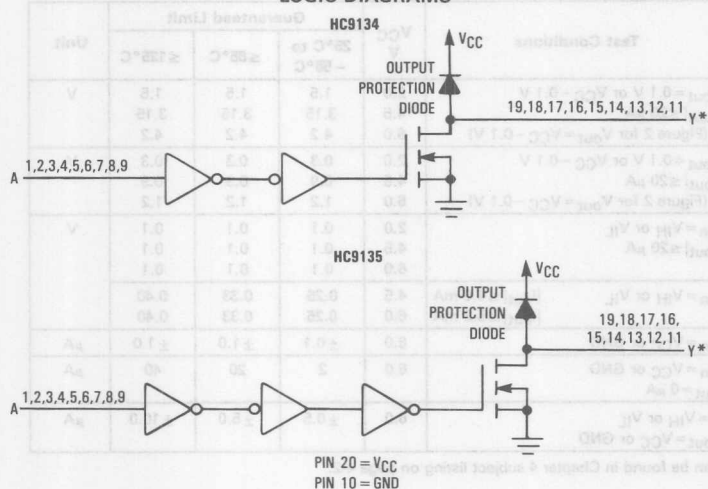
These devices find primary use as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data are needed and an extra bit is required for parity, control, or handshake.

Each of the HC9134 and HC9135 outputs are fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable pullup resistor, these gates can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

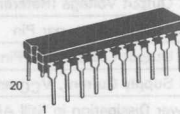
- Output Drive Capability: 10 LSTTL Loads — with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 45 FETs or 11.25 Equivalent Gates (HC9134)
63 FETs or 15.75 Equivalent Gates (HC9135)

LOGIC DIAGRAMS

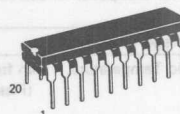


*Denotes open-drain outputs.

MC54/74HC9134 MC54/74HC9135



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT

A1	1	20	VCC
A2	2	19	Y1
A3	3	18	Y2
A4	4	17	Y3
A5	5	16	Y4
A6	6	15	Y5
A7	7	14	Y6
A8	8	13	Y7
A9	9	12	Y8
GND	10	11	Y9

FUNCTION TABLE

A Input	Y Outputs	
	HC9134	HC9135
L	Z	L
H	L	Z

Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC}+1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC}+0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds† (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC}=2.0\text{ V}$ 0 $V_{CC}=4.5\text{ V}$ 0 $V_{CC}=6.0\text{ V}$ 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{ V or } V_{CC} - 0.1\text{ V}$ $ I_{out} \leq 20\text{ }\mu\text{A}$ (Figure 2 for $V_{out} = V_{CC} - 0.1\text{ V}$)	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{ V or } V_{CC} - 0.1\text{ V}$ $ I_{out} \leq 20\text{ }\mu\text{A}$ (Figure 2 for $V_{out} = V_{CC} - 0.1\text{ V}$)	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20\text{ }\mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0\text{ mA}$ $ I_{out} \leq 5.2\text{ mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or GND}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or GND}$ $I_{out} = 0\text{ }\mu\text{A}$	6.0	2	20	40	μA
I_{OZ}	Maximum Output Leakage Current	$A = V_{IH} \text{ or } V_{IL}$ $V_{out} = V_{CC} \text{ or GND}$	6.0	± 0.5	± 5.0	± 10.0	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

MC54/74HC9134•MC54/74HC9135

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Projected Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLZ} , t_{PZL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	HC9134	2.0	115	145	ns
			4.5	23	29	
			6.0	20	25	
		HC9135	2.0	120	150	
			4.5	24	30	
			6.0	20	26	
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, $V_{CC} = 5.0$ V	pF
		15	

SWITCHING WAVEFORMS

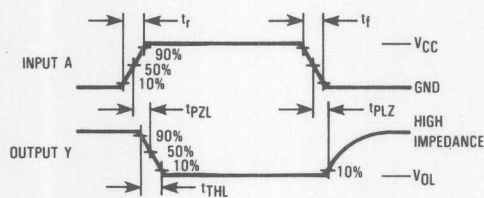


Figure 1A. HC9134

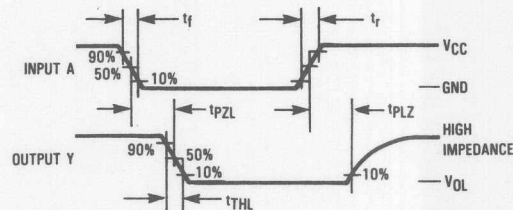
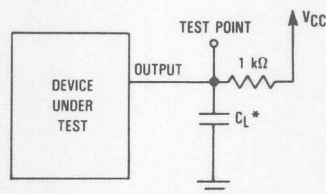
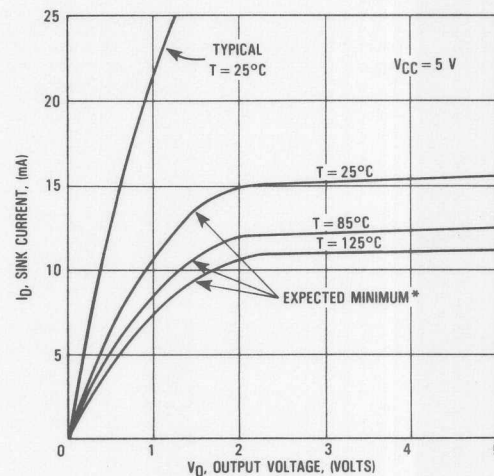


Figure 1B. HC9135



*Includes all probe and jig capacitance.

Figure 2. Test Circuit



*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

Symbol	Parameter	Unit
t_{PLZ} Figure 1 and 2	Maximum Propagation Delay, Input A to Output Y	ns
t_{PLZ}	Maximum Propagation Delay, Input A to Output Y	ns
t_{HL} Figure 1 and 2	Maximum Output Transition Time, Any Output	ns
C_{in}	Maximum Input Capacitance	pf
C_{out} (Load)	Maximum Three-State Output Capacitance (Output in High-Impedance State)	pf

NOTES:

- For propagation delays with loads other than 50 pf, see Chapter 4 subject listing on page 4-5.
- Information on typical parameter values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (See Bottom)	pf
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-5.	
	Typical @ 25°C, $V_{CC} = 5.0$ V	18

SWITCHING WAVEFORMS



Figure 1A. HC133A

Figure 1B. HC133B

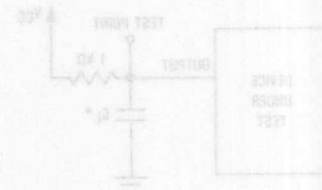


Figure 2. Test Circuit

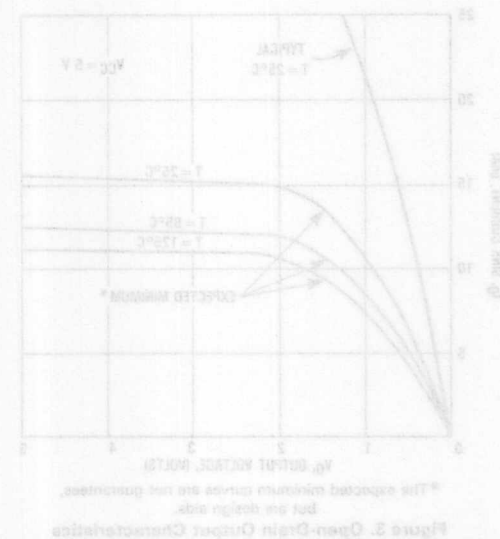


Figure 3. Open-Drain Output Characteristics
*The expected minimum curves are not guaranteed, but are design aids.

RELIABILITY

INTRODUCTION

The Motorola High-Speed CMOS Reliability monitor program is designed to generate an ongoing data base of reliability performance for High-Speed CMOS Logic devices. The primary purpose of the program is to identify negative trends in the data so that immediate corrective action can be taken. The program also allows Motorola to develop a large data base of reliability information. This information is made available to customers on a quarterly and yearly basis. The High-Speed CMOS data base consists of results obtained from over 6500 devices from 144 lots.

ACCELERATED LIFE TEST

Accelerated life testing is used to simulate long-term device operation and to gather data for failure rate predictions. The test is conducted at an ambient temperature of 125°C with devices biased at 5 volts. A complete functional and dc parameter test to data sheet specifications is performed after 100, 1000, and 10000 cumulative hours. A device is considered to have failed if parameters listed are exceeded or if functionality cannot be demonstrated under nominal and worst-case conditions specified in the data sheet. Forms of mechanical damage, such as cracking of the package, are also considered failures.

A complete summary of accelerated life test data is presented in Tables 1 and 2, and Figure 1. Accelerated life testing is also referred to as high temperature operating life testing or high temperature reverse bias testing.

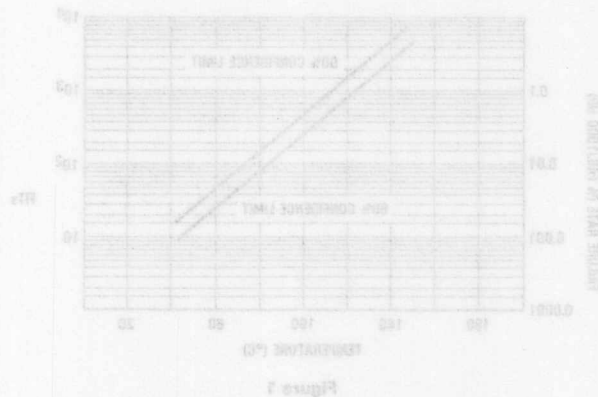
Table 1. 1985 Life Test Data
125°C 5 V

YHCOXX	% of	Lot	Hours	Hours	% Failures
1985	36	21302	01308	31281	0.10
Total			100	1000	

Table 2. Summary of 1985 Life Test Data

YHCOXX	Total	125°C	85°C	55°C
Failures	4	Device Hours	Equivalent	Equivalent
1985	1	3.50 x 10 ⁵	3.70 x 10 ⁷	2.70 x 10 ⁸
1986	3			

100 FITS = 0.01%/1000 hours
* See Figure 1 which depicts failure rate versus temperature.
*** 0.1% 5V; 60% Confidence Limit
** 0.1% 5V; 90% Confidence Limit



Reliability 6

RELIABILITY

INTRODUCTION

The Motorola High-Speed CMOS Reliability monitor program is designed to generate an ongoing data base of reliability performance for High-Speed CMOS Logic devices. The primary purpose of the program is to identify negative trends in the data so that immediate corrective action can be taken. The program also allows Motorola to develop a large data base of reliability information. This information is made available to customers on a quarterly and yearly basis. The 1985 High-Speed CMOS data base consists of results obtained from over 9500 devices from 144 lots.

ACCELERATED LIFE TEST

Accelerated life testing is used to simulate long-term device operation and to gather data for failure rate predictions. The test is conducted at an ambient temperature of 125°C with devices biased at 5 volts. A complete functional and dc parametric test to data sheet specifications is performed after 48, 168, and 1008 cumulative hours. A device is considered to have failed if parametric limits are exceeded or if functionality cannot be demonstrated under nominal and worst-case conditions specified in the data sheet. Forms of mechanical damage, such as cracking of the package, are also considered failures.

A complete summary of accelerated life test data is presented in Tables 1 and 2, and Figure 1.

Accelerated life testing is also referred to as high temperature operating life testing or high temperature reverse bias testing.

Table 1. 1985 Life Test Data
125°C 5 V

74HCXXX	# of Lots	48 Hours	168 Hours	1008 Hours	Total % Failures
Plastic	38	2/3763	0/3758	2/3751	0.10

Table 2. Summary of 1985 Life Test Data

74HCXXX	Total Failures	125°C Device Hours	85°C Equivalent Device Hours	85°C* Predicted Failure Rate FITs
Plastic	4	3.80×10^6	3.70×10^7	219** 141***

100 FITs = 0.01%/1000 hours

*See Figure 1 which depicts failure rate versus temperature.

**0.7 eV; 90% Confidence Limit

***0.7 eV; 60% Confidence Limit

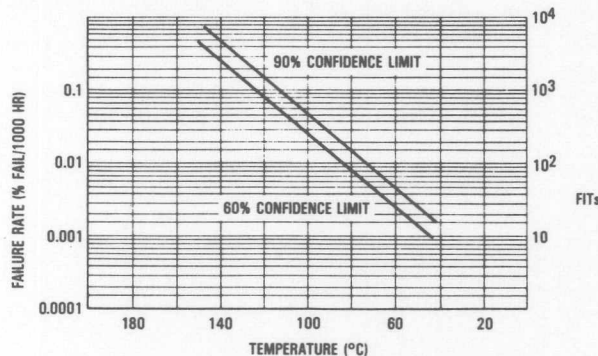


Figure 1

RELIABILITY

TEMPERATURE HUMIDITY BIAS

Temperature Humidity Bias (THB) is an environmental test designed to evaluate the moisture-related performance of the package-die combination. THB is a destructive test performed under a 5 volt bias at 85°C and 85% relative humidity. Electrical performance is measured at 504 and 1008 hours to full data sheet specifications. A device is considered to have failed the temperature humidity bias test if parametric limits are exceeded or if functionality cannot be demonstrated under the conditions specified in the data sheet. Results of the 1985 temperature humidity bias testing are shown in Table 3.

Table 3. Temperature Humidity Bias
85°C 85% R.H. 5 Volts

74HCXXX	# of Lots	504 Hours	1008 Hours	% Failures
Plastic	33	0/2231	1/2086	0.05

AUTOClave

Autoclave, like THB, is an environmental test which measures device resistance to moisture penetration along the lead-frame-plastic interface. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig; no bias voltage is applied. Corrosion of the die is the expected failure mechanism. As with THB testing, both package integrity and actual die construction play a major role in the results. Autoclave is a highly accelerated, destructive test.

Failure criteria for autoclave testing are the same as those used for THB testing. Cosmetic package defects and degradation of lead finish and solderability are not considered as reject criteria.

Autoclave results for 1985 are found in Table 4. The single failure, detected at the 144 hour test point, failed for input leakage; no corrosion was found.

Table 4. Autoclave
121°C 100% R.H. 15 psig

74HCXXX	# of Lots	144 Hours	240 Hours	% Failures
Plastic	41	1/1995	0/2084	0.05

TEMPERATURE CYCLE

The compatibility of materials used in the fabrication of any device is essential to its reliability. Any appreciable mismatch in physical properties, such as thermal expansion coefficients, can cause long-term device failures. Those concerns are investigated by performing temperature cycling.

During temperature cycle testing, devices are loaded into a cycling system and held at -65°C for at least ten minutes, then brought to +150°C for at least ten minutes. The system employs a circulating air environment to assure rapid stabilization at the specified temperatures. The dwell at each extreme, plus two transition periods of five minutes, constitute one cycle.

Devices are electrically tested after 500 and 1000 cumulative cycles. A device is defined as a failure if parametric limits are exceeded, or if functionality cannot be demonstrated per data sheet specifications. Mechanical damage, such as cracking, chipping, or breaking of the package, are also considered as failure criteria, provided such damage was not induced by fixturing or handling. Results of temperature cycle tests are found in Table 5.

Table 5. Temperature Cycle
-65°C to +150°C

74HCXXX	# of Lots	500 Cycles	1000 Cycles	Cumulative % Failures
Plastic	32	1/1803	0/1800	0.05

CONCLUSIONS

Thorough reliability testing has been performed on an extensive cross section of the High-Speed CMOS Logic family. The evaluations included accelerated life tests and a series of environmental stresses designed to assess package integrity, moisture resistance, and thermal compatibility. Through these tests, Motorola's High-Speed CMOS has proven to be an exceptionally reliable family of devices. Reliability testing is performed on a continuous basis, and comprehensive reports are issued annually. Reports are available upon customer request.

For additional information, contact CMOS Logic Reliability Engineering at:

CMOS Logic Reliability Engineering
Motorola Inc.
3501 Ed Bluestein Boulevard
Austin, Texas 78721

The consistency of materials used in the fabrication of any device is essential to its reliability. Any appreciable mismatch in physical properties, such as thermal expansion coefficients, can cause long-term device failures. These concerns are investigated by performing temperature cycling.

During temperature cycle testing, devices are loaded into a cycling system and held at -85°C for at least ten minutes, then brought to $+125^{\circ}\text{C}$ for at least ten minutes. The system employs a circulating air environment to assure rapid equilibration at the specified temperatures. The dwell at each extreme, plus two transition periods of five minutes, constitutes one cycle.

Devices are electrically tested after 500 and 1000 cumulative cycles. A device is defined as a failure if parametric limits are exceeded, or if functionality cannot be demonstrated per data sheet specifications. Mechanical damage, such as cracking, chipping, or breaking of the package, are also considered as failure criteria. Provided such damage was not induced by handling or handling. Results of temperature cycle tests are found in Table 5.

Table 5. Temperature Cycle
 -85°C to $+125^{\circ}\text{C}$

PARAMETER	% of Lots	500 Cycles	1000 Cycles	Cumulative % Failures
Plastic	50	11/1000	0/1000	0.00

CONCLUSIONS

Thorough reliability testing has been performed on an extensive cross section of the High-Speed CMOS Logic family. The evaluations included accelerated life tests and a series of environmental stresses designed to assess package integrity, moisture resistance, and thermal compatibility. Through these tests, Motorola's High-Speed CMOS has proven to be an exceptionally reliable family of devices. Reliability testing is performed on a continuous basis, and comprehensive reports are issued annually. Reports are available upon customer request.

For additional information, contact CMOS Logic Reliability

Engineering at:
CMOS Logic Reliability Engineering
Motorola Inc.
3801 Ed Bluestein Boulevard
Austin, Texas 78721

Temperature Humidity Bias (THB) is an environmental test designed to evaluate the moisture-related performance of the package-de connection. THB is a destructive test performed under a 2 volt bias at 85°C and 85% relative humidity. Electrical performance is measured at 504 and 1008 hours to full data sheet specifications. A device is considered to have failed the test if it functionally cannot be demonstrated under the conditions specified in the data sheet. Results of the THB temperature humidity bias testing are shown in Table 3.

Table 3. Temperature Humidity Bias
 85°C 85% R.H. 2 Volts

PARAMETER	% of Lots	504 Hours	1008 Hours	% Failures
Plastic	50	0/2231	1/2008	0.00

AUTOCUVE

Autocuve, like THB, is an environmental test which measures device resistance to moisture penetration along the lead-frame package interface. Conditions employed during the test include 125°C , 100% relative humidity, and 18 p.p.s. no bias voltage is applied. Corrosion of the die is the expected failure mechanism. As with THB testing, both package integrity and actual die connection play a major role in the results. Autocuve is a highly accelerated, destructive test.

Failure criteria for autocuve testing are the same as those used for THB testing. Cosmetic package defects and degradation of lead finish and solderability are not considered as reject criteria.

Autocuve results for 1008 are found in Table 4. The single failure, detected at the 144 hour test point, failed for input leakage; no corrosion was found.

Table 4. Autocuve

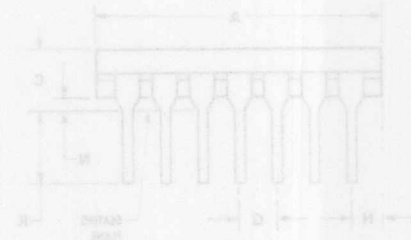
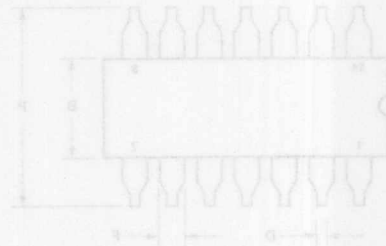
PARAMETER	% of Lots	144 Hours	288 Hours	% Failures
Plastic	47	1/1008	0/2004	0.00

PACKAGE DIMENSIONS

The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

14-PIN PACKAGES

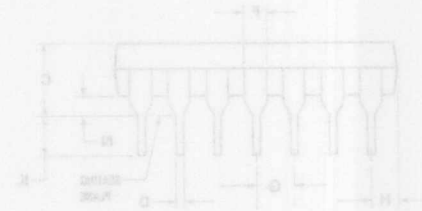
14-PIN
CERAMIC
CASE 623-01



DIMENSIONS		MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX	MIN
A	12.90	12.94	0.508	0.510	0.020
B	6.10	6.14	0.240	0.242	0.008
C	—	0.00	—	0.000	0.000
D	0.30	0.33	0.012	0.013	0.001
E	1.50	1.53	0.059	0.060	0.002
F	—	0.00	—	0.000	0.000
G	0.34	0.36	0.014	0.015	0.001
H	1.81	1.84	0.071	0.073	0.003
I	0.30	0.33	0.012	0.013	0.001
J	1.50	1.53	0.059	0.060	0.002
K	1.50	1.53	0.059	0.060	0.002
L	1.50	1.53	0.059	0.060	0.002
M	—	0.00	—	0.000	0.000
N	0.34	0.36	0.014	0.015	0.001
O	0.34	0.36	0.014	0.015	0.001

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-601 AS OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
4. LEADS WITHIN 1.25 mm (0.049 in) DIA OF TUBE.
5. POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

14-PIN
PLASTIC
CASE 646-01



DIMENSIONS		MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX	MIN
A	12.90	12.94	0.508	0.510	0.020
B	6.10	6.14	0.240	0.242	0.008
C	—	0.00	—	0.000	0.000
D	0.30	0.33	0.012	0.013	0.001
E	1.50	1.53	0.059	0.060	0.002
F	—	0.00	—	0.000	0.000
G	0.34	0.36	0.014	0.015	0.001
H	1.81	1.84	0.071	0.073	0.003
I	0.30	0.33	0.012	0.013	0.001
J	1.50	1.53	0.059	0.060	0.002
K	1.50	1.53	0.059	0.060	0.002
L	1.50	1.53	0.059	0.060	0.002
M	—	0.00	—	0.000	0.000
N	0.34	0.36	0.014	0.015	0.001
O	0.34	0.36	0.014	0.015	0.001

NOTES:
1. LEADS WITHIN 1.25 mm (0.049 in) DIA OF TUBE.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD.
4. LEADS WITHIN 1.25 mm (0.049 in) DIA OF TUBE.
5. POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

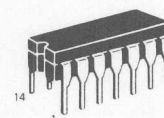
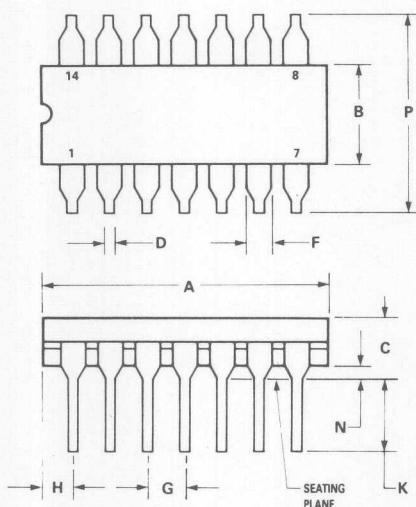
Package Dimensions 7

PACKAGE DIMENSIONS

The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

14-PIN PACKAGES

**J SUFFIX
CERAMIC
CASE 632-07**

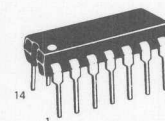
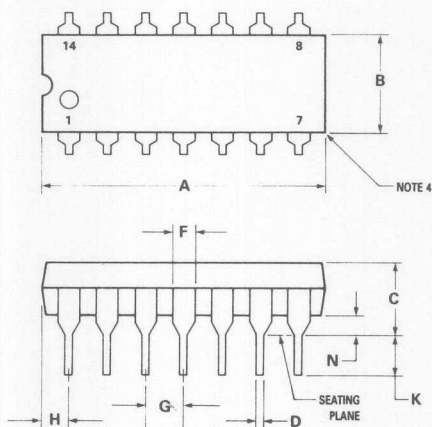


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:

- ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "A" AND "B" (632-07) DO NOT INCLUDE GLASS RUN-OUT. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE
- POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

**N SUFFIX
PLASTIC
CASE 646-06**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

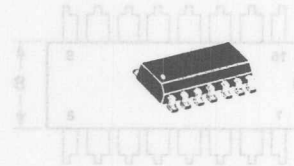
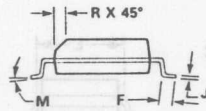
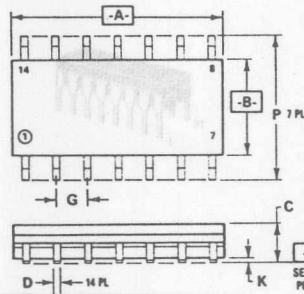
NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.

PACKAGE DIMENSIONS

14-PIN PACKAGES

D SUFFIX
SOIC
CASE 751A-02



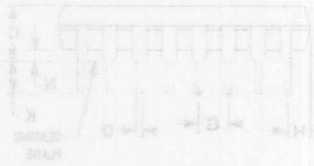
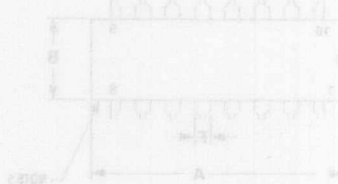
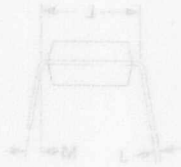
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751A-02

NOTES:

- DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
- POSITIONAL TOLERANCE FOR D DIMENSION (14 PLACES):
 $\pm 0.25 (0.010) \text{ T B } \textcircled{A}$
- POSITIONAL TOLERANCE FOR P DIMENSION (7 PLACES):
 $\pm 0.25 (0.010) \text{ B } \textcircled{P}$
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

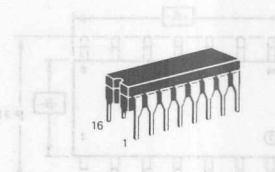
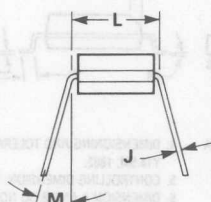
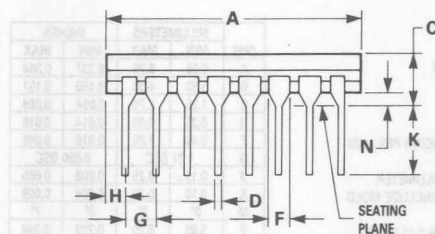
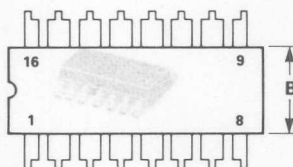
MILLIMETERS		INCHES	
MIN	MAX	MIN	MAX
8.55	8.75	0.337	0.344
3.80	4.00	0.150	0.157
1.35	1.75	0.054	0.068
0.35	0.49	0.014	0.019
0.40	1.25	0.016	0.049
1.27 BSC		0.050 BSC	
0.19	0.25	0.008	0.009
0.10	0.25	0.004	0.009
0°	7°	0°	7°
5.80	6.20	0.229	0.244
0.25	0.50	0.010	0.019



MILLIMETERS		INCHES	
MIN	MAX	MIN	MAX
8.55	8.75	0.337	0.344
3.80	4.00	0.150	0.157
1.35	1.75	0.054	0.068
0.35	0.49	0.014	0.019
0.40	1.25	0.016	0.049
1.27 BSC		0.050 BSC	
0.19	0.25	0.008	0.009
0.10	0.25	0.004	0.009
0°	7°	0°	7°
5.80	6.20	0.229	0.244
0.25	0.50	0.010	0.019

- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE PARALLEL.
 - POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 - PACKAGE INDEX NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
 - DIMENSION "T" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE PARALLEL.
 - POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 - PACKAGE INDEX NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.

**J SUFFIX
CERAMIC
CASE 620-08**

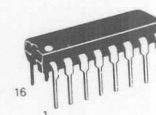
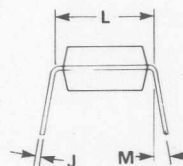
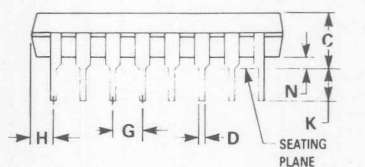
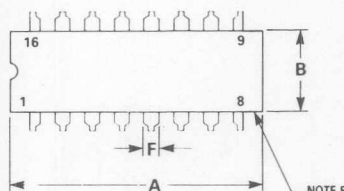


NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
- DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

**N SUFFIX
PLASTIC
CASE 648-06**



NOTES:

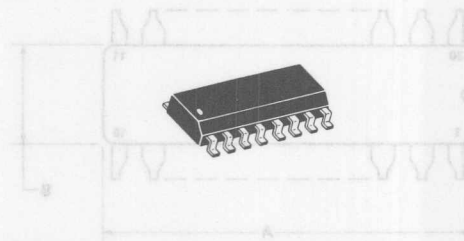
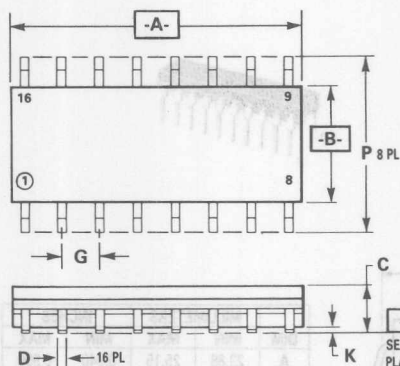
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- "F" DIMENSION IS FOR FULL LEADS.
- ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

PACKAGE DIMENSIONS

16-PIN PACKAGES

D SUFFIX
SOIC
CASE 751B-03



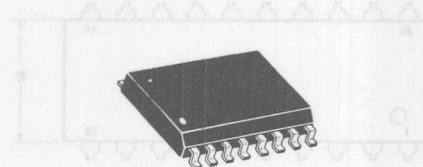
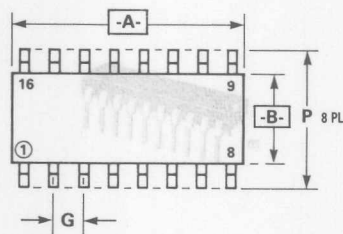
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751B-03

NOTES:

- DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
- POSITIONAL TOLERANCE FOR D DIMENSION (16 PLACES):
 $\pm 0.25 (0.010) (M) T B (S) A (S)$
- POSITIONAL TOLERANCE FOR P DIMENSION (8 PLACES):
 $\pm 0.25 (0.010) (M) B (M)$
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DW SUFFIX
SOIC
CASE 751B-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

CASE 751G-01

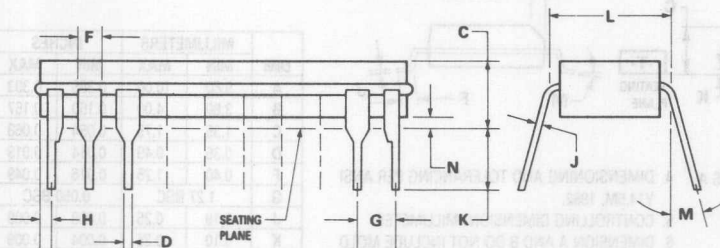
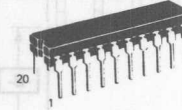
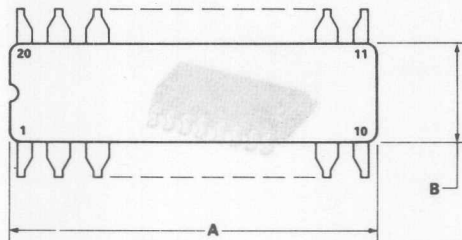
NOTES:

- DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
- POSITIONAL TOLERANCE FOR D DIMENSION (16 PLACES):
 $\pm 0.25 (0.010) (M) T B (S) A (S)$
- POSITIONAL TOLERANCE FOR P DIMENSION (8 PLACES):
 $\pm 0.25 (0.010) (M) B (M)$
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

PACKAGE DIMENSIONS

20-PIN PACKAGES

J SUFFIX
CERAMIC
CASE 732-03

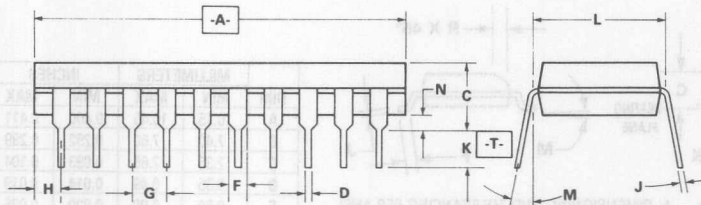
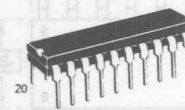
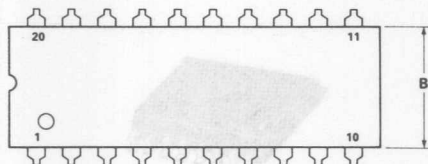


NOTES:

- LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
- DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

N SUFFIX
PLASTIC
CASE 738-02



NOTES:

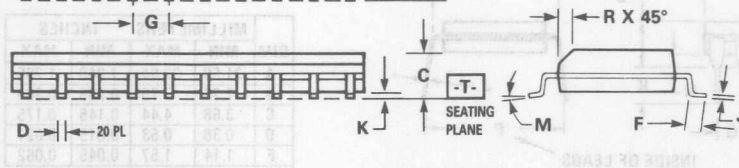
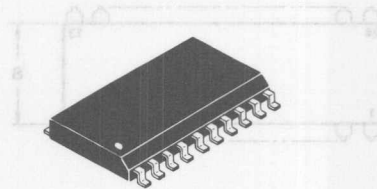
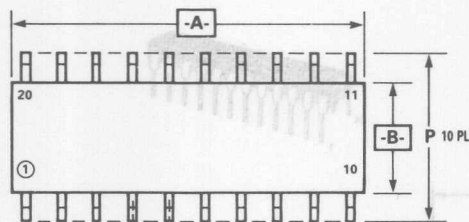
- DIM \boxed{A} IS DATUM.
- POSITIONAL TOL FOR LEADS:
 $\boxed{\phi 0.25 (0.010) \text{ M T A}}$
- \boxed{T} IS SEATING PLANE.
- DIM "B" DOES NOT INCLUDE MOLD FLASH.
- DIM \boxed{L} TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.65 NOM		0.065 NOM	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

PACKAGE DIMENSIONS

20-PIN PACKAGES

DW SUFFIX
SOIC
CASE 751D-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.509
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

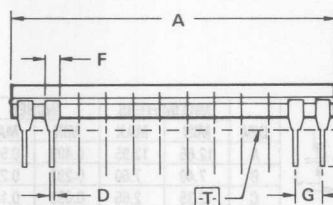
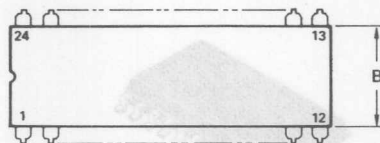
CASE 751D-02

NOTES:

- DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
- POSITIONAL TOLERANCE FOR D DIMENSION (20 PLACES):
 $\pm 0.25 (0.010) \text{ (M) T B (S) A (S)}$
- POSITIONAL TOLERANCE FOR P DIMENSION (10 PLACES):
 $\pm 0.25 (0.010) \text{ (M) B (M)}$
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MIN	MAX	DIM	MIN	MAX
A	12.65	12.95	A	12.65	12.95
B	7.40	7.60	B	7.40	7.60
C	2.35	2.65	C	2.35	2.65
D	0.35	0.49	D	0.35	0.49
E	0.50	0.90	E	0.50	0.90
F	0.50	0.90	F	0.50	0.90
G	1.27 BSC		G	1.27 BSC	
H	0.25	0.32	H	0.25	0.32
I	0.10	0.25	I	0.10	0.25
J	0°	7°	J	0°	7°
K	0.10	0.25	K	0.10	0.25
L	0.10	0.25	L	0.10	0.25
M	0.10	0.25	M	0.10	0.25
N	0.10	0.25	N	0.10	0.25
O	0.10	0.25	O	0.10	0.25
P	10.05	10.55	P	10.05	10.55
Q	0.10	0.25	Q	0.10	0.25
R	0.10	0.25	R	0.10	0.25
S	0.10	0.25	S	0.10	0.25
T	0.10	0.25	T	0.10	0.25
U	0.10	0.25	U	0.10	0.25
V	0.10	0.25	V	0.10	0.25
W	0.10	0.25	W	0.10	0.25
X	0.10	0.25	X	0.10	0.25
Y	0.10	0.25	Y	0.10	0.25
Z	0.10	0.25	Z	0.10	0.25

J SUFFIX
CERAMIC
CASE 758-01

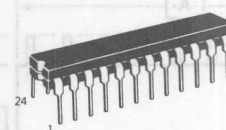


INSIDE OF LEADS

NOTES:

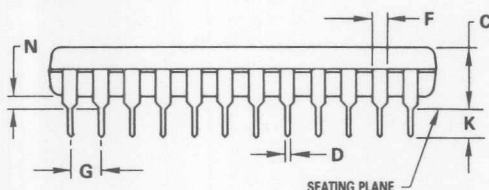
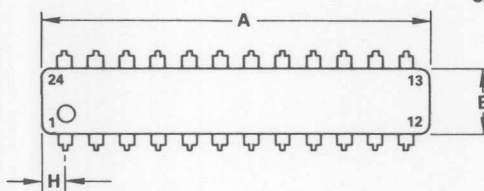
1. DIMENSION A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES
3. [T] IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

$\oplus 0.25 (0.010) (M) T A (M)$

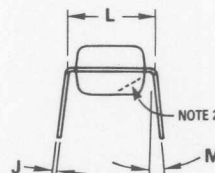


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

N SUFFIX
PLASTIC
CASE 724-02



SEATING PLANE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.13	1.230	1.265
B	6.35	6.86	0.250	0.270
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040

NOTES:

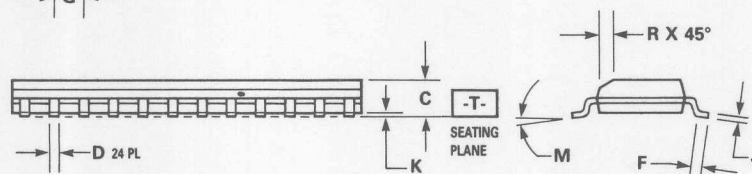
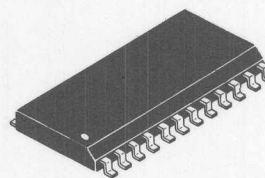
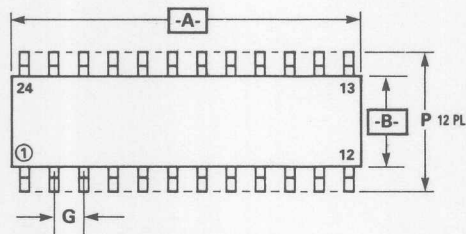
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).
2. CHAMFERED CONTOUR OPTIONAL.

7

PACKAGE DIMENSIONS

24-PIN PACKAGES

DW SUFFIX
SOIC
CASE 751E-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.50	0.601	0.610
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:

- DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
- POSITIONAL TOLERANCE FOR D DIMENSION (24 PLACES):
- POSITIONAL TOLERANCE FOR P DIMENSION (12 PLACES):
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

$\pm 0.25 (0.010) \text{ (M)} \text{ T B } \text{ (S)} \text{ A } \text{ (S)}$

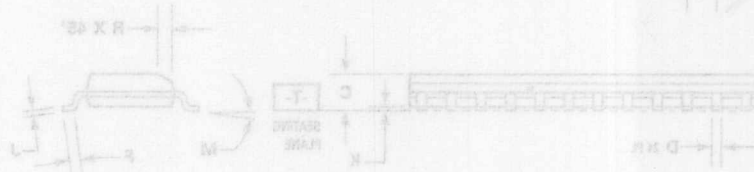
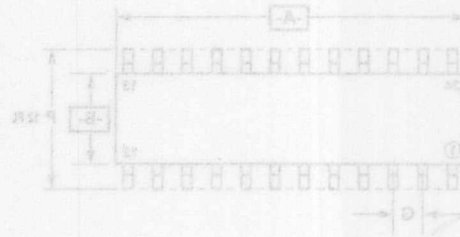
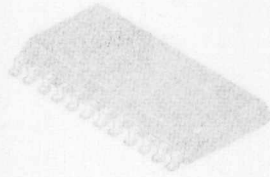
$\pm 0.25 (0.010) \text{ (M)} \text{ B } \text{ (M)}$

CASE 751E-01

PACKAGING NOTES

24-PIN PACKAGES

DW SUPPLY
SOLIC
CASE 7516-01



DIM	MIN	MAX	MIN	MAX
A	15.25	16.50	0.601	0.650
B	1.40	1.60	0.055	0.063
C	1.38	1.58	0.054	0.062
D	0.35	0.45	0.014	0.018
E	0.50	0.60	0.020	0.024
F	1.35	1.55	0.053	0.061
G	0.35	0.45	0.014	0.018
H	0.10	0.20	0.004	0.008
I	0.10	0.20	0.004	0.008
J	0.10	0.20	0.004	0.008
K	0.10	0.20	0.004	0.008
L	0.10	0.20	0.004	0.008
M	0.10	0.20	0.004	0.008
N	0.10	0.20	0.004	0.008
O	0.10	0.20	0.004	0.008
P	0.10	0.20	0.004	0.008
Q	0.10	0.20	0.004	0.008
R	0.10	0.20	0.004	0.008
S	0.10	0.20	0.004	0.008
T	0.10	0.20	0.004	0.008
U	0.10	0.20	0.004	0.008
V	0.10	0.20	0.004	0.008
W	0.10	0.20	0.004	0.008
X	0.10	0.20	0.004	0.008
Y	0.10	0.20	0.004	0.008
Z	0.10	0.20	0.004	0.008

CASE 7516-01

1. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE
2. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION
3. CONTROLLING DIMENSION: MILLIMETER
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1987
5. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE
6. POSITIONAL TOLERANCE FOR D DIMENSION (IN PLACES)
7. POSITIONAL TOLERANCE FOR P DIMENSION (IN PLACES)

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (IN PLACES)
3. POSITIONAL TOLERANCE FOR P DIMENSION (IN PLACES)
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1987
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION
6. CONTROLLING DIMENSION: MILLIMETER
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE